FNAL E690 is a large acceptance, high rate, multiparticle spectrometer which will be capable of recording several $10^5$ Beauty events/fixed target run within the next few years. The spectrometer is currently capable of taking "high" interaction rates (a few $10^6$ interactions/second) which are reduced by "open" triggers to $10^5$ events/sec. These events are fully reconstructed in real time and the event summary information can be used for triggering.

Introduction

FNAL E690 is the continuation of a series of experiments started with BNL E766. The objective of these experiments is the comprehensive study of the spectroscopy and production of particles with strangeness, charm and beauty quantum numbers. At BNL the experiment ran with beams of neutrons (momentum spectrum up to 24 GeV/c) and protons (28 GeV/c) incident on a liquid hydrogen target. At FNAL the beam will be protons (800 GeV/c) incident on the same apparatus.

In both experiments the final states of interest are those for which all final state particles are measured. The kinematic constraints from those fully reconstructed events significantly improve signal-to-background for heavy particle spectroscopy. The spectrometer acceptance is large enough to contain these events with modest losses.

To obtain a sufficient number of events to perform the study, the acquisition and trigger subsystems of the apparatus were designed to operate at megacycle interaction rates. The first two levels of trigger identify potentially high multiplicity events in a relatively unbiased manner. The third level trigger is based on the complete reconstruction of the event. At this level, very complex triggers can be formed in a flexible manner, analogous to offline data summary trigger decisions.

The uniform architecture of the data acquisition system and trigger system is the result of a coherent approach to design. The apparatus, electronics, reconstruction software, physics measurements, etc. were all considered in the initial design stages. High bandwidth, measurement redundancy, "reconstructability", (the ability to efficiently reconstruct trajectories from the spectrometer data), maintainability, and low cost were among the considerations. Because of these requirements, all of the design was undertaken "in house". The architecture chosen for this system is data driven, parallel pipelined, distributed and synchronous. The implementation
of the design was undertaken in ECL technology which has high bandwidths and excellent reliability. The architecture readily admits other technologies (e.g. CMOS, etc.) and other devices (e.g. DSPs, etc.).

In the following sections some relevant spectrometer details will be discussed. The general triggering scheme, emphasizing the on-line reconstruction hardware will be described, along with currently realized performance. The conclusion will address the question of applicability to high sensitivity Beauty physics.

**Spectrometer**

Figure 1 shows a plan view of the spectrometer. This spectrometer has 6 MWPC chamber stations with 4-views per station located within the dipole magnet M1. The field of M1 is non-uniform and is 7kGauss maximum on beamline in the center of the magnet. The acceptance of this spectrometer extends to 300 milliradians for particles which pass through all 6 chambers. Tracks passing through 3, 4, and 5 chambers are also accepted and reconstructed. The entire length of this detector is 11 feet. The measurement of the high momentum forward particles is accomplished in FNAL E690 Stage II with 4 additional chambers and another dipole magnet, M2. The forward spectrometer acceptance goes out to 100 milliradians. Not shown in Figure 1 are the 2 beam spectrometers each comprised of 2 chambers followed by a dipole magnet train which in turn are followed by 2 chambers. The upstream beam spectrometer measures the initial beam particle 3-momenta, the downstream spectrometer measures an outgoing beam system which has a low multiplicity (e.g. 1 particle, as in a target dissociation event).

The drift chambers were built to minimize both measurement and recovery times, with standard MWPC narrow spaced anode wires (2mm to 3.5mm) and thin anode-to-cathode spacing (3mm). All 4 views are "bending" views which provides a redundant measurement of the track momentum, allowing for small inefficiencies in the chamber system and to facilitate pattern recognition in reconstruction. The drift chamber TDC's record for each wire the digital time of the first coincidence within a narrow gate (40ns to 60ns) in 2.5ns bins.

Not shown in Figure 1 are the 200 channels of scintillator counters used to trigger the spectrometer and to provide time-of-flight measurements for particle identification. The particle identification also utilizes the highly segmented (96 channel) threshold Cerenkov counter (CO). The FNAL E690 Stage II apparatus will be expanded to provide additional particle identification using ring imaging Cerenkov counters (C1 and C2) and to have neutrals detection (calorimeters).

The BNL E766/FNAL E690 Stage I detector has roughly 14000 channels of MWPC and 300 channel of phototube pulse height and time information. The FNAL E690 Stage II detector will have an additional 8,000 MWPC, 300 phototubes and 10,000 ADC channels.

**Acquisition and Triggering**

The data acquisition system, triggering and reconstruction electronics architectures are data driven. Figure 2 shows the event flow rates through the system along with the number of signals which are associated with triggering decisions at each level. The system is pipelined which allows
multiple events to be considered throughout the triggering system.

An event is defined with increasingly complex characterization through 3 levels of triggers. In the first level trigger the event definition does not distinguish between a noninteracting beam particle and a high multiplicity event. The event is a coincidence of the Target counter and one of the hodoscope counters. This trigger level provides a synchronizing strobe used for all subsequent measurements of the event defined by the leading edge of the phototube signal from the Target counter. The trigger circuit standardizes the Target counter phototube signal by requiring a minimal pulse height (using a "traditional" discriminator). The leading edge of the signal is clipped to a 2ns pulse which forms a part of the coincidence which also requires: (1) the absence of a Target counter signal for 4ns, (2) an "OR" of the hodoscope counters, (3) the absence of a VETO signal (used to disable the trigger system from the on-line computer monitor) and (4) the absence of a first level trigger for the next level trigger decision time (roughly 25ns). Both (1) and (4) above are built in deadtimes which reduce confusion and event overlap, with roughly 25% deadtime for rates of $10^7$ triggers/sec.

The signals used to form the level 2 trigger originate at the phototube bases and have the shortest propagation delay time to the trigger system. While the level 1 trigger is being formed, the signals to the other measurement systems are stored in parallel, in delay cables which terminate in the various measurement modules.

The second level trigger reduces the deadtime introduced by the digitization and buffering time of the event (roughly 1 microsecond) to an acceptably low level. This trigger level must reduce the few $10^6$ triggers/second from the level 1 trigger to a few $10^5$ events/sec readout into the buffers (including analog buffers for high precision analog measurements). The rejection is accomplished by requiring a minimum number of counters be hit, biasing the surviving events to high charged particle multiplicity. The trigger is generated by strobing saturated signals from phototube base amplifiers into coincidence latches (using level 1 trigger strobe) that drive a parallel pipeline of directly coupled logic, including counting (majority) logic.

Level 1 triggers occurring during the digitization and buffering time of the event, or following a "deadtime" trigger (which allows additional time for the detector to recover from a "messy" but rejected event, e.g. the 100ns drift chamber time) are ignored in the level 2 trigger. A master event scaler counts all level 1 triggers not ignored by the level 2 trigger. The scaler provides a means of prescaling the level 2 trigger (and above) insuring that events taken with relaxed trigger conditions will be available for trigger studies, normalization, etc.

The data area read into buffers as a result of the completion of the digitization of the event. The data are compressed upon readout, only non-zero channels are buffered. The data paths are parallel: 8 chamber, 1 phototube and 1 trigger systems and are read at 1 16-bit data word every 75ns, giving an aggregate bandwidth of 250 MByte/sec into the 10 parallel buffers. An average event size is 1kByte.

The buffers isolate the level 1 and 2 triggers from the level 3 trigger as long as the buffers do not fill, that is as long as the event rate into the
level 3 trigger pipeline does not exceed the pipeline's capacity or the
capacity of the ultimate event storage. Level 3 triggers can, accordingly, be
arbitrarily complicated without effecting the deadtime of the level 1 and 2
triggers. A prompt reset decision from the level 3 trigger can stop the
buffering operation and reduce the readout deadtime to a value intermediate
between the tens of nanoseconds of the level 1 and 2 triggers and the
microsecond digitization and readout time (the reset is not currently
implemented).

The level 3 trigger is formed using the event's digitized data. Once
the event is in the trigger pipeline, a wide range of flexible triggers can be
set. Among the various trigger decisions that can be made in the pipeline,
all or part of the event data can be dropped, or the event can be routed
around tedious calculations, etc. The decisions can reduce the subsequent
storage and processing requirements in the trigger pipeline. Triggers early
in the pipeline based on nonrecursive calculations (e.g. drift chamber
multiplicity) can provide additional time for extremely recursive calculations
(e.g. track reconstruction) by reducing the number of events flowing through
the pipeline. The level 3 trigger utilizes the Hardware Processor to
calculate and execute the trigger decisions.

Hardware Processor

Central to the design considerations of the apparatus and the data
acquisition and trigger architecture was the hardware processor. This device
was designed to be a collection of flexibly configurable and programmable
electronic modules capable of executing a complex algorithm in real time. A
number of simple algorithms have been implemented using the hardware processor
as a real time trigger. The processor has also been used in an off-line mode
to reconstruct the data collected during the various BNL data runs.

The hardware processor is a data driven, parallel pipelined,
distributed memory, synchronous device. The various electronic modules are
connected to each other and to the input and output buffers by high speed
buses. Each of the modules perform a specific operation on the data. The
data contain the routing and computing information required by the modules to
perform operations. The algorithm "executed" by the processor is defined by
the network of buses and operators. Once the processor is initialized no
external computer intervention is required to drive the computation.

The data are passed from register to register on each system clock.
Operations are performed on the data "between" registers depending on the
operator type, program and the data type. The execution of an operation
depends on the presence of data and on a place to put the data. If the data
cannot be transferred to the next register, then the operator holds the
upstream data flow. The algorithm is subdivided into subprocessors (or
subroutines) which are separated by memory buffers. These buffers decouple
one subprocess from another, keeping the data flowing through each of the
subprocessors by providing a "reservoir" for the data flow. Event data
required by the various parts of the processor and subprocessor is stored
where needed. This results in redundant information storage but eliminates
the problems arbitrating among subprocessors for use of a central storage
resource.
Every register, counter and memory location in the processor is accessible through a special control bus. Thus, the state of the processor can be uniquely determined at any time and the next-cycle-state of the processor can be predicted. All operations take place from cycle-to-cycle, independent of the cycle period. The access to and predictability of the processor can be used as a powerful diagnostic tools for debugging a processor algorithm and determining processor performance.

The implementation of an algorithm in the processor is analogous to coding the algorithm in assembler language. A network which contains the necessary operators and interconnections is laid out. The operations must specify not only the arithmetic transformation of the data but also the transformation of control information accompanying the data. The algorithm implementation (referred to as a "configuration") is not unique, but is an optimization of many factors among which are: operator utilization efficiency, required computation speed, cost, power dissipation, and physical realizability to name a few. The FNAL E690 collaboration has embarked on a program to create tools to ease in the creation, implementation and debugging of hardware processor algorithms.

The Performance of a Track Reconstruction Algorithm

BNL E766 used the hardware processor on-line during 2 data taking periods in 1985 and 1986. The track reconstruction algorithm was implemented and the $10^9$ events (with average track multiplicities of 7) from the two run periods were reconstructed in 6 weeks during the summer of 1987.

On-line Performance

The Hardware Processor was used to provide several simple triggers based on the number of hit clusters in the spectrometer systems (including the upstream beam spectrometer during the BNL proton run). During another BNL run a 4 chamber track finder was used to calculate the approximate total momentum of the event in each view of the drift chamber system.

The algorithm used to calculate the number of hit clusters in the spectrometer is nonrecursive. The drift chamber data entered modules designed to count the number of clusters (a hit cluster is defined as a group of adjacent wire "hits" in a drift chamber plane) in each drift chamber plane. There were eventually 7 such modules, one for each drift chamber plane plus one for the beam chamber spectrometer, the cluster counting proceeds in parallel. The end of data to a module (a special word makes this condition) causes the module to produce a 16-bit word containing the cluster counts for the 3 least populated planes.

One word from each of the modules and a summary of the level 2 trigger are then used by another type of module to produce a trigger. The trigger is programmable, during the various BNL data runs the triggers included: charged particle multiplicity, where events were rejected based on consistent numbers of clusters in the drift chambers; prescale, based on the event number; number of beam particles, a count of the multiplicity of the beam spectrometers. These triggers do not add deadtime to the system; the calculations are done as the event data is transferred from one buffer level to the next (50ns per 16-bit word, typically 5 to 10 words per drift chamber plane). The trigger decision is available a few clock cycles after the data transfer is complete.
(10 clock cycles at 50ns/cycle). The level 3 trigger information is summarized and merged into the event data.

The multiplicity triggers reject events which, when reconstructed, would not have the particular charged particle multiplicity of interest. These triggers have a typical rejection of 100 events per trigger, for multiplicities below 8 or 9 charged particles (depending on the beam particle type). Analysis of the data off-line, and calculations of acceptance indicate that the multiplicity triggers rejected roughly 56\% of the heavy particle events compared with 94\% for all level 2 triggers.\textsuperscript{2,3} These triggers reduce the event flow rate through the remaining pipeline, providing more time per event for calculations.

**Offline Performance**

Hardware processors are useful for offline computations of the type typically done at large computer centers. The BNL E766 acquisition system was software configurable to route data to the hardware processor either from the detector or from tape drives. This allowed the processor to be used to reconstruct data already collected during previous running periods.

A block diagram of the BNL E766 hardware processor is shown in Figure 3. Each block represents a set of electronics modules, each line a data bus. Data enters parallel memory buffers at the top of the data stream from either the detector or the data playback system. The data flow past the multiplicity logic, which uses the algorithm sketched above to trigger on specific multiplicity events. The event data are transferred into a set of "control buffers" waiting for the calculations to be completed and transfer to begin. The control buffer "tiers" separates the various subprocessors and control the flow of data through the algorithm network.

The event which passes the multiplicity triggers is transferred along to the 6-Plane Line Finder subprocessor. This subroutine recognizes line related to tracks in each of 4 views independently. These line segments are then matched in the next subprocessor, the Matcher. This subroutine matches line segments with similar sagittas in 2 of the 4 views and predicts the hit position in the other 2 views. If the hit pattern in the predicted views matches the data, the 2 line segments are combined to form a track candidate. Each eventual "real" track may have multiple track candidates. These track candidates are then fit using a linearized least squares fitting algorithm implemented in the subroutine called the Fitter. Tracks which survive minimal least-squared cuts are cleaned up and compared with other surviving track candidates. If the track parameterization is similar in 2 candidates, the candidate with the best fit parameter is kept. Thus all track candidates are compared with each other and only the best tracks are kept, eliminating duplicate tracks.

The hits which make up the track are then tagged so that they will not be used to find 4-plane tracks. The algorithm considers 2 types of 4-plane tracks: those occurring in the first 4 planes and in the last 4 planes. The control information which accompanies the data causes the control buffer tier to route the data past the 4-Plane Line Finder and back through the Matcher-Fitter-Cleanup subprocessors to find and fit the 4-plane tracks, using
the same hardware. The track type information indicating that a candidate is a 6-plane, front 4-plane of back 4-plane track modifies the operations performed in the shared hardware sequences.

At the end of the cleanup for the 4-plane tracks a trigger decision was made to pass or skip the event based on the total multiplicity, total parallel momentum and event number (for pre-scale events). Events failing the trigger were skipped, surviving events were written to tape.

**Conclusion Beauty Physics Possibilities**

Detector measurements, data acquisition and trigger rates consistent with $10^5$ events/second analyzed from $10^6$ interactions/second will be achieved shortly in FNAL E690. The extension of the data acquisition and trigger architecture to much higher rates seems straightforward. Currently available detector performance and measurement techniques form the limitations to higher rates; a large acceptance multiparticle spectrometer would have difficulty exceeding $10^7$ interactions/second.

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**References**

1) The BNL E766/FNAL E690 collaboration is:

- M. Church, B. Knapp, E. Gottschalk, W. Sippach, B. Stern, L. Wiencke
- Columbia University, Nevis Laboratories
- D. Christian, G. Gutierrez, S. Holmes, J. Strait, A. Wehmann
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Figure 1
TRIGGERING & READOUT

Max rates into level:

"event" level 1

- target counter - hodoscope "OR"
- ~ 10 signals

"interesting" event level 2

- majority logic + special counters
- ~ 100 counters

{digitize & readout - 1 μsec

readout bandwidth = \frac{10 \text{ parallel paths} \times 2 \text{ bytes}}{75 \text{ ns}} = 250 \text{ Mbytes/sec.}

typical event size = 1 kbyte}

"reconstruction event" level 3

- online event reconstruction
- ~ 10000 signals

{computation speed \geq \frac{300 \text{ registers}}{25 \text{ ns}} = 10^{10} \text{ operations/sec}

1 \text{ μsec/track candidate, multiple events, ...}}

"write tape"

\leq 10^5 \text{ events/sec}

\leq 10^7 \text{ events/sec}

\leq 10^6 \text{ events/sec}

\leq 10^3 \text{ events/sec}

Figure 2
Figure 4

10 track event reconstructed by the Hardware Processor

(trjectories and where track leaves detector)