Design of the Core 2-4 GHz Betatron Equalizer

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Abstract: *The core betatron equalizer in the Accumulator in the Antiproton Source at Fermilab needed to be upgraded. The performance could be rated as only circa 650 MHz when the system was a 2 GHz system. The old equalizer did not correct for the strong phase mismatch for the relatively strong gain of the system slightly below 2 GHz. The design corrects this phase mismatch and is relatively well matched both in and out of band.*

I. Introduction

The core betatron 2-4 GHz stochastic cooling systems in the Accumulator at the Antiproton Source at Fermilab were not performing as required. Instead of the goal 2 GHz bandwidth, the system bandwidth could best be described as only having 670 MHz[1]. A snapshot from the "new" network analyzer page (P131) is shown in Fig. 1. Figure 1 shows that just below the frequency point of 2 GHz, the gain of the system is still relatively strong and the phase not near zero. Because the phase of Fig. 1 is not near zero for the strong magnitude near 2 GHz, the system bandwidth suffers needlessly. The measurement of Figure 1 has contained within it, or embedded within it, an existing equalizer fabricated here at Fermilab. This equalizer data had to be extracted from the measurement data depicted in Fig. 1 in order to obtain the true 2-4 GHz core betatron cooling system response.

After the data was extracted of the embedded "old" equalizer, the "new" equalizer was designed, built, and installed. The final data will be presented and shown that the system with the new equalizer has roughly twice the bandwidth of the original system.

II. Design Considerations

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[1]The system bandwidth is for a general system F(ω) is $\dfrac{\int_a^b d\omega \, \mathrm{Re}(F(\omega))}{Max\{F(\omega); a \le \omega \le b\}}$.
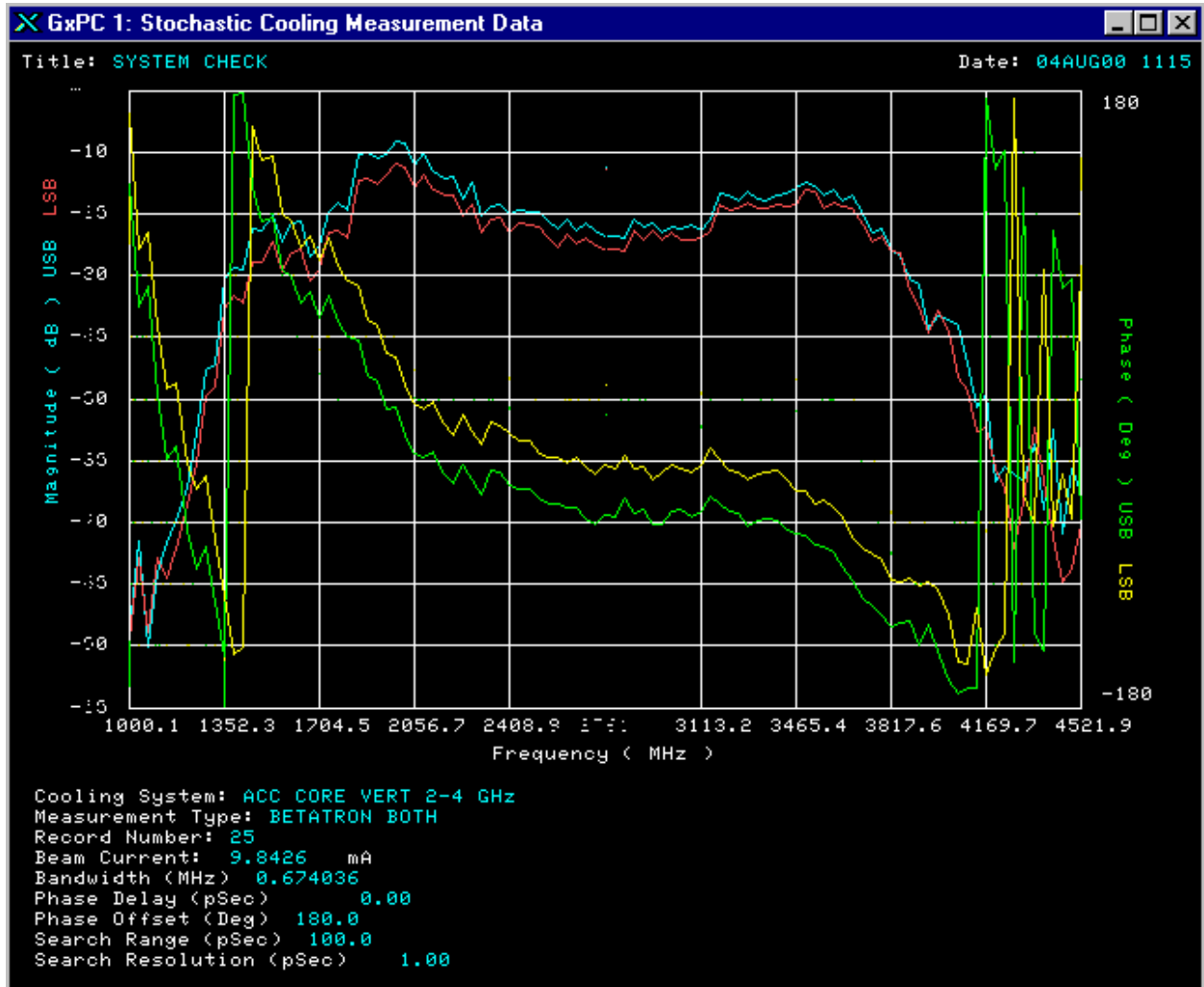
Figure 1. Picture from the P131 network analyzer page. This picture shows the response of the core 2-4 betatron stochastic cooling system. The bandwidth is 674 MHz. Magnitude fluctuations of 5dB were observed. The phase was wildly out of control just below the bandwidth of the system where there was still significant system gain.

The system design criteria of the equalizer included to maximize the broadband system response, to have a short group delay through the equalizer, and to have as high of an insertion loss as close to 0 dB as possible for S/N consideration. The equalizer was designed to have circa 10 nsec. This was adjusted for by cutting a cable in the 2-4 core cooling rack. Two options stood out for designing the topology of the equalizer. I could have chosen either using an FIR technique [1] or a more traditional microwave technique of using stubs. I decided to use the
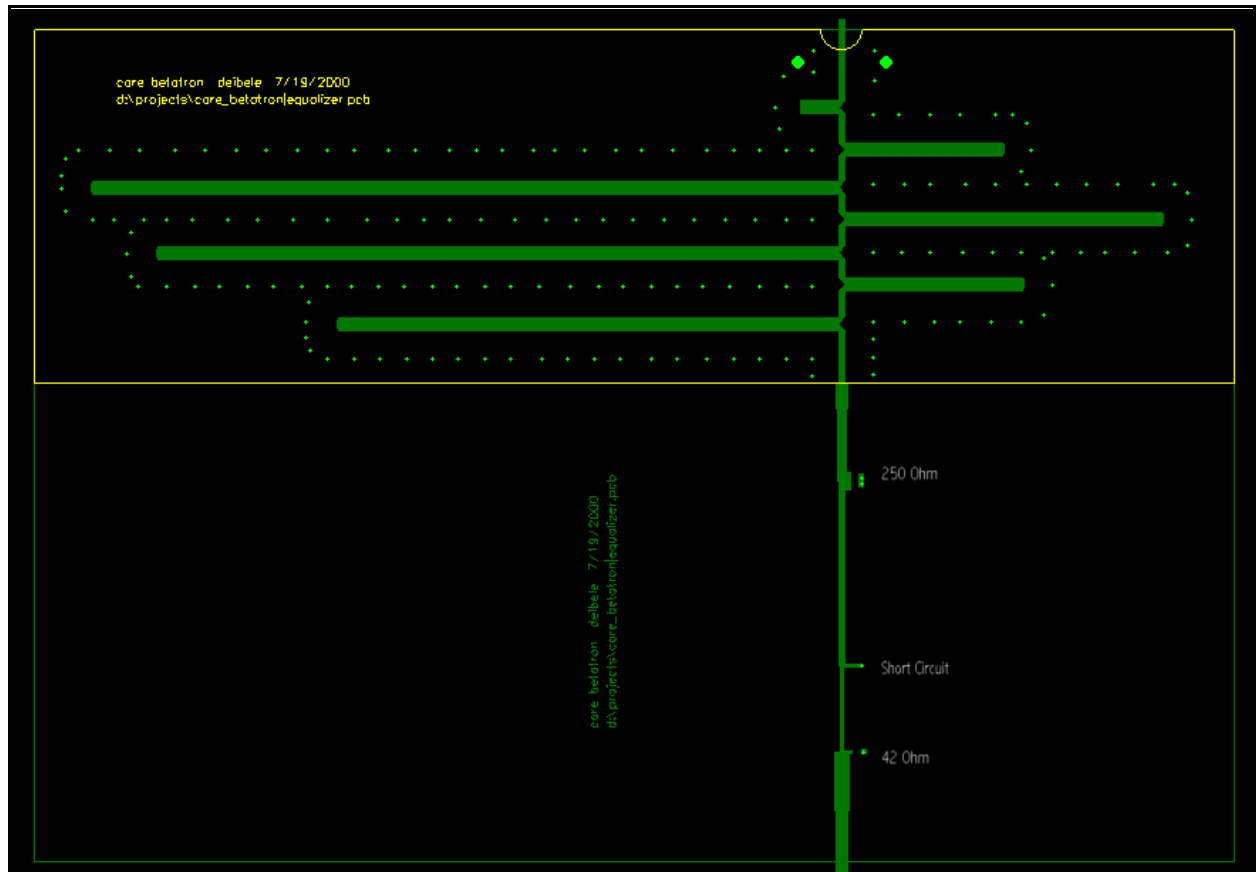
Figure 2. This is the layout designed for the core 2-4 GHz equalizer. The bottom half is configured for microstrip. The microstrip portion does the major brunt of amplitude equalization and is designed such that it has a good broadband match. Two resistors are used, a 42Ω and a 250Ω. The top half of the board is stripline and does broadband phase equalization. The coupling is on the order of -11dB in each Schiffmann phase shifter, and each coupled line is edge coupled.

traditional technique of using stubs to find the optimum magnitude equalization and to use

Schiffman phase shifters [2] to optimize the phase response. I used Agilent Technologies

Touchstone Series IV to optimize the design.

The design needed to have a low reflection coefficient and this required that the design

use resistors. This design criteria was discovered upon examining the components in the system

design and reflected energy due to the equalizer would not be tolerated. To enhance the

reflection measurement of this board, two 3dB attenuators were used to further enhance the better-than-12dB reflection coefficient measured.
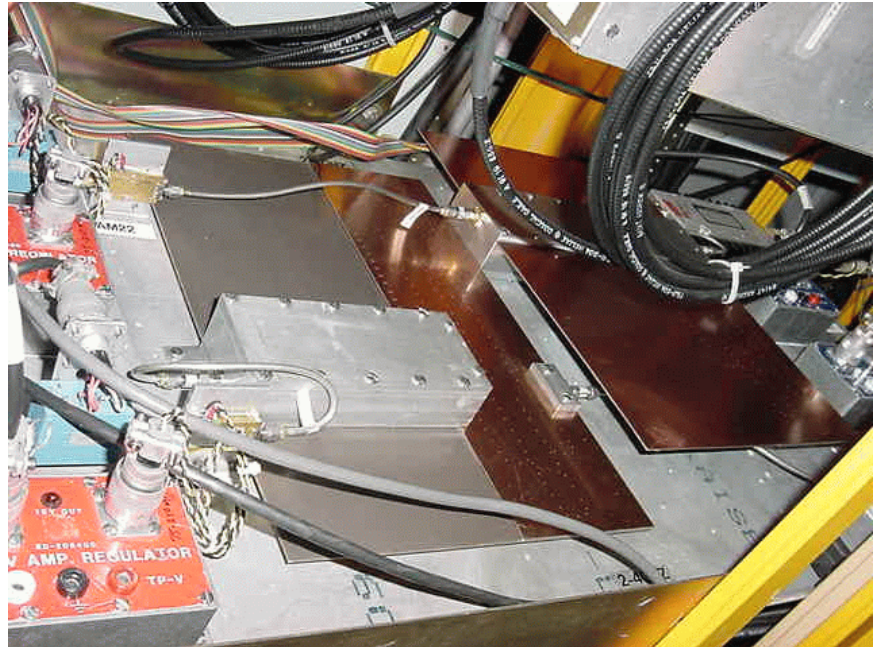
The topology of the equalizer was a hybrid of microstrip and stripline. The microstrip section was chosen to do the dominant magnitude matching and some broadband phase

Figure 3. This is a picture of the plate where the equalizers are installed in the tunnel. One can see both the vertical and the horizontal equalizers. The microstrip section is contained within the aluminum box, while the stripline is exposed to the environment. A coating was sprayed onto the copper to lengthen its lifetime before copper corrosion from the environment. Please see [3] for specifics of the mechanical drawings of the microstrip box.
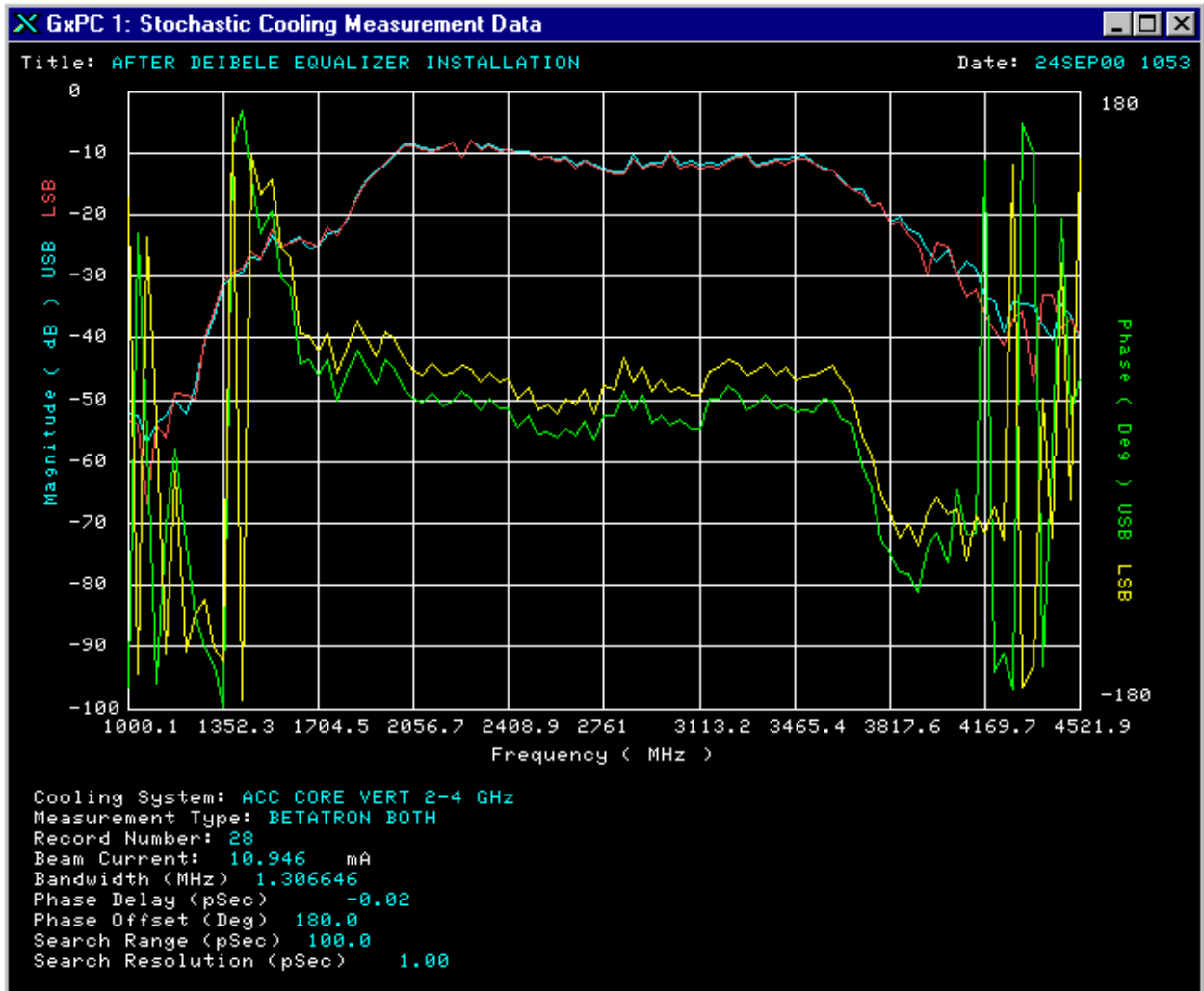
matching while the stripline did the major work of phase equalization. A picture of the layout is shown in Fig. 2.

Each Schiffmann phase shifter in Fig. 2 had to be individually tailored for this application and this resulted in long calculation times using Ansoft's Ensemble program. Each phase shifter had to be optimized for minimum reflection for the system to work in concert with the other six independent phase shifters. Each phase shifter required around one week of simulation and optimization on my IBM Thinkpad notebook computer.

This was an aggressive design since the topology had a microstrip to stripline interface while having seven phase shifters. I had to adjust my design to account for the dielectric losses

Figure 4. The system response after the installation of the equalizer. The bandwidth of the system grew to 1.307 GHz compared to the original bandwidth of 674 MHz. The magnitude of the response is now flattened as compared to the original response of Fig. 1.

incurred within the stripline portion of the circuit card. A picture of the installed equalizer can be seen in Fig. 3. Figure 3 was taken in the tunnel in the rack of the core betatron cooling. The specific mechanical drawings for the design of the boxes can be found at [3]. The design of the launch onto the microstrip was optimized for low reflection. This optimization was experimentally found by using several different microstrip box heights, box wall widths, and launch aperture radii. The drawings in [3] show the results of some experimental verification for

launching onto the Arlon material. It was experimentally determined that the wall thickness from coax to microstrip should be minimized, and the aperture should be as large as possible. For this application, the wall thickness at the coax/microstrip interface was 100 mils, and the semicircular aperture at the coax/microstrip interface had a diameter of 350 mils.

In Fig. 3, one can see both vertical and horizontal cooling equalizers, they are installed as mirror images of each other. The aluminum box contains the microstrip portion of the circuit while the stripline is exposed to the environment. A protective spray was placed upon the copper to protect it from oxidation and corrosion from the environment of the tunnel.

The physical size of the equalizer was not appealing because it was difficult to install into the existing system. The system had to be disassembled, the microwave "plumbing" had to be reworked to accommodate the size of these equalizers. Pete Seifrid and Wes Mueller did an extraordinary job in their installation and rework of the system layout.

A picture of the system response after installation is shown in Fig. 4. The calculated bandwidth of the new system with the new equalizer is shown to be better than 1.3 GHz, so the overall improvement is on the order of a factor of 2 better in bandwidth.

III. Conclusion

The design and implementation of the equalizer for the core 2-4 GHz betatron stochastic cooling system was realized using a hybrid of microstrip and stripline. The bandwidth was improved by a factor of around 2 and is now about 1.3 GHz. The equalizers have been installed and measured with the results being satisfactory.

expertise of installation.

Bibliography

[1] C. Deibele, "Synthesis of Bandpass Filters and Equalizers using Microwave FIR Techniques," Pbar Note #643.

[2] C. Deibele, "Design of the 2-4 GHz Equalizers for the Antiproton Accumulator Stacktail System," Pbar Note #622.

[3] Chris Ader, Mechanical Support - FNAL drawing #'s: 8035-MB-375875, 8035-MC-375873, and 8035-MB-375873.