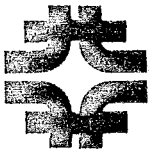

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FERMILAB-TM-2711-AD

MAIN RING LOW LEVEL RF

WRITE-UP

PART II: MRRF TIMING

Rod Gerig

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MAIN RING RF TIMING

The subject which is dealt with in this write-up is the timing at main ring RF. However, since this is intended to be a part of an overall discussion on the low level system it is appropriate to make mention of how the components which comprise the timing serve the low level system.

Referring to the low level system block diagram, the timing components are seen to be the 'Main Ring RF Timing Controller' and the 'Universal Logic Chassis Card.' The timing information that is required by the low level system is seen to be in the form of four pulses which are sent to the GATE GENERATOR module (see forthcoming write-up of this module for description of its functions) and one gate which is used by the GATE AND FAN OUT DRIVER. Since the advent of the curves MAC there is also some timing information which is independent of the Timing Controller. Through the curves MAC and its associated pulse generator card, pulses at specified energies are available; and it is one of these pulses that is used for transition time. This pulse is used by the GATE GENERATOR module. Through these two sources the low level system receives all the timing information it needs.

I will now discuss the components which on the block diagram are labeled MAIN RING RF TIMING CONTROLLER and the UNIVERSAL LOGIC CHASSIS CARD.

These units are instrumental in deriving the pulses and gates which control the RF systems. An additional service which is provided by the timing controller is that the WATCHDOG system uses it to turn off the RF in event of a failure.

The timing controller contains a clock. It is selectable to either 5 kHz or 10 kHz and it presently runs at 5 kHz. Any reference to this clock will be in MCP (Main Ring Clock Pulses). This clock needs to be referenced to the rest of the accelerator, and two signals are used to do so. The first is the T_{ϕ} pulse, which is derived from the MR Phase Reversal Clock and is used to reset the clock. The second reference source is the booster clock which is sent to main ring RF. Any reference to this pulse train will be in BCP (Booster Clock Pulses).

From these two sources, Main Ring Reset and the Booster Clock, the necessary synchronization is obtained. There are four timing channels calibrated to the Booster Clock. These are called Injector Timing Channels (ITC) and are in units of Booster Clock Pulses. There are 16 timing channels synchronized to Main Ring Reset. These are known as Main Ring Timing Channels (MRTC) and are in Main Ring Clock Pulses. From these timing channels four gates are derived. Also contained in the timing controller are three special purpose timing registers which record the count of the Main Ring Clock counter at various times.

As a first step in understanding the MRRF timing each of the ITC's, MRTC's, GATES and registers will be individually discussed.

ITC1 - This timing channel also has the name BEX1. Its purpose is to provide a pulse that indicates beam is coming to main ring. It does so by providing a pulse after the first 8-GAP from booster, after a T_{ϕ} pulse. The amount of time after the 8-GAP until the BEX1 pulse is controllable through the main ring 530 with a parameter called BEX1 (units are BCP).

In other words if BEX1 is set for 35080, the BEX1 pulse on ITC1 will occur 35080 Booster Clock Pulses after the first 8-GAP that has occurred since the last T_{ϕ} pulse (main ring reset). This pulse is used to generate some of the other pulses discribed below and is sent out to the gate generator module.

ITC2 - Also called BEX. This provides pulses similar to BEX1 except that it does so on every 8-GAP. Thus, during normal main ring operation there will be 13 pulses on ITC2 per main ring cycle. It is available as a scope trigger at the RF building.

ITC3 - This channel is also known as EBEX1. Its only known use is in scope triggering. Its value will be that of BEX1 minus an offset that can be entered on the bottom of subpage 2, page 18 on the Main Ring X530. If a negative number is entered on page 18, EBEX1 will be set to 1. Therefore EBEX1 will normally occur at the same time, or shortly before BEX1. It is therefore known as Early BEX1.

ITC4 - This timing channel is a spare although it can be controlled from subpage 2, page 18 of the 530 where it is called a general purpose trigger.

MAIN RING TIMING CHANNELS

MRTC1 - RFON: This pulse is used to start the RF and DC gates. It is generated in such a way so that when the number of booster pulses changes or booster pulses are shifted a cycle earlier or later, the RF on time will change automatically. To do so the timing controller monitors the BEX1 pulse (ITC1) and records this time in MCP in a special purpose register.

This therefore is merely BEX1 time in main ring clock pulses and is called BEX1M. The RFON pulse is derived from the value in the BEX1M register plus a value entered by an operator through the 530 called NRFON (nominal RFON). In addition there is a software offset of 41 MCP programmed into the system. The final value of this pulse, which is then displayed on the 530 CCI as RFON is:

$$\text{RFON (MCP)} = \text{BEX1M (MCP)} - 41 \text{ MCP} + \text{NRFON (MCP)}$$

This timing channel is used internally by the timing controller in the formation of the RF and DC gates, which will be described later.

MRTC2 - RFOFF: This timing channel is used in the formation of the RF and DC gates to turn the RF off. Its value is determined directly by an operator through the main ring 530.

MRTC3 - SCPTRG: This timing channel is used to trigger the scope at the RF building. Its derivation is similar to MRTC1 in that it is referenced to BEX1M. It can be offset by changing NSCTRG on the MR530, and the actual time will then be displayed as SCPTRG.

$$\text{SCPTRG} = \text{BEX1M (MCP)} - 46 \text{ MCP} + \text{NSCTRG (MCP)}$$

MRTC4 - ACCSW: This pulse is used by the gate generator module in the formation of the injection gate and the Radial Position Enable gate. It is originated by an operator through the main ring 530.

MRTC5 - Not used at the present time. In older documentation it was called RVRTRG.

MRTC6 - SCPINT: Supplies a pulse for intensified scope trigger. Entered directly through MR530.

MRTC7 - MACINT: This pulse is shipped directly back to the MAC where it queues interrupt level 2 for sampling the MRRF MADC. It also is entered directly through MR530.

MRTC8 - This timing channel is not used at this time. In older documentation it was called ATSMPL.

MRTC9 - PDP8GO: Presently used as the start time for the PDP8 memory feedback.

MRTC10 - PRFON: This timing channel is used to turn the RF on when a past pulse is injected into main ring. The value of PRFON is entered directly through the X530. The pulse sent out on this timing channel is hardware OR'd with MRTC1 so that either timing channel can control the GATES.

MRTC11 - PRFOFF: This is the past pulse RF off timing channel. It is hardware OR'd with MRTC2 so that either timing channel is capable of turning the RF off.

MRTC12: SDON: Super damper on time.

MRTC13: SDOFF: Super damper off time.

MRTC14 - BDON: Beam dampers on time.

MRTC15 - BDOFF: Beam dampers off time.

See appendix for update list.

MRTCM - This is the manual channel in that it can be locally changed at the RF building without putting the timing controller into manual. It's available on the front panel of the timing controller for general purposes.

TIMING REGISTERS

BEX1M - This register contains the number of Main Ring Clock pulses that have occurred between clock reset time (the $T_{\emptyset}$ pulse from the utility crate below the HLU and the BEX1 pulse on ITC1.

MAXCP - The contents of this register is the number of clock pulses that occur between $T_{\emptyset}$'s (Main Ring Resets). This register cannot contain a number greater than 65535, which is 13.107 seconds when the clock rate is 5 kHz. Should the main ring cycle time exceed 13.107 seconds this register will contain the value 65535 and be displayed in red on page 18 of the main ring X530. Any attempt to set a timing channel to a value greater than MAXCP will result in that timing channel being set to the value of MAXCP.

GEN INP - This register is connected to a BNC input on the front of the timing controller and contains the number of MCP between $T_{\emptyset}$ and whatever pulse is connected to the general input. At the present time the input is connected to a pulse that occurs at transition time, and this register therefore contains transition time.

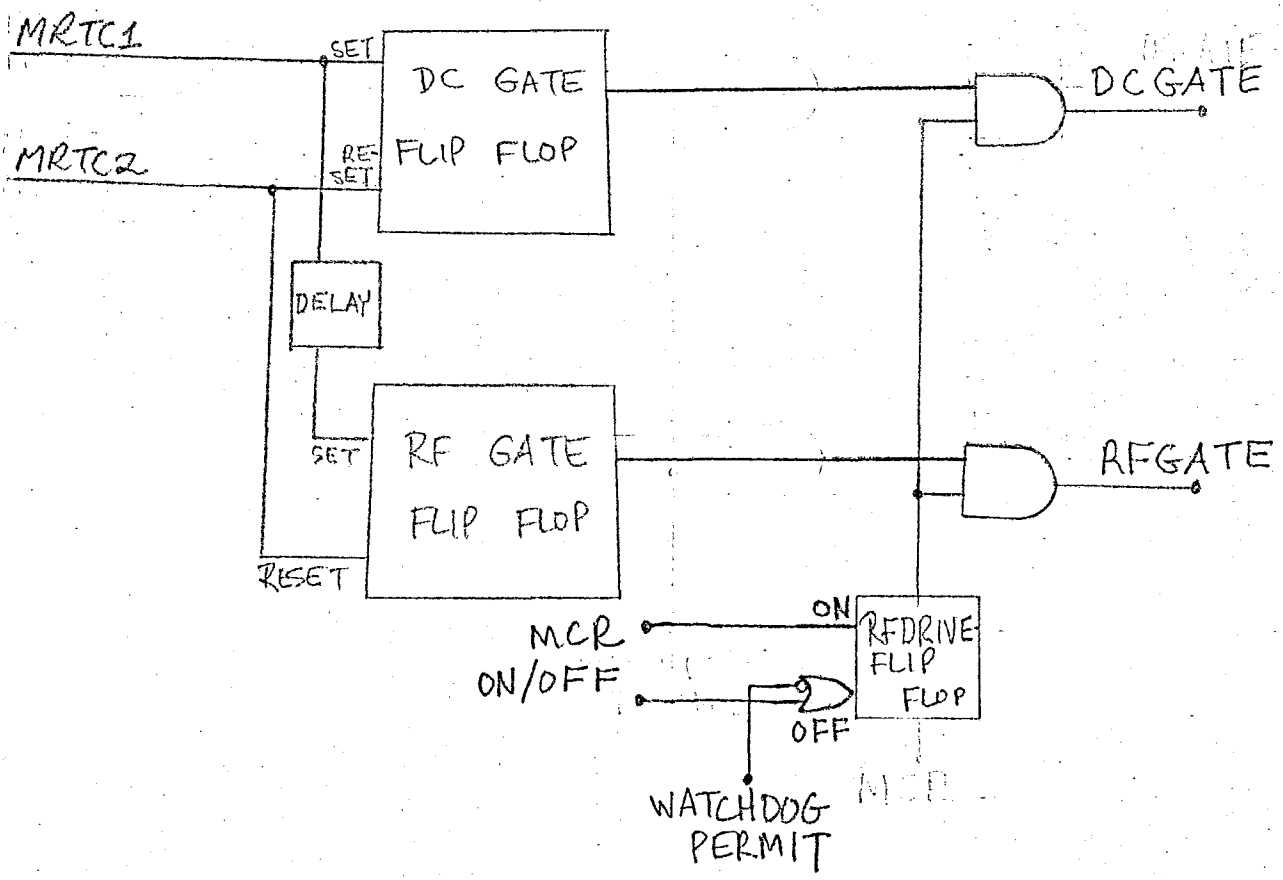
GATES

GATE 1 - DC GATE: This gate is turned on by MRTC1 and turned off by MRTC2. There are several other conditions for this gate which will be mentioned below. This gate allows the anode program to pass to the high level equipment.

GATE 2 - RF GATE: This gate is also turned on by MRTC1 and off by MRTC2. There is, however, a delay in the turn on that is controllable from 0-15 MCLK pulses (hard-wire change). It is presently set to 4 MCLK as can be seen on subpage 2, page 18, X530. An external signal is also applied to both of these gates. This is the WATCHDOG permit signal. When the WATCHDOG signal goes to a logical '∅' the gates are turned off immediately and cannot be turned on again until the WATCHDOG has been reset. In addition, both of these gates can be disabled by turning RFDRIVE on page 21, X530 to OFF.

This gate is sent to the Gate and Fan-out Driver, the low level rf systems which allows the rf signal to be sent to the individual station.

A brief schematic follows.



GATE 3 - SUPER DAMPER GATE: This gate is turned on by MRTC12 and off by MRTC13. It can be disabled on subpage 2, page 18, MR X530, and of course controls the on/off time of the Super Damper.

GATE 4 - Not used, although at one time was used to control a feature called RF SLOW OFF. It retains this nomenclature on subpage 2, page 18, MR X530 where it can be disabled.

This concludes the discussion of the basic functions of the timing controller as it pertains to the operation of the RF. One important operational feature that has not been mentioned is PHLOCK. When phase lock is turned on or off three things occur. As mentioned in PART I of the low level RF write-up, a coaxial relay closes when phase lock is turned off and sends booster a RF signal directly from the reference oscillator.

The other things that happen when phase lock is turned off concern the timing controller. Of primary importance is that ICLCK is disabled. In other words, the information from the injector timing channels (ITC's) are ignored. Therefore BEX1M will be frozen to whatever value it is when PHLOCK is turned off. The second thing that happens is that MRTC1 (RFON) and MRTC3 (SCPTRG) are released from their dependence on BEX1M and can be controlled directly through the MR X530. The gold dashes to the left of the line on page 18 will be positioned at RFON & SCPTRG when PHLOCK is off rather than at NRFON and NSCTRG when PHLOCK is on.

An additional parameter that can be controlled via page 18, MR X530 is VICD. This is the interrupt rate for PLOTM1 and PLOTM2. The timing controller queues the MRRF MAC on interrupt level 12 at the rate specified

as VICD. This is a very high priority level, and the task associated with this level takes about 80 μsec. VICD should therefore be quite a bit greater than 80 μsec or the MAC won't have time for anything else. Presently VICD is set to 300 μsec.

UNIVERSAL LOGIC CHASSIS

The UNIVERSAL LOGIC CHASSIS (ULC) has various functions depending on the needs of the rf system. The function which concerns us here is the Gate Enable Card.

The timing system operated as previously described for some time, however, in order to provide some protection the Gate Enable Card was added. The Gate Enable Card receives several inputs: The DC gate, the RF gate, MRTC1, MRTC2 and the T_{ϕ} pulse from the timing controller just described and the WATCHDOG permit from the WATCHDOG crate.

Recall that the DCGATE and RF GATE can be turned on at any point during the cycle by an operator. In the timing controller this changes the state of a flip-flop causing the gate to go high immediately which would turn the rf systems on. One of the functions of the ULC is to prevent the rf from being turned on in the middle of the cycle. The other function is to provide a crash off capability by either the WATCHDOG crate or the next T_{ϕ} pulse.

In the following drawing and timing chart the gates from the timing controller previously called DCGATE & RFGATE are referred to as GATE1 and GATE2, respectively, to differentiate them from the output gates of the ULC.

APPENDIX

One of the problems with a write-up such as this is that things change so quickly. Already the write-up as it stands is incorrect. However, I intended it to be a description of how the timing works and not an exact documentation of timing channels and gates.

This documentation already exists. Bob Ducar keeps a notebook in the Main Control Room called RF SYSTEM OPERATIONS MANUAL in which the timing channels and gates are listed. This notebook is updated regularly and I suggest it be looked at regularly also. (The list of timing channels occurs near the end of the section called ASSIGNMENT SHEETS.) Also included in the notebook are other write-ups including one on the timing which can be used in conjunction with this write-up.

To bring this paper up to date I note the following changes:

MRTC5	RVTON/Start Phase Revert	used for rf debunching during slow spill
MRTC8	RVTOFF/End of Phase Revert	
Gate 4	Phase Revert Gate	
MRTC10	spare	
MRTC11	spare	

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ENGINEERING NOTE

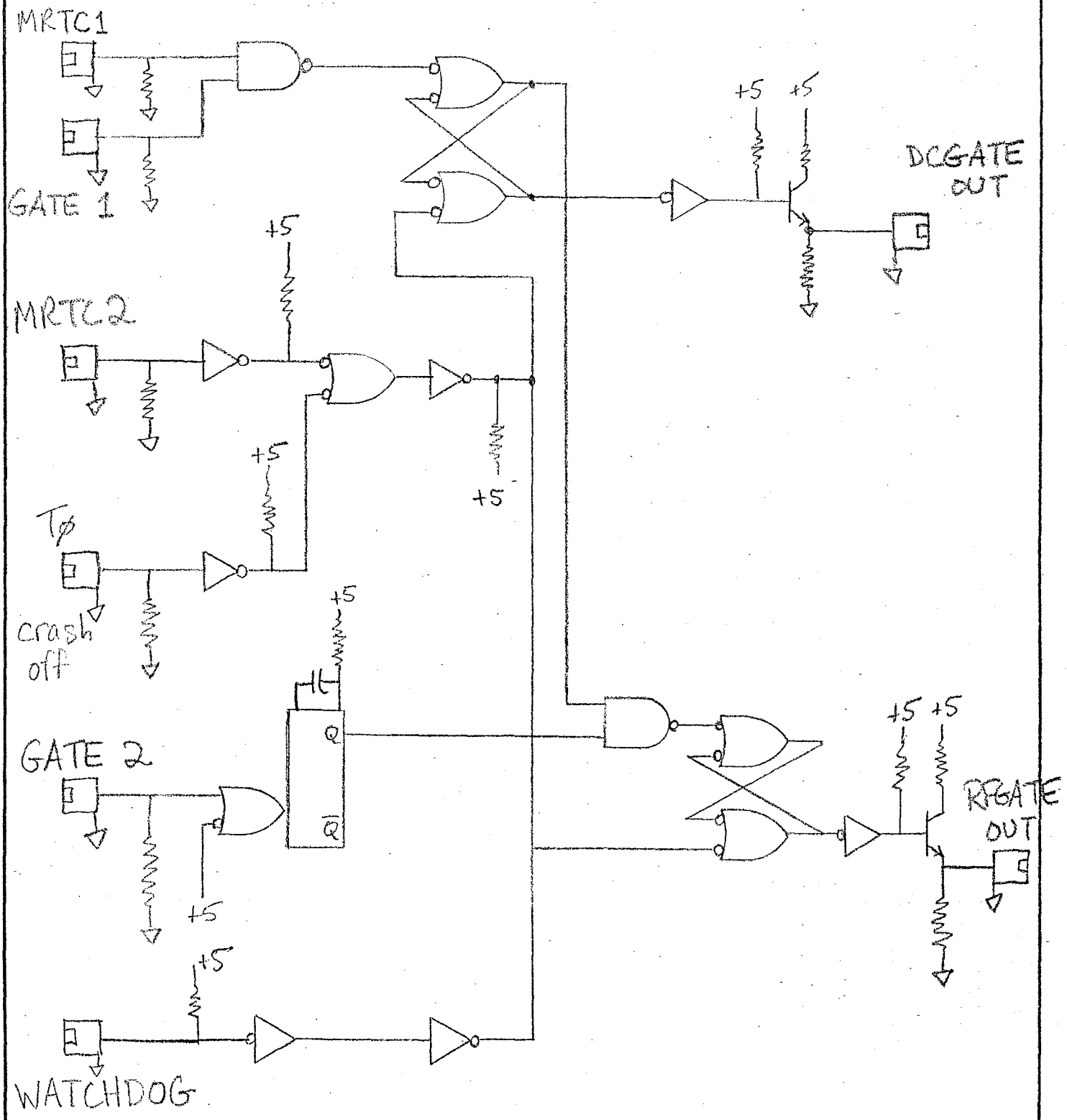
SECTION	PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT

UNIVERSAL LOGIC CHASSIS GATE ENABLE CARD

NAME

DATE	REVISION DATE



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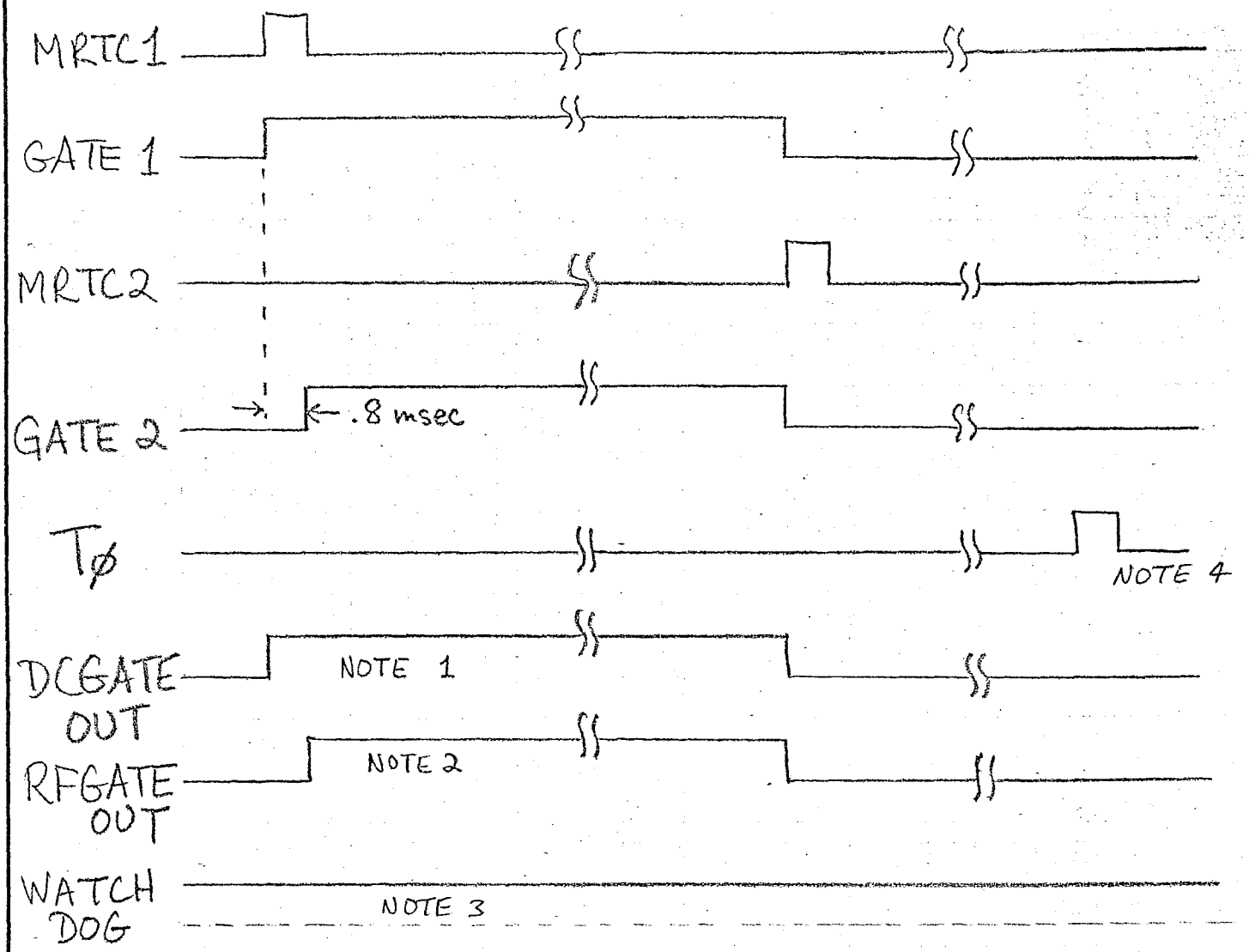

1) IF GATE1 IS HIGH DURING MRTC1, START DCGATE OUT

2) IF DCGATE OUT IS HIGH AT LEADING EDGE OF GATE2, START RFGATE OUT

3) WATCHDOG MUST BE HIGH TO ENABLE GATES, IF WATCHDOG GOES LOW DURING NORMAL CYCLE GATES GO OFF IMMEDIATELY.

4) Tø IS A CRASH OFF TO TURN GATES OFF IF MRTC2 IS SET ABOVE MAXIMUM CLOCK COUNT OR LESS THAN MRTC1.

08/04/76 1501

18 MAIN RING RF TIMING -- PAGE 1

-BEX1	FIRST BOOSTER EXTRACT	35080	BCP
BEX1M	FIRST BOOSTER EXTRACT	13.1	SEC
NRFON	RFON - NOMINAL.....	0	MCP
-RFON	RF ON TIME.....	.598	SEC
-RFOFF	RF OFF TIME.....	4.458	SEC
-ACCSW	END BATCH INJ & RST..	1.416	SEC
-MRTC10	SPARE TIMING CHANNEL.	12.45	SEC
-MRTC11	SPARE TIMING CHANNEL.	.105	SEC
-RVTON	START PHASE REVERT...	4.477	SEC
NSCTRG	SCPTRG - NOMINAL.....	0	MCP
-SCPTRG	RF SCOPE TRIGGER.....	.377	SEC
-SCPINT	SCOPE INTENSIFIER....	.6	SEC
-MACINT	MADC SCAN INTRPT TIME	3	SEC
-VICD	PLOTTING INTRPT RATE.	300	BCP
MAXCP	MAX NO. OF CP/CYCLE..	13.1	SEC
MCR	MAIN RING CLOCK RATE.	5	KHZ

-RF ON ... -PHLOCK .. OFF
-SPARE .. OFF

SAVE TIME: 07/19/76 0147
RESTORE TIME/PREVIEW TIME PAGE 2

08/04/76 1502

18 MAIN RING RF TIMING -- PAGE 2

-PDP8GO	PDP-8 START TIME.....	1.404	SEC
-RVTOFF	END OF PHASE REVERT..	6.672	SEC
-ITC4	GEN PURPOSE TRIGGER..	5000	BCP
-SDON	SUPER DAMPER ON	.2	SEC
-SDOFF	SUPER DAMPER OFF	4.45	SEC
-BDON	BEAM DAMPER ON.....	.2	SEC
-BDOFF	BEAM DAMPER OFF.....	6.5	SEC
TRT	TRANSITION (GEN INP).	1.628	SEC

TIMING CONTROLLER MODE	AUTO
DC & RF GATE PERMIT (WATCHDOG)	ENABLE
GATE 1 - DC GATE	ON
GATE 2 - RF GATE	ON
-GATE 3 - SUPER DAMPER GATE	.. OFF
-GATE 4 - PHASE REVERT	.. OFF
DC ON TO RF ON DELAY TIME	4 MCP
MCLK FREQUENCY (.2/.1 MS PER CP)	5 KHZ
MCLK PRESENCE	ON
5/26 VOLT POWER	ON

-EBEX1 TO BEX1 DELAY: 0 BCP #PAGE 1