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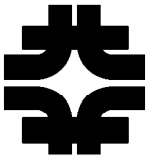

Fermi National Accelerator Laboratory

D-Zero Detector Electronics
Run II b Upgrade Project

VME LVDS SERDES Buffer (VLSB)
Module Specification

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1 Introduction

This document specifies the D0 VME64 LVDS SERDES Buffer (D0 VLSB). TheD0 VLSB is part of the electronics of the D-Zero Central Tracker Trigger Test System at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page:
http://www.fnal.gov/

More information on the D0 Detector is available on:
http://www-d0.fnal.gov/

The designers welcome suggestions and corrections [Ref.], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page:
http://www-ese.fnal.gov/

More information and documentation on the D0 VME LVDS SERDES Buffer Project are available on:
http://www-ese.fnal.gov/D0 VLSB/

2 Overview

The D0 VME64 LVDS SERDES Buffer (D0 VLSB) is a VME64 [Ref.] single wide 6U module used for testing the Analog Front-End boards system [Ref.]. The module is a custom LVDS SERDES Buffer with 4 LVDS inputs channels and can be operated stand-alone with minimal additional hardware.

The current testing needs require only a 4 channel D0 VLSB module but the design allows system expansion to multiple modules.

A D0 VLSB module can receive/generate trigger signals over two Lemo© [Ref.] connectors on the module front panel.

A normal test system configuration consist of a VME 64 subrack were slot 1 is occupied by a VME subrack controller and the D0 VLSB cards will occupy one or more of the remaining slots.

3 VLSB card and system

3.1 Interfaces

The VLSB module supports the following interfaces:

Backplane Interface

VME bus

Used for remote access (readout, controls and diagnostic). The VME [Ref.] interface conforms to VME64 (VITA 1.1 - 1997) standard.

Power supply

A VLSB module is powered through the backplane connection to the subrack 5 Volt power supply. For stand-alone operations a VLSB module can be powered through an auxiliary connector. Each VLSB module has its own over-current/over-voltage protection.

Trigger interface

The trigger interface is implemented with two Lemo© [Ref.] connectors and controlled by the Module Controller FPGA.

JTAG (IEEE 1149.1) interface

A four pin Test Access Port (TAP) provides access to the module card JTAG chain. The JTAG port is used for module FPGAs/EEPROMs configuration, diagnostic, and boundary scan.

Serial (RS232) interface

A connector provides access to the RS232 interface. The RS232 interface provides an additional access to the VLSB module logic for monitoring and debugging. The RS232 interface can be used for the VLSB module standalone operation removing the need of a VME subrack and VME controller.

Logic Analyzer interface

For debugging/diagnostic purposes, the VLSB module has several connectors to fit the high-density adapter cables for Agilent 16550A logic analyzers.

Module-to-module interface

A front panel connector provides a mean to synchronize the operation of multiple modules.

3.2 How the VLSB fits into the testing of the AFE System

The main purpose of the VLSB is to test the AFE cards/system. Figure 3.1 briefly describes the AFE data flow on an AFE card. The VLSB will be used to receive and store the data transmitted by the AFE over the LVDS links. The VLSB will not be a part of the D0 CTT system but will be used only to verify performance and functionality of the AFE cards in a separate test environment.

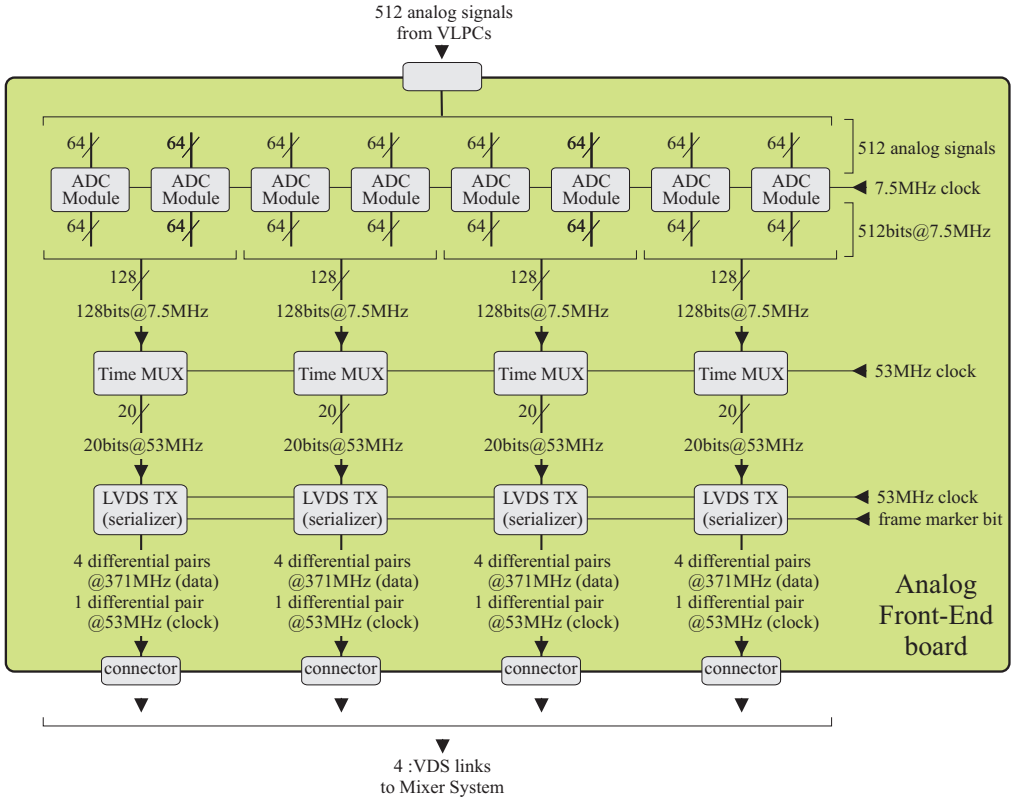

Figure 3.1, AFE board data flow

3.2.1 VLSB single card system

A VLSB module can be operated in standalone mode. In this mode the card can be positioned on a bench or in a 6U VME subrack. The VLSB module can be controlled from a PC using the RS-232 interface. In standalone operation the VLSB module is powered through an on-board connector by an external 5 Volt power supply or by the 6U VME subrack 5 Volt power supply.

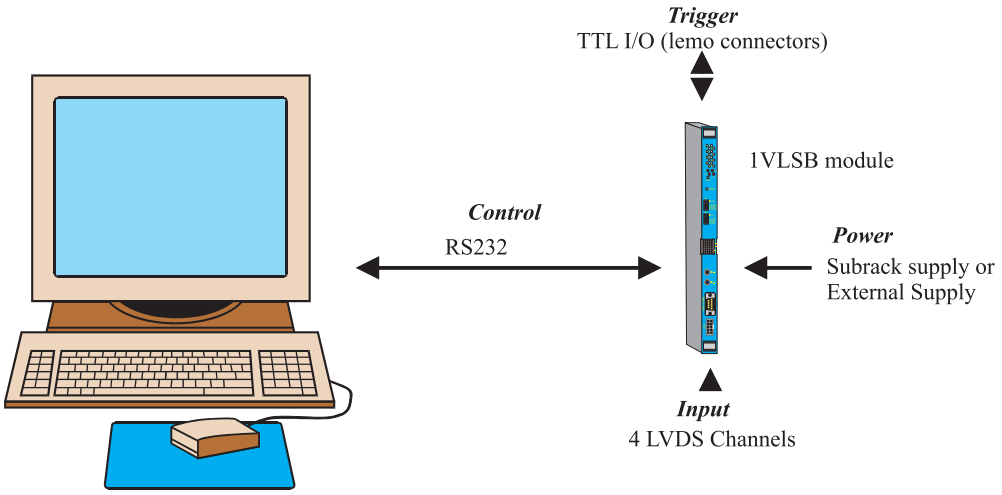

Figure 3.2, VLSB single card system.

3.2.2 VLSB multiple-cards system

The VLSB standalone system can be expanded to a set of several cards hosted by a 6U VME64X subrack. In this case, the cards can be individually accessed though their RS-232 interfaces. A set of four module can be synchronized through the use of the front panel board-to-board connectors. All cards in the system can be accessed through a VME subrack controller that can be hosted in the subrack slot 1. This controller can provide the VLSB cards with additional interfaces to the outside world (Ethernet, MIL-STD 1553, ...).

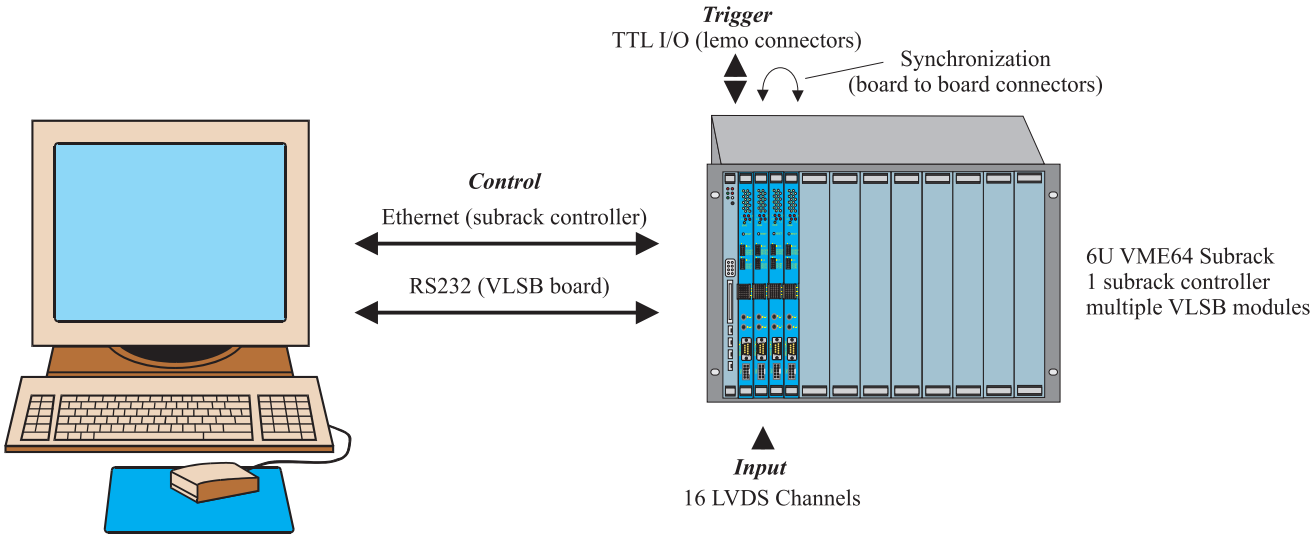

Figure 3.3, VLSB multiple cards system.

3.3 VLSB card block diagram

Figure 3.4 provides a block diagram of a VLSB module.

The module can be controlled through two different interfaces: RS-232 (front panel) and VME (backplane).

The VLSB module hosts the "Module Controller FPGA" which handles the VME and RS232 interfaces, the timing and the diagnostics and supervise the data flow operations. The FPGA is configured at power-up by two on-board EEPROMs.

The VLSB module also hosts the four LVDS SERDES receivers used to convert and de-serialize the input LVDS signals to Low Voltage TTL. A logic analyzer pod is provided for each LVDS link.

The Module Controller FPGA manages the input LVDS interface and stores the data received into the ZBT SRAM. The FPGA control/status registers and the ZBT SRAM content can be accessed from both VME an RS232 interfaces.

A JTAG connector provides access to the VLSB module's FPGAs and its configuration EEPROMs.

If external timing (LVDS input links) is not available a 53MHz oscillator provides the Module Controller FPGA with a time reference.

Front panel LEDs provide real-time diagnostic allowing access to board status and setting information.

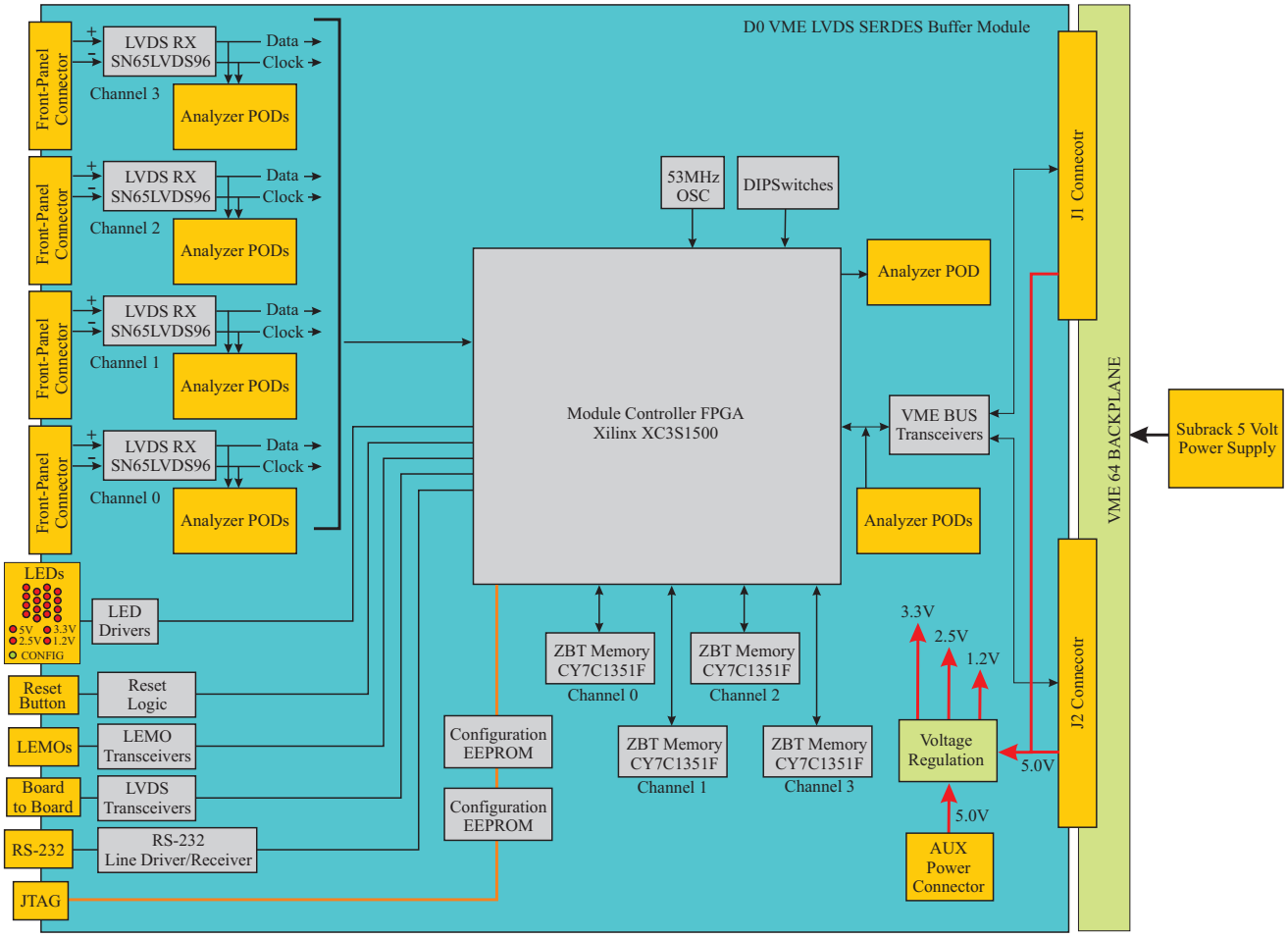

Figure 3.4, VLSB Card block diagram

4 Interfaces

4.1 Backplane Interface

The VLSB card complies with the VME64 (VITA 1.1-1997) electrical and mechanical standard. The subrack used is 6U high by 160mm deep.

The VME64 standard and the 6U form factor were chosen to make the module compatible with the existing subracks.

The implementation of the VME64 standard utilizes two 160-pin connectors, J1/P1 and J2/P2. Backplane interface pinouts are provided in Appendix A.

Each slot in a VME64 Subrack is uniquely identified by the 6 bits address provided in Table 4.2. The address bits are hardwired into the backplane (Geographical Addressing) using 6 bits (GAP* and GAP4:GA0*) allowing each board to be addressed by is location in the subrack. The GAP* (Geographical Address Parity) signal is not used on the VLSB Module.

When the VLSB Module detects a standard VME backplane, it automatically uses the on board dip switches 5:1 as board address.

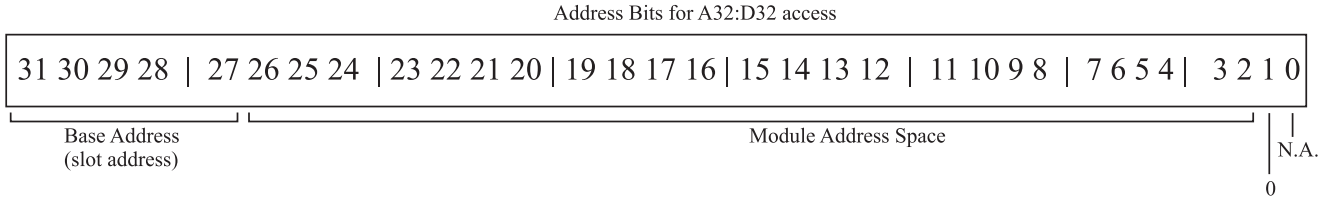

Figure 4.1, Address bits.

Access Type	Address Modifier	Function	DS1*	DS0*	LWORD*	A01
A32:D32	0x09 0x0A 0x0D 0x0E	Extended non privileged data access Extended non privileged program access Extended supervisory data access Extended supervisory program access	0	0	0	0
A32:D32	0x0B 0x0F	Extended non privileged block transfer Extended supervisory block transfer	0	0	0	0
A24:D16	0x39 0x3A 0x3D 0x3E	Standard non privileged data access Standard non privileged program access Standard supervisory data access Standard supervisory program access	0	0	1	0 (data 15:0) 1 (data 31:16)

Table 4.1, Type of Accesses recognized by the VLSB Module

Slot #	GP*	GA*(4:0)	Base Address (Hex)	Slot MODULE_ID	DIP Switches (8:4)	Notes
--	1	b11111	Set by switches(8:4)	b00000		Legacy backplane (non VME64)
1	1	b11110	n/a	n/a	-	Subrack Controller slot.
2	1	b11101	10	b00010	b00010	VME 64
3	0	b11100	18	b00011	b00011	VME 64
4	1	b11011	20	b00100	b00100	VME 64
5	0	b11010	28	b00101	b00101	VME 64
6	0	b11001	30	b00110	b00110	VME 64
7	1	b11000	38	b00111	b00111	VME 64
8	1	b10111	40	b01000	b01000	VME 64
9	0	b10110	48	b01001	b01001	VME 64
10	0	b10101	50	b01010	b01010	VME 64
11	1	b10100	58	b01011	b01011	VME 64
12	0	b10011	60	b01100	b01100	VME 64
13	1	b10010	68	b01101	b01101	VME 64
14	1	b10001	70	b01110	b01110	VME 64
15	0	b10000	78	b01111	b01111	VME 64
16	1	b01111	80	b10000	b10000	VME 64
17	0	b01110	88	b10001	b10001	VME 64
18	0	b01101	90	b10010	b10010	VME 64
19	1	b01100	98	b10011	b10011	VME 64
20	0	b01011	A0	b10100	b10100	VME 64
21	1	b01010	A8	b10101	b10101	VME 64

Table 4.2, Subrack slot geographical addressing (VME 64)

DIP Switches (8:4) (Module_ID)	Base Address (hex)	DIP Switches (8:4) (Module_ID)	Base Address (hex)
b00000	00	b10000	80
b00001	08	b10001	88
b00010	10	b10010	90
b00011	18	b10011	98
b00100	20	b10100	A0
b00101	28	b10101	A8
b00110	30	b10110	B0
b00111	38	b10111	B8
b01000	40	b11000	C0
b01001	48	b11001	C8
b01010	50	b11010	D0
b01011	58	b11011	D8
b01100	60	b11100	E0
b01101	68	b11101	E8
b01110	70	b11110	F0
b01111	78	b11111	F8

Table 4.3, Subrack module addressing (VME)

4.1.1 Data Space Description

Address (hex)	
From 00 00 00 00 00 00 00 04 00 00 00 08 00 00 00 0C 00 00 00 10 ● To 00 00 00 3C	Module Status/Control registers (4 bit addressing, 16 locations)
From 00 00 00 40 To 00 FF FF FC	Not Used
From 01 00 00 00 To 01 07 FF FC	Memory Bank 0 128k deep (17 bit addressing, 131072 locations)
From 01 08 00 00 To 01 0F FF FF	Not Used
From 01 10 00 00 To 01 17 FF FC	Memory Bank 1 128k deep (17 bit addressing, 131072 locations)
From 01 18 00 00 To 01 1F FF FF	Not Used
From 01 20 00 00 To 01 27 FF FC	Memory Bank 2 128k deep (17 bit addressing, 131072 locations)
From 01 28 00 00 To 01 2F FF FF	Not Used
From 01 30 00 00 To 01 37 FF FC	Memory Bank 3 128k deep (17 bit addressing, 131072 locations)
From 01 38 00 00 To 07 FF FF FC	Not Used

Table 4.4, Data Space Address Map

The VLSB Module provides 16 32-bit wide register locations in data space as described in the following subsections. Some register locations of the data space are not currently implemented. Table 4.5 shows the module data space address map.

Register	Access	Register address (27 bits)
(0) Board Status/Control register	Read/Write	hex 0000000
(1)	Read/Write	hex 0000004
(2)	Read/Write	hex 0000008
(3)	Read/Write	hex 000000C
(4) Input Links Error Status register	Read	hex 0000010
(5) Memory Banks start address	Read/Write	hex 0000014
(6) Memory Banks end address	Read/Write	hex 0000018
(7) Trigger Data Word	Read/Write	hex 000001C
(8) Trigger Data Mask	Read/Write	hex 0000020
(9) Trigger Control register	Read/Write	hex 0000024
(10) Module Information register	Read	hex 0000028
(11) LED Control register	Read/Write	hex 000002C
(12) MMode Data register	Read/Write	hex 0000030
(13) Monitoring Status register	Read	hex 0000034
(14) Monitoring Status History register	Read	hex 0000038
(15)	Read/Write	hex 000003C

Table 4.5, Module Registers Address Map.

4.1.2 Memory Data Word

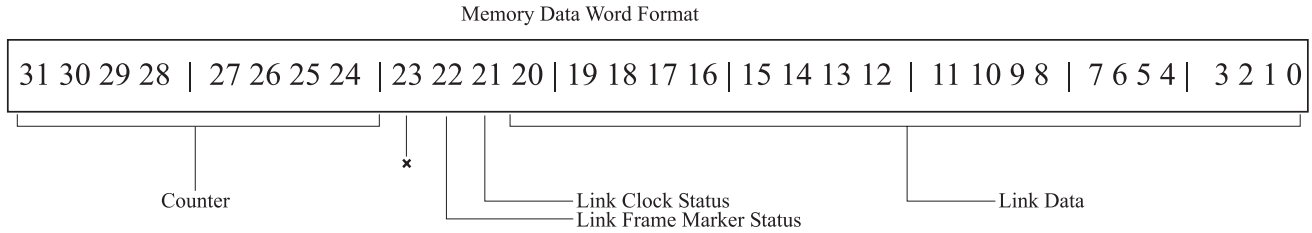

Figure 4.2, Memory Data Word Format

Bit#	Name (Type)	Interpretation
31..24	counter	8 bit counter
23	--	--
22	Link Frame Marker Status	Link Frame Marker Status, '1' if en error is detected in the frame marker bit (data stream LSb).
21	Link Clock Status	Link Clock Status, '1' if an error is detected in the link clock (frequency out of range)
20..0	Link Data	Link Data Stream

Table 4.6, Memory Data Word

4.1.2.1 Memory Bank Start Address register (5)

Relative address 0x0000014 (27 bits) is the Memory Bank Start Address register, a read/write register. This register is used to set the start address for the memory bank address.

The address counter uses this 17-bit value as initial address when a trigger is received.

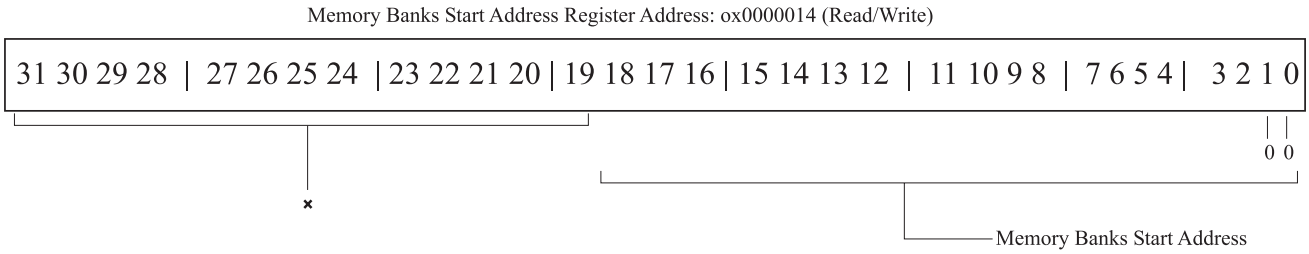

Figure 4.3, Memory Bank Start Address Register

Bit#	Name (Type)	Interpretation
31..19	--	--
18..0	Memory Bank Start Address	Memory bank start address. The two LS bits are always zero. Default register value is 0.

Table 4.7, Memory Bank Start Address Register

4.1.2.2 Memory Bank End Address register (6)

Relative address 0x0000018 (27 bits) is the Memory Bank End Address register, a read/write register. This register is used to set the end address for the memory bank address.

The address counter uses this 17-bit value as final address when a trigger is received.

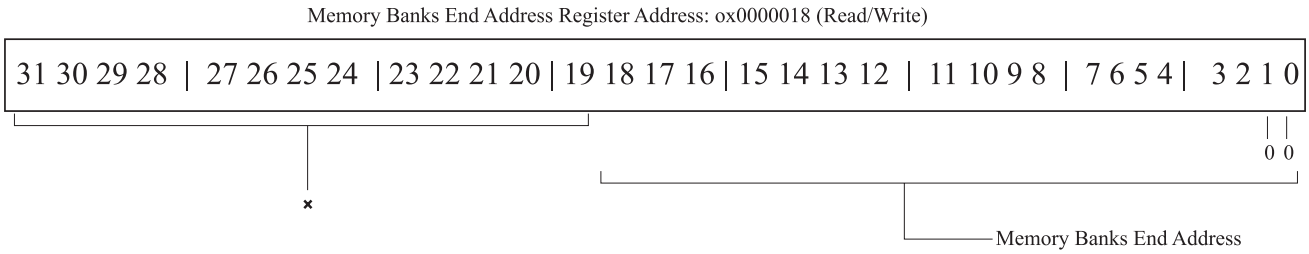

Figure 4.4, Memory Bank End Address Register

Bit#	Name (Type)	Interpretation
31..19	--	--
18..0	Memory Bank End Address	Memory bank end address. The two LS bits are always zero. Default Register Value is 7FFFC.

Table 4.8, Memory Bank End Address Register

4.1.2.3 Trigger Data Word register (7)

Relative address 0x000001C (27 bits) is the Trigger Data Word register, a read/write register. This register is used to set the 21-bit word used to generate the data trigger. A data trigger is generated when the following statements are true:

1) The board is operating in triggered mode.
2) The Data Trigger is enabled (Trigger Control Register)
3) The Data Trigger generation is enabled on at least one of the input links.
4) The Trigger Data Word is received on the link/s enabled to generate a data trigger.

The Trigger Data Mask register allows the user to set which bits in the trigger data word should be used to generate a trigger. By default all bits are used.

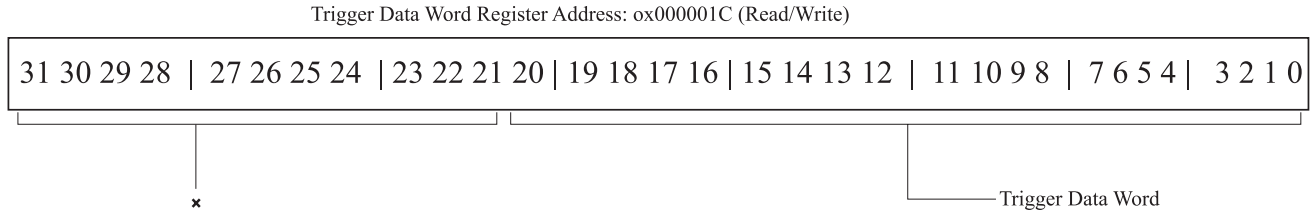

Figure 4.5, Trigger Data Word Register

Bit#	Name (Type)	Interpretation
31..21	--	--
20..0	Trigger Data Word	21-bit word used to generate the Data Trigger.

Table 4.9, Trigger Data Word Register

4.1.2.4 Trigger Data Mask register (8)

Relative address 0x0000020 (27 bits) is the Trigger Data Mask register, a read/write register. This register allows the user to set which bits from the trigger data word register should be used to generate a trigger. The default content of the register is 001FFFFF (all bits are used).

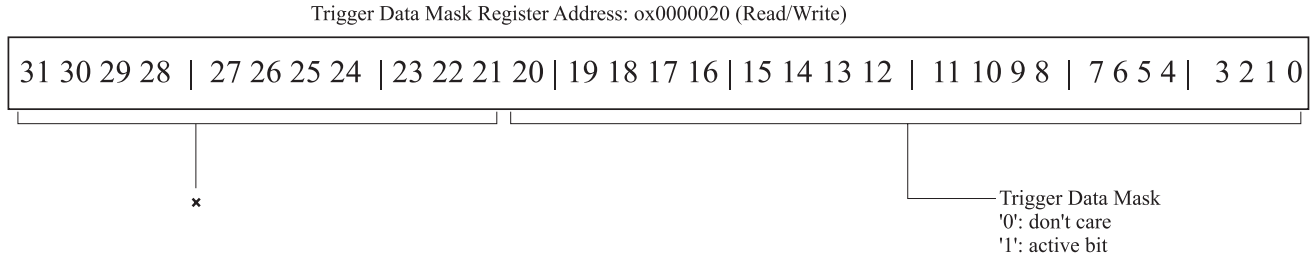

Figure 4.6, Trigger Data Mask Register

Bit#	Name (Type)	Interpretation
31..21	--	--
20..0	Trigger Data Mask	21-bit data word mask used to generate the Data Trigger. '0': don't care bit. '1': active bit.

Table 4.10, Trigger Data Mask Register

4.1.2.5 Trigger Control register (9)

Relative address 0x0000024 (27 bits) is the Trigger Control register, a read write register. This register controls the trigger signals for the input links FIFOs.

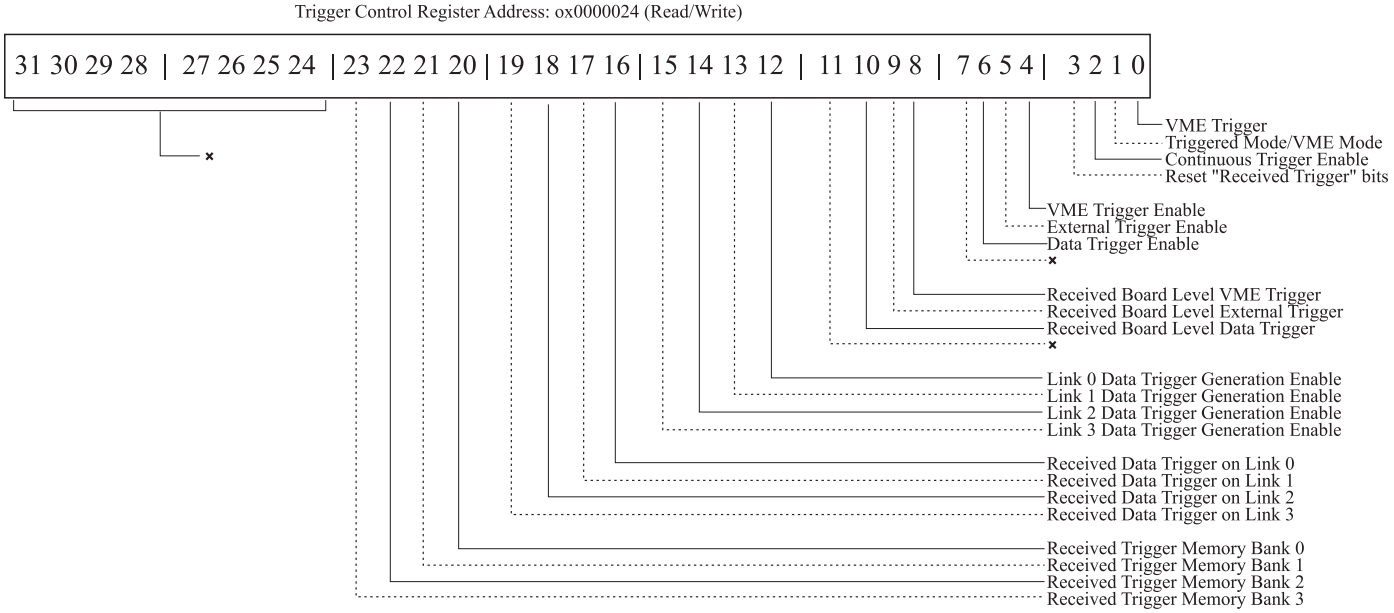

Figure 4.7, Trigger Control Register

Bit#	Name (Type)	Interpretation
31..24	--	--
23..20	Memory Banks received triggers	Memory Banks received triggers bit 23: Memory Bank 3 bit 22: Memory Bank 2 bit 21: Memory Bank 1 bit 20: Memory Bank 0
19..16	Input Links received data triggers	Input links received data triggers bit 19: Link 3 bit 18: Link 2 bit 17: Link 1 bit 16: Link 0
15..12	Links Data Trigger generation enables	Links data trigger generation enables bit 15: Link 3 enable bit 14: Link 2 enable bit 13: Link 1 enable bit 12: Link 0 enable
11..8	Received triggers	Module received triggers bit 19: -- bit 18: Received Data Trigger bit 17: Received External trigger bit 16: Received VME Trigger
7	--	--
6	Data Trigger Enable	Enables data stream triggering.
5	External Trigger Enable	Enables external triggering.
4	VME Trigger Enable	Enables VME triggering.
3	Reset “received trigger” bits	Reset “received trigger” bits.
2	Continuous Trigger Enable	Enables Continuous Trigger generation.
1	Triggered Mode Enable	Enables Triggered Mode. Memory will store data each time it receives a trigger. VME access to memory is disabled.
0	VME Trigger	Writing a ‘1’ to this bit will generate a VME trigger signal when VME triggering is enabled. Always read-back ‘0’.

Table 4.11, Trigger Control Register

Received trigger bits are set to 1 when the trigger is enabled and a trigger has been received.

4.1.2.6 Module Information register (10)

Relative address 0x0000028 (27 bits) is the Module Information register, a read only register. This register provides the module serial number and the firmware revision date/code.

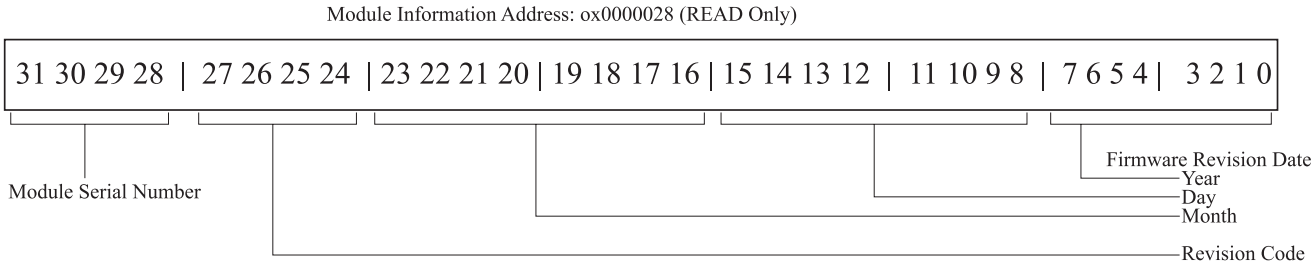

Figure 4.8, Module Information Register

Bit#	Name (Type)	Interpretation
31..28	Module Serial Number	Module serial number.
27..24	Firmware revision code	Firmware revision code.
23..16	Firmware revision month	Firmware revision date. Month in binary coded decimal (BCD).
15..8	Firmware revision day	Firmware revision date. Day in binary coded decimal (BCD).
7..0	Firmware revision year	Firmware revision date. Year in binary coded decimal (BCD).

Table 4.12, Module Information Register

4.1.2.7 LED Control register (11)

Relative address 0x000002C (27 bits) is the LED Control register, a read/write register. This register can be used to change the monitoring mode, which allows the user to select the set of signals that are driving the front panel LEDs (see Section 6.1 for a description of the monitoring modes). The status of these signals can also be remotely read by accessing the Monitoring Status register (Paragraph 4.1.2.8). Information about whether the monitored signals are changing or have changed is stored in the Monitoring Mode Status History register (Paragraph 4.1.2.9). Accessing the LED Control register in writing will reset the Monitoring Status History register. It should be noted that the monitoring mode can also be changed using the front panel reset button. Each time the button is pressed for less then two seconds, the board switches to the next LED-monitoring mode. This change is automatically reflected in the content of the Monitoring Mode register.

Each front panel LED consists of a green and a red LED in the same package. The LED latch mode feature allows latching the LED in the ON position when they get driven.

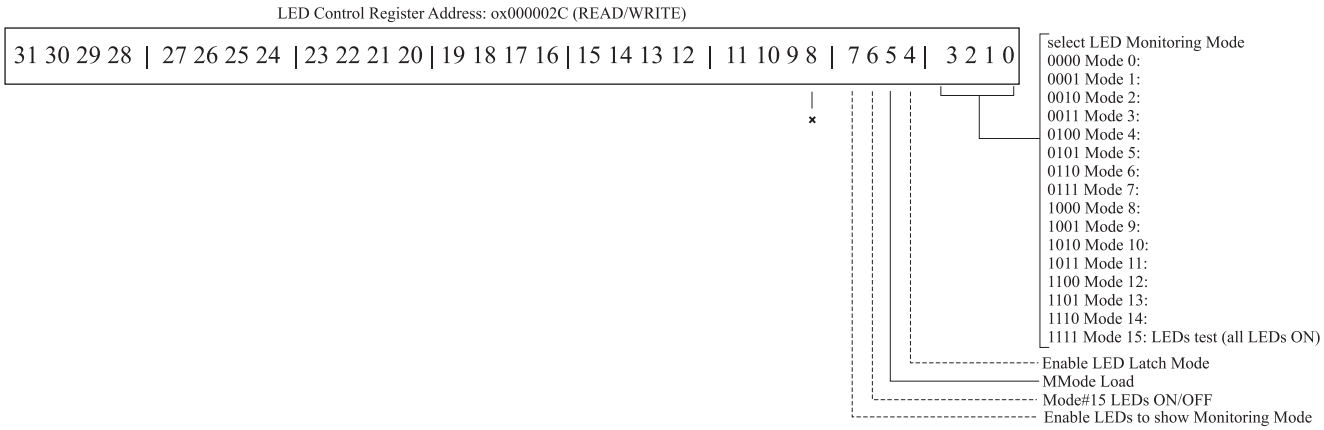

Figure 4.9, LED Control Register

Bit#	Name (Type)	Interpretation
7	--	Not used.
6	Mode 15 LEDs ON/OFF	In Monitoring Mode #15 all LEDs are on by default ('0'). When this bit is set high ('1') all the LEDs will be forced to be OFF in Monitoring Mode #15.
5	MMode	Enable MMode operations.
4	Enable LED Latch Mode	When enabled will force the LEDs (both red and green) to remain ON when they are turned ON even by a short transition. This "LED latching" is reset every time the Monitoring mode is changed (through the monitoring mode register or using the front panel reset button) or when the monitoring mode register is accessed in writing. Default is disabled ('0').
3..0	Monitoring Mode Select	Allows for selection of the monitoring mode

Table 4.13, LED Control Register

4.1.2.8 Monitoring Status register (13)

Relative address 0x0000034 (27 bits) is the Monitoring Status register. It is a read only register. This registers allows for reading of the current status of the front panel LEDs. The front panel LEDs reflect the status of different groups of signals on the mixer board depending on the current monitoring mode. The monitoring mode can be changed using the front panel reset button (pressing it for less then 2 seconds) or remotely by accessing the LED Control register. The sixteen available monitoring modes are described in Section 6.1.

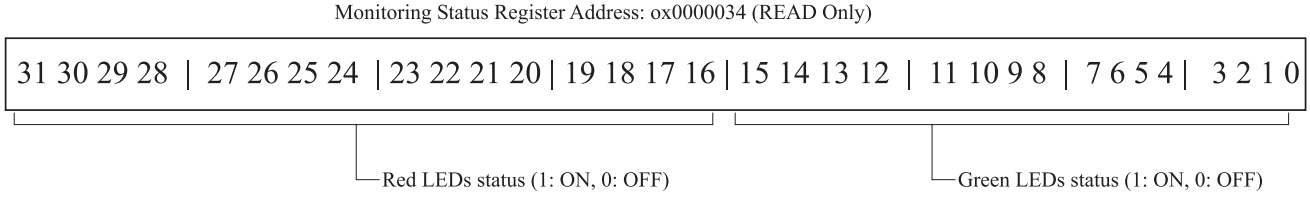

Figure 4.10, Monitoring Status Registers

Bit#	Name (Type)	Interpretation
15..0	Green LEDs #15 to #0 status	Status of the Green LEDs #15 to #0. '1': LED is ON, '0': LED is OFF.
31..16	Red LEDs #7 to #0 status	Status of the Red LEDs #7 to #0. '1': LED is ON, '0': LED is OFF.

Table 4.14, Monitoring Status Register

4.1.2.9 Monitoring Status History register

Relative address 0x0000038 (27 bits) is the Monitoring Status History register. It is a read only register. The bits in this register are set if the signal driving the corresponding LED has changed status (high to low or low to high) since the last time the registers were reset. The registers are reset each time the Monitoring Mode register is accessed in writing.

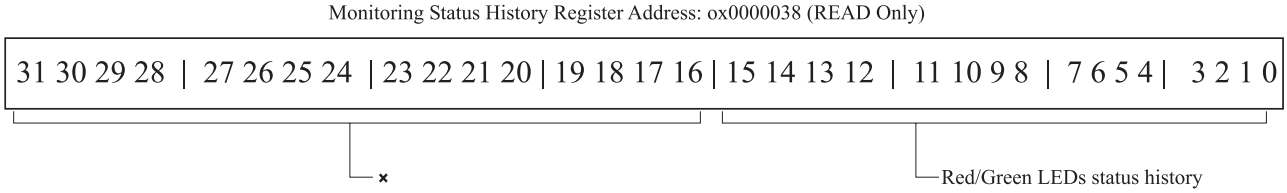

Figure 4.11, Monitoring Status History Register

Bit#	Name (Type)	Interpretation
15..0	Green/Red LEDs #15 to #0 status history	Status history of the Green LEDs. '1' means that the corresponding Green LED changed status since last reset of the register, '0' otherwise.
31..16	--	Not Used

Table 4.15, Monitoring Status History Register

4.2 Power supply

The VME64 standard defines, via the J1/P1 and the J2/P2 connectors, ten pins of +3.3V and six pins of +5V. The standard VME64 backplane connector has also 1 pin that supplies +12V, and 1 pin that provides –12V. Each pin is rated for 1.5 amps.

The VLSB module is powered only the +5V pins.

The VLSB module has also a Molex style power connector to allow for standalone operations with a +5V power supply.

The VLSB module design allows for operation in a standard VME 6U subrack.

4.3 Interface with AFE card

The VLSB module hosts 4 Low Voltage Differential Signal (LVDS) SERDES (SERializer-DESerializer) receivers (4 channels). The receiver used are the Texas Instrument [Ref.] SN65LVDS96.

The VLSB module receives the data from the AFEs on four 21 bits wide LVDS Links. The data is transmitted on these links along four differential pair (three data and one clock). The Analog Front-End board uses the Texas Instrument [Ref.] SN65LVDS95 serializes as transmitters and the VLSB module uses the SN65LVDS96 deserializers as receivers which provide the 21 outputs of 3.3 V TTL data and a clock.

The high-speed LVDS links interfacing the Analog Front End Boards with the VLSB Module use 100 Ω controlled-impedance custom parallel cables. The front panel connectors are the AMP 1-1064-1 [Ref.] which have a 50 Ω single ended (signal to ground) and an 89 Ω differential (signal to signal) impedance.

Special care was taken on the VLSB Module design to ensure that the highest signal integrity was maintained. To achieve this, the board's impedance was controlled to 50 Ω single ended and 100 Ω differential for the high-speed LVDS serial connections. The board's impedance was controlled to 50 Ω for the slower parallel data. The quantity of vias was minimized and, when necessary, placed as close as possible to the device drivers. Since this is a combined serial and parallel interface, care was taken to control both impedance and trace length mismatch (board skew) [Ref.]. All traces from the connector to the receivers are as short as possible and matched in length. The 100 Ω LVDS interconnecting media is matched with a 100 Ω termination at the inputs of the receivers.

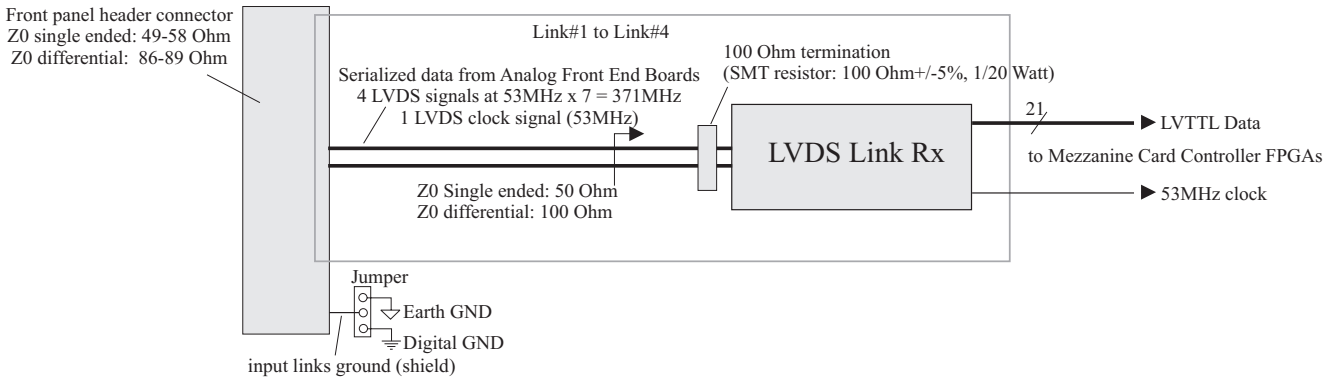

Figure 4.12, Diagram of VLSB-AFE interface

4.4 RS-232 Interface

A Universal Asynchronous Receiver/Transmitter (UART) is implemented in the VLSB Module Controller FPGA. The UART allows interfacing the card with a computer having a serial port. The VLSB design uses an Analog Devices ADM3202 as RS-232 transceiver. The card behaves like a Data Communication Equipment (DCE) with adjustable settings. The default settings are the following: BAUD rate 115200, 1 start bit, 2 stop bits, no parity and no handshake.

4.5 JTAG Interface

See a description of JTAG in Paragraph 12. One four pin Test Access Port (TAP) is provided on the VLSB module, it accesses the Module Controller FPGA and its two configuration EEPROMs.

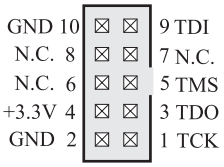

Figure 4.13, JTAG Interface

JTAG Chain		
Device #	Device Type	Notes
1	XCF04SV020	In-System-Programmable Configuration EEPROM 1.
2	XCF04SV020	In-System-Programmable Configuration EEPROM 0.
3	X3CS1500-4FG676C	Module Controller FPGA

Table 4.16, JTAG Chain Devices

4.6 Logic Analyzer Connectors

For debugging/diagnostic purposes the VLSB module has eight Amp "Mictor 38" connectors (AMP 2-767004-2) to fit the Agilent (formerly HP) High Density adapter cables (Agilent E5346A). Each adapter cable fits two test pods of an Agilent 16550A Logic Analyzer allowing monitoring up to 38 signals.

4.7 Memory Map

The Memory mapping will allow access to the Module Controller FPGA registers and Module ZBT Memory through two different interfaces, VME and RS232.

5 Module Configuration

5.1 Configuration through on-board EEPROM

At power-up the Module Controller FPGA is configured with the content of the two on-board EEPROMs. Pressing the front-panel reset button for more then 2 second will force a FPGA re-configuration.

5.2 Configuration through JTAG

For testing purposes the VLSB Module Controller FPGAs can be programmed through the JTAG interface connector. The JTAG interface is also used to update the content of the configuration EEPROMs.

6 Monitoring and diagnostic features

The VLSB design includes several diagnostic features. Beside logic analyzer connectors the user can access relevant information on module status from VME and RS232 interfaces.

6.1 LED diagnostics

The front panel accommodates 4 red LEDs and 1 green LED and sixteen bicolor LEDs numbered from 0 to 15 Figure 6.1.

The 4 red LEDs provide information about the 4 power voltages 5V (backplane) 3.3V (switching regulator), 2.5V (linear regulator), 1.2V (switching regulator).

The green LED provides status of the FPGA configuration (DONE signal).

The sixteen bicolor LEDs together with the reset push button are used by the LED diagnostic. This allows the user to view in real-time the status on module signals, registers and flags scrolling through several “monitoring modes”.

The bicolor LEDs are controlled by the FPGAs and the reset push button is used to select the set of signal to be displayed by the LEDs. At power up, the default set is set number twelve. Pushing the reset button (for less then two seconds) allows the user to select the next set. Immediately after the reset button is pushed the LEDs will indicate for about two seconds the selected set of signal that will be displayed. Pressing the reset button for more then two seconds forces the mixer board to reset.

If not specified otherwise, the LED use is as follows: green LED ON if signal is in a logic low state, red LED ON if signal is in a logic high state. Each LED is controlled by it's own state machine which stretches the signal driving the LED to a minimum of 150msec in order to make it visible to the human eye. If a signal is continuously changing both the green and red LEDs will be ON resulting in a yellow color.

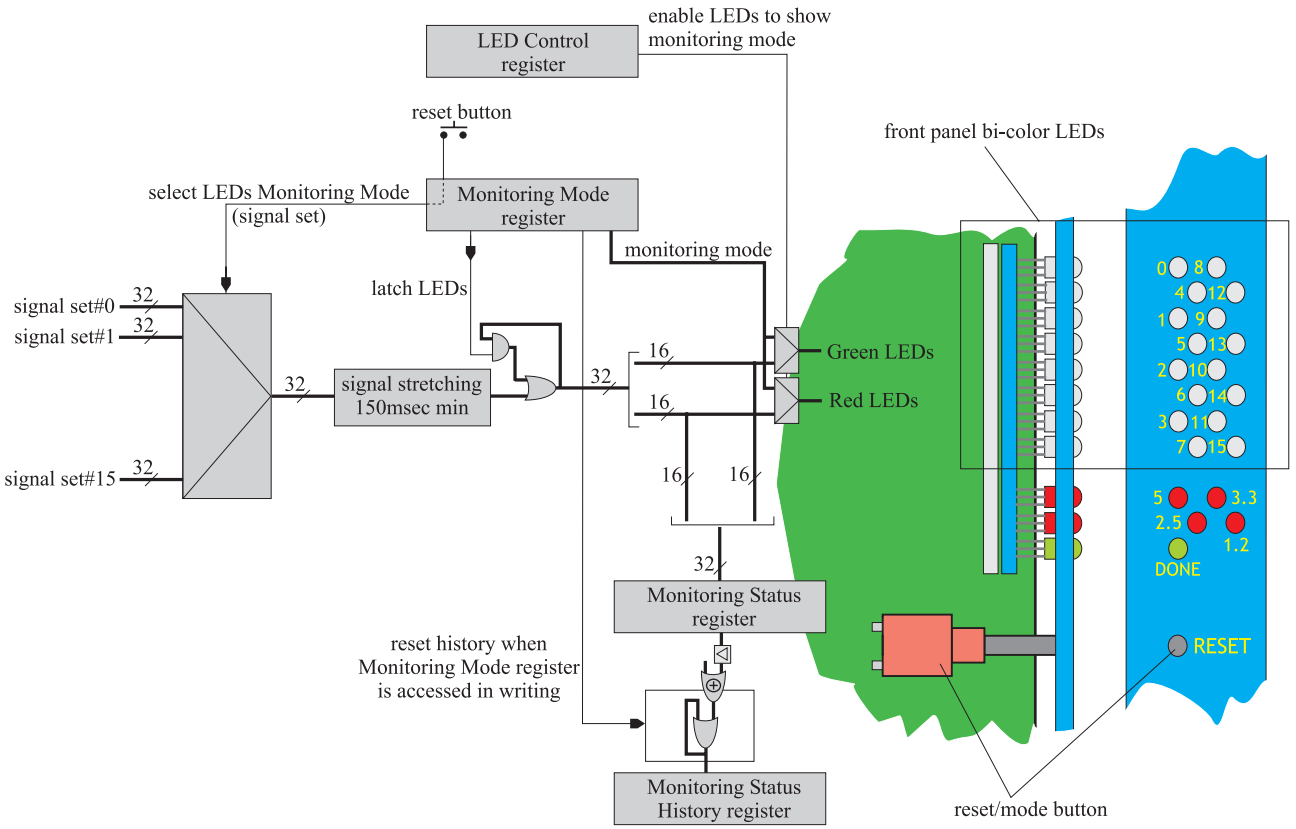

Figure 6.1, Front panel LEDs and LEDs monitoring modes

The following tables describe the sixteen available sets of signals (or monitoring modes).

LED#	
15	VME Trigger (RED LED: Trigger Enable, GREEN LED: Received Trigger)
14	External Trigger (RED LED: Trigger Enable, GREEN LED: Received Trigger)
13	Data Trigger (RED LED: Trigger Enable, GREEN LED: Received Trigger)
12	Trigger Mode. LEDs OFF: trigger mode disabled. RED LED: one shot trigger mode , GREEN LED: continuous trigger mode)
11..8	Input links data trigger (RED LED: Trigger Enable, GREEN LED: Received Trigger)
7..4	Input links frame markers
3..0	Input links clocks status

Table 6.1, LED's set #0

LED#	
15..0	

Table 6.2, LED's set #1.

LED#	
15..0	

Table 6.2, LED's set #2.

LED#	
15..0	

Table 6.3, LED's set #3.

LED#	
15..0	

Table 6.2, LED's set #4.

LED#	
15..0	

Table 6.4, LED's set #5.

LED#	
15..0	

Table 6.5, LED's set #6.

LED#	
15..0	

Table 6.6, LED's set #7.

LED#	
15..0	

Table 6.7, LED's set #8.

LED#	This set is used to monitor the VME Address least significative 16 bits
15..0	VME_ADDRESS(15..0)

Table 6.8, LED's set #9.

LED#	This set is used to monitor the VME Address most significative 16 bits
0..15	VME_ADDRESS(31..16)

Table 6.5, LED's set #10.

LED#	This set is used to monitor the VME Data least significative 16 bits
15..0	VME_DATA(15..0)

Table 6.5, LED's set #11.

LED#	This set is used to monitor the VME Data most significative 16 bits
15..0	VME_DATA(31..16)

Table 6.6, LED's set #12.

LED#	This set is used to monitor the several VMEbus signals
5..0	VME_AM(5..0). VMEbus address modifiers.
6	*VME_AS. VMEbus Address Strobe (active low).
7	*VME_LongWord. VMEbus Long Word (active low).
9..8	*VDS1, *VDS0. VMEbus Address Strobes (active low).
10	*VBCLR
11	*VBBSY
12	*VWRITE
13	*VME_DTACK
14	*VME_BERR
15	SYSCLK

Table 6.7, LED's set #13.

LED#	This set is used to monitor the several VMEbus signals
0	*VSYSRESET
1	VME_BUFF_DIR (schematic "VDIR")
2	nVME_BUFF_OE (schematic "nVnOE")
7..3	nGA_ID(4..0)
15..8	SWADDR(8..1)

Table 6.7, LED's set #14.

LED#	Led Test. This set is used to check that all the LEDs are functioning.
15..0	Both Green and Red LEDs are always ON (Orange light).

Table 6.7, LED's set #15.

7 Appendix A - Backplane Interface - connectors pinout

The following three tables describe the pin assignment for the backplane interface. The signals marked with a [●] are not used on the VLSB module. Signal highlighted in green are those used by the VLSB module and are connected to the module logic (Module Controller FPGA).

The 160 pin J1 and J2 connectors are completely optional in the VME64 standard but they are used in the VLSB design.

Pin#	Row Z (VME64x)	Row A	Row B	Row C	Row D (VME64x)
1	MPR (Bus Pause Request) [●]	D00 (Data Bus)	BBSY* (Bus Busy)	D08 (Data Bus)	VPC (Voltage Pre-Charge) [●]
2	GND (Ground)	D01 (Data Bus)	BCLR* (Bus Clear)	D09 (Data Bus)	GND (Ground)
3	MCLK (Module Clock) [●]	D02 (Data Bus)	ACFAIL* (AC Power Fail) [●]	D10 (Data Bus)	+V1 (auxiliary power) [●]
4	GND (Ground)	D03 (Data Bus)	BG0IN* (Bus Grant daisy-chain) [●]	D11 (Data Bus)	+V2 (auxiliary power) [●]
5	MSD (Slave Data) [●]	D04 (Data Bus)	BG0OUT* (Bus Grant daisy-chain) [●]	D12 (Data Bus)	ResvU (reserved Unbussed) [●]
6	GND (Ground)	D05 (Data Bus)	BG1IN* (Bus Grant daisy-chain) [●]	D13 (Data Bus)	-V1 (auxiliary power) [●]
7	MMD (Module Data) [●]	D06 (Data Bus)	BG1OUT* (Bus Grant daisy-chain) [●]	D14 (Data Bus)	-V2 (auxiliary power) [●]
8	GND (Ground)	D07 (Data Bus)	BG2IN* (Bus Grant daisy-chain) [●]	D15 (Data Bus)	ResvU (reserved Unbussed) [●]
9	MCTL (Module Control) [●]	GND (Ground)	BG2OUT* (Bus Grant daisy-chain) [●]	GND (Ground)	GAP* (Geographical Address Parity)
10	GND (Ground)	SYSCLK	BG3IN* (Bus Grant daisy-chain) [●]	SYSFAIL* (System Fail) [●]	GA0* (Geographical Address)
11	RESP* (Response) [●]	GND (Ground)	BG3OUT* (Bus Grant daisy-chain) [●]	BERR* (Bus Error)	GA1* (Geographical Address)
12	GND (Ground)	DS1* (Data Strobe)	BR0* (Bus Request) [●]	SYSRESET* (System Reset)	Power:+3.3V
13	ResBus (Reserved Bussed) [●]	DS0* (Data Strobe)	BR1* (Bus Request) [●]	LWORD* (Long Word)	GA2* (Geographical Address)
14	GND (Ground)	WRITE* (Read/Write)	BR2* (Bus Request) [●]	AM5 (Address Modifier)	Power:+3.3V
15	ResBus (Reserved Bussed) [●]	GND (Ground)	BR3* (Bus Request) [●]	A23 (Address Bus)	GA3* (Geographical Address)
16	GND (Ground)	DTACK* (Data Transfer Acknowledge)	AM0 (Address Modifier)	A22 (Address Bus)	Power:+3.3V
17	ResBus (Reserved Bussed) [●]	GND (Ground)	AM1 (Address Modifier)	A21 (Address Bus)	GA4* (Geographical Address)
18	GND (Ground)	AS* (Address Strobe)	AM2 (Address Modifier)	A20 (Address Bus)	Power:+3.3V
19	ResBus (Reserved Bussed) [●]	GND (Ground)	AM3 (Address Modifier)	A19 (Address Bus)	ResBus (Reserved Bussed) [●]
20	GND (Ground)	IACK* [●] (Interrupt Acknowledge)	GND (Ground)	A18 (Address Bus)	Power:+3.3V
21	ResBus (Reserved Bussed) [●]	IACKIN* [●] (Interrupt Acknowledge daisy-chain)	SERA (Serial Bus)[●]	A17 (Address Bus)	ResBus (Reserved Bussed) [●]
22	GND (Ground)	IACKOUT* [●] (Interrupt Acknowledge daisy-chain)	SERB (Serial Bus)[●]	A16 (Address Bus)	Power:+3.3V
23	ResBus (Reserved Bussed) [●]	AM4 (Address Modifier)	GND (Ground)	A15 (Address Bus)	ResBus (Reserved Bussed) [●]
24	GND (Ground)	A07 (Address Bus)	IRQ7* (Interrupt request) [●]	A14 (Address Bus)	Power:+3.3V
25	ResBus (Reserved Bussed) [●]	A06 (Address Bus)	IRQ6* (Interrupt request) [●]	A13 (Address Bus)	ResBus (Reserved Bussed) [●]
26	GND (Ground)	A05 (Address Bus)	IRQ5* (Interrupt request) [●]	A12 (Address Bus)	Power:+3.3V
27	ResBus (Reserved Bussed) [●]	A04 (Address Bus)	IRQ4* (Interrupt request) [●]	A11 (Address Bus)	LI/I* [●]
28	GND (Ground)	A03 (Address Bus)	IRQ3* (Interrupt request) [●]	A10 (Address Bus)	Power:+3.3V
29	ResBus (Reserved Bussed) [●]	A02 (Address Bus)	IRQ2* (Interrupt request) [●]	A09 (Address Bus)	LI/O* [●]
30	GND (Ground)	A01 (Address Bus)	IRQ1* (Interrupt request) [●]	A08 (Address Bus)	Power:+3.3V
31	ResBus (Reserved Bussed) [●]	Power: -12V	Power: +5VSTDBY [●]	Power: +12V	GND (Ground)
32	GND (Ground)	Power: +5V	Power: +5V	Power: +5V	VPC (Voltage Pre-Charge) [●]

Table 7.1. J1/P1 Pin Assignments

Pin#	Row Z (VME64x)	Row A	Row B	Row C	Row D (VME64x)
1	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
2	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
3	UD (User Defined)	UD (User Defined)	RETRY*	UD (User Defined)	UD (User Defined)
4	GND (Ground)	UD (User Defined)	A24 (Address Bus)	UD (User Defined)	UD (User Defined)
5	UD (User Defined)	UD (User Defined)	A25 (Address Bus)	UD (User Defined)	UD (User Defined)
6	GND (Ground)	UD (User Defined)	A26 (Address Bus)	UD (User Defined)	UD (User Defined)
7	UD (User Defined)	UD (User Defined)	A27 (Address Bus)	UD (User Defined)	UD (User Defined)
8	GND (Ground)	UD (User Defined)	A28 (Address Bus)	UD (User Defined)	UD (User Defined)
9	UD (User Defined)	UD (User Defined)	A29 (Address Bus)	UD (User Defined)	UD (User Defined)
10	GND (Ground)	UD (User Defined)	A30 (Address Bus)	UD (User Defined)	UD (User Defined)
11	UD (User Defined)	UD (User Defined)	A31 (Address Bus)	UD (User Defined)	UD (User Defined)
12	GND (Ground)	UD (User Defined)	Ground	UD (User Defined)	UD (User Defined)
13	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
14	GND (Ground)	UD (User Defined)	D16 (Data Bus)	UD (User Defined)	UD (User Defined)
15	UD (User Defined)	UD (User Defined)	D17 (Data Bus)	UD (User Defined)	UD (User Defined)
16	GND (Ground)	UD (User Defined)	D18 (Data Bus)	UD (User Defined)	UD (User Defined)
17	UD (User Defined)	UD (User Defined)	D19 (Data Bus)	UD (User Defined)	UD (User Defined)
18	GND (Ground)	UD (User Defined)	D20 (Data Bus)	UD (User Defined)	UD (User Defined)
19	UD (User Defined)	UD (User Defined)	D21 (Data Bus)	UD (User Defined)	UD (User Defined)
20	GND (Ground)	UD (User Defined)	D22 (Data Bus)	UD (User Defined)	UD (User Defined)
21	UD (User Defined)	UD (User Defined)	D23 (Data Bus)	UD (User Defined)	UD (User Defined)
22	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
23	UD (User Defined)	UD (User Defined)	D24 (Data Bus)	UD (User Defined)	UD (User Defined)
24	GND (Ground)	UD (User Defined)	D25 (Data Bus)	UD (User Defined)	UD (User Defined)
25	UD (User Defined)	UD (User Defined)	D26 (Data Bus)	UD (User Defined)	UD (User Defined)
26	GND (Ground)	UD (User Defined)	D27 (Data Bus)	UD (User Defined)	UD (User Defined)
27	UD (User Defined)	UD (User Defined)	D28 (Data Bus)	UD (User Defined)	UD (User Defined)
28	GND (Ground)	UD (User Defined)	D29 (Data Bus)	UD (User Defined)	UD (User Defined)
29	UD (User Defined)	UD (User Defined)	D30 (Data Bus)	UD (User Defined)	UD (User Defined)
30	GND (Ground)	UD (User Defined)	D31 (Data Bus)	UD (User Defined)	UD (User Defined)
31	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	GND (Ground)
32	GND (Ground)	UD (User Defined)	Power: +5V	UD (User Defined)	VPC (Voltage Pre-Charge) [●]

Table 7.2. J2/P2 Pin Assignments

8 Appendix B - LVDS SERDES Interface - connectors pinout

Table 8.1 shows the pinout of the input links front panel connector. Each input link has three differential pairs for data and one pair for the clock. On the LVDS cables the center column is connected to the cable shield. The center column of the board connector and all the pins labeled as "IS_GND" are connected to a copper pour that can be left floating, connected to the earth ground (front panel, chassis), or to the VLSB Module digital ground. The connection between the input links shield ground copper pour and the earth or digital ground can be done placing a solder bridge between two pads on the bottom front corner (solder side) of the VLSB Module.

Link#	Pin #	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'
3	8	D1	/D1	IS_GND	D2	/D2
	7	/D0	D0	IS_GND	CLK	/CLK
2	6	D1	/D1	IS_GND	D2	/D2
	5	/D0	D0	IS_GND	CLK	/CLK
1	4	D1	/D1	IS_GND	D2	/D2
	3	/D0	D0	IS_GND	CLK	/CLK
0	2	D1	/D1	IS_GND	D2	/D2
	1	/D0	D0	IS_GND	CLK	/CLK

Table 8.1, Signal assignments for the LVDS SERDES inputs connector.

9 Appendix C - Logic Analyzer Connectors Pinout

The following tables list the signals connected to the VLSB module's logic analyzer connectors. Four of the logic analyzer connectors are connected to the outputs of the LVDS SERDES receivers.

Three analyzer connectors are connected to the backplane VME signals.

The eighth logic analyzer connector is directly connected to the FPGA and the signals driving it can be assigned in the FPGA hardware description (VHDL code). These user-defined connections are marked with ⚠.

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
not connected	N.C.	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
Link “n” clock	RXCLKn	5	CLK1	CLK2	6	N.C.	not connected
Link “n” data bit 15	RXnD15	7	P1.15	P2.15	8	N.C.	not connected
Link “n” data bit 14	RXnD14	9	P1.14	P2.14	10	N.C.	not connected
Link “n” data bit 13	RXnD13	11	P1.13	P2.13	12	N.C.	not connected
Link “n” data bit 12	RXnD12	13	P1.12	P2.12	14	N.C.	not connected
Link “n” data bit 11	RXnD11	15	P1.11	P2.11	16	N.C.	not connected
Link “n” data bit 10	RXnD10	17	P1.10	P2.10	18	N.C.	not connected
Link “n” data bit 9	RXnD9	19	P1.09	P2.09	20	N.C.	not connected
Link “n” data bit 8	RXnD8	21	P1.08	P2.08	22	N.C.	not connected
Link “n” data bit 7	RXnD7	23	P1.07	P2.07	24	N.C.	not connected
Link “n” data bit 6	RXnD6	25	P1.06	P2.06	26	N.C.	not connected
Link “n” data bit 5	RXnD5	27	P1.05	P2.05	28	N.C.	not connected
Link “n” data bit 4	RXnD4	29	P1.04	P2.04	30	RXnD20	Link “n” data bit 20
Link “n” data bit 3	RXnD3	31	P1.03	P2.03	32	RXnD19	Link “n” data bit 19
Link “n” data bit 2	RXnD2	33	P1.02	P2.02	34	RXnD18	Link “n” data bit 18
Link “n” data bit 1	RXnD1	35	P1.01	P2.01	36	RXnD17	Link “n” data bit 17
Link “n” data bit 0	RXnD0	37	P1.00	P2.00	38	RXnD16	Link “n” data bit 16

Table 9.1, HP Logic Analyzer connector J1, J3, J4, J5 (LVDS RXs)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
not connected	N.C.	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
not connected	N.C.	5	CLK1	CLK2	6	N.C.	not connected
VME Address bit 15	VA15	7	P1.15	P2.15	8	VA31	VME Address bit 31
VME Address bit 14	VA14	9	P1.14	P2.14	10	VA30	VME Address bit 30
VME Address bit 13	VA13	11	P1.13	P2.13	12	VA29	VME Address bit 29
VME Address bit 12	VA12	13	P1.12	P2.12	14	VA28	VME Address bit 28
VME Address bit 11	VA11	15	P1.11	P2.11	16	VA27	VME Address bit 27
VME Address bit 10	VA10	17	P1.10	P2.10	18	VA26	VME Address bit 26
VME Address bit 9	VA9	19	P1.09	P2.09	20	VA25	VME Address bit 25
VME Address bit 8	VA8	21	P1.08	P2.08	22	VA24	VME Address bit 24
VME Address bit 7	VA7	23	P1.07	P2.07	24	VA23	VME Address bit 23
VME Address bit 6	VA6	25	P1.06	P2.06	26	VA22	VME Address bit 22
VME Address bit 5	VA5	27	P1.05	P2.05	28	VA21	VME Address bit 21
VME Address bit 4	VA4	29	P1.04	P2.04	30	VA20	VME Address bit 20
VME Address bit 3	VA3	31	P1.03	P2.03	32	VA19	VME Address bit 19
VME Address bit 2	VA2	33	P1.02	P2.02	34	VA18	VME Address bit 18
VME Address bit 1	VA1	35	P1.01	P2.01	36	VA17	VME Address bit 17
Connected to ground	GND	37	P1.00	P2.00	38	VA16	VME Address bit 16

Table 9.2, HP Logic Analyzer connector J12 (VME address)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
not connected	N.C.	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
System Clock	VSYSCLK	5	CLK1	CLK2	6	N.C.	not connected
Data Transfer Ack	VDTACK	7	P1.15	P2.15	8	N.C.	not connected
Bus Error	VBERR	9	P1.14	P2.14	10	N.C.	not connected
Bus Busy	/VBBSY	11	P1.13	P2.13	12	N.C.	not connected
Bus Clear	/VBCLR	13	P1.12	P2.12	14	N.C.	not connected
System Reset	/VSYSRESET	15	P1.11	P2.11	16	N.C.	not connected
Data Strobe 1	/VDS1	17	P1.10	P2.10	18	N.C.	not connected
Data Strobe 0	/VDS0	19	P1.09	P2.09	20	N.C.	not connected
Long Word	/VLWORD	21	P1.08	P2.08	22	N.C.	not connected
Address Strobe	/VAS	23	P1.07	P2.07	24	N.C.	not connected
Write	/VWRITE	25	P1.06	P2.06	26	N.C.	not connected
Address Modifier 5	VAM5	27	P1.05	P2.05	28	N.C.	not connected
Address Modifier 4	VAM4	29	P1.04	P2.04	30	N.C.	not connected
Address Modifier 3	VAM3	31	P1.03	P2.03	32	N.C.	not connected
Address Modifier 2	VAM2	33	P1.02	P2.02	34	N.C.	not connected
Address Modifier 1	VAM1	35	P1.01	P2.01	36	N.C.	not connected
Address Modifier 0	VAM0	37	P1.00	P2.00	38	N.C.	not connected

Table 9.3, HP Logic Analyzer connector J14 (VME control)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
not connected	N.C.	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
not connected	N.C.	5	CLK1	CLK2	6	N.C.	not connected
VME Data bit 15	VD15	7	P1.15	P2.15	8	VD31	VME Data bit 31
VME Data bit 14	VD14	9	P1.14	P2.14	10	VD30	VME Data bit 30
VME Data bit 13	VD13	11	P1.13	P2.13	12	VD29	VME Data bit 29
VME Data bit 12	VD12	13	P1.12	P2.12	14	VD28	VME Data bit 28
VME Data bit 11	VD11	15	P1.11	P2.11	16	VD27	VME Data bit 27
VME Data bit 10	VD10	17	P1.10	P2.10	18	VD26	VME Data bit 26
VME Data bit 9	VD9	19	P1.09	P2.09	20	VD25	VME Data bit 25
VME Data bit 8	VD8	21	P1.08	P2.08	22	VD24	VME Data bit 24
VME Data bit 7	VD7	23	P1.07	P2.07	24	VD23	VME Data bit 23
VME Data bit 6	VD6	25	P1.06	P2.06	26	VD22	VME Data bit 22
VME Data bit 5	VD5	27	P1.05	P2.05	28	VD21	VME Data bit 21
VME Data bit 4	VD4	29	P1.04	P2.04	30	VD20	VME Data bit 20
VME Data bit 3	VD3	31	P1.03	P2.03	32	VD19	VME Data bit 19
VME Data bit 2	VD2	33	P1.02	P2.02	34	VD18	VME Data bit 18
VME Data bit 1	VD1	35	P1.01	P2.01	36	VD17	VME Data bit 17
VME Data bit 0	VD0	37	P1.00	P2.00	38	VD16	VME Data bit 16

Table 9.4, HP Logic Analyzer connector J16 (VME data)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
Voltage selected with R84 (+3.3V) or R85 (+5V)	+3.3V or +5V	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
not connected	N.C.	5	CLK1	CLK2	6	PCLK2	FPGA diagnostic PCLK2
FPGA diagnostic P1_15	P1_15	7	P1.15	P2.15	8	P2_15	FPGA diagnostic P2_15
FPGA diagnostic P1_14	P1_14	9	P1.14	P2.14	10	P2_14	FPGA diagnostic P2_14
FPGA diagnostic P1_13	P1_13	11	P1.13	P2.13	12	P2_13	FPGA diagnostic P2_13
FPGA diagnostic P1_12	P1_12	13	P1.12	P2.12	14	P2_12	FPGA diagnostic P2_12
FPGA diagnostic P1_11	P1_11	15	P1.11	P2.11	16	P2_11	FPGA diagnostic P2_11
FPGA diagnostic P1_10	P1_10	17	P1.10	P2.10	18	P2_10	FPGA diagnostic P2_10
FPGA diagnostic P1_9	P1_9	19	P1.09	P2.09	20	P2_9	FPGA diagnostic P2_9
FPGA diagnostic P1_8	P1_8	21	P1.08	P2.08	22	P2_8	FPGA diagnostic P2_8
FPGA diagnostic P1_7	P1_7	23	P1.07	P2.07	24	P2_7	FPGA diagnostic P2_7
FPGA diagnostic P1_6	P1_6	25	P1.06	P2.06	26	P2_6	FPGA diagnostic P2_6
FPGA diagnostic P1_5	P1_5	27	P1.05	P2.05	28	P2_5	FPGA diagnostic P2_5
FPGA diagnostic P1_4	P1_4	29	P1.04	P2.04	30	P2_4	FPGA diagnostic P2_4
FPGA diagnostic P1_3	P1_3	31	P1.03	P2.03	32	P2_3	FPGA diagnostic P2_3
FPGA diagnostic P1_2	P1_2	33	P1.02	P2.02	34	P2_2	FPGA diagnostic P2_2
FPGA diagnostic P1_1	P1_1	35	P1.01	P2.01	36	P2_1	FPGA diagnostic P2_1
FPGA diagnostic P1_0	P1_0	37	P1.00	P2.00	38	P2_0	FPGA diagnostic P2_0

Table 9.5, HP Logic Analyzer connector J10 (User Defined - FPGA)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
Voltage selected to 3.3V with R84 (+3.3V)	**+3.3V**	1	+5VDC	SCL	2	N.C.	not connected
Ground	GND	3	GND	SDA	4	N.C.	not connected
not connected	N.C.	5	CLK1	CLK2	6	PCLK2	TX Link clock
TX Link data bit 15	P1_15	7	P1.15	P2.15	8	P2_15	FPGA diagnostic P2_15
TX Link data bit 14	P1_14	9	P1.14	P2.14	10	P2_14	FPGA diagnostic P2_14
TX Link data bit 13	P1_13	11	P1.13	P2.13	12	P2_13	FPGA diagnostic P2_13
TX Link data bit 12	P1_12	13	P1.12	P2.12	14	P2_12	FPGA diagnostic P2_12
TX Link data bit 11	P1_11	15	P1.11	P2.11	16	P2_11	FPGA diagnostic P2_11
TX Link data bit 10	P1_10	17	P1.10	P2.10	18	P2_10	FPGA diagnostic P2_10
TX Link data bit 9	P1_9	19	P1.09	P2.09	20	P2_9	FPGA diagnostic P2_9
TX Link data bit 8	P1_8	21	P1.08	P2.08	22	P2_8	FPGA diagnostic P2_8
TX Link data bit 7	P1_7	23	P1.07	P2.07	24	P2_7	FPGA diagnostic P2_7
TX Link data bit 6	P1_6	25	P1.06	P2.06	26	P2_6	FPGA diagnostic P2_6
TX Link data bit 5	P1_5	27	P1.05	P2.05	28	P2_5	FPGA diagnostic P2_5
TX Link data bit 4	P1_4	29	P1.04	P2.04	30	P2_4	TX Link data bit 20
TX Link data bit 3	P1_3	31	P1.03	P2.03	32	P2_3	TX Link data bit 19
TX Link data bit 2	P1_2	33	P1.02	P2.02	34	P2_2	TX Link data bit 18
TX Link data bit 1	P1_1	35	P1.01	P2.01	36	P2_1	TX Link data bit 17
TX Link data bit 0	P1_0	37	P1.00	P2.00	38	P2_0	TX Link data bit 16

Table 9.6, HP Logic Analyzer connector J10 (LVDS Test Mode - FPGA)

10 Appendix D - VLSB Module Components and Layout

10.1 Front Panel Layout

10.2 Module Controller FPGA

The Xilinx XC3S1500-4FG676C FPGA has 487 maximum user I/O, of which 403 are unrestricted user I/Os.

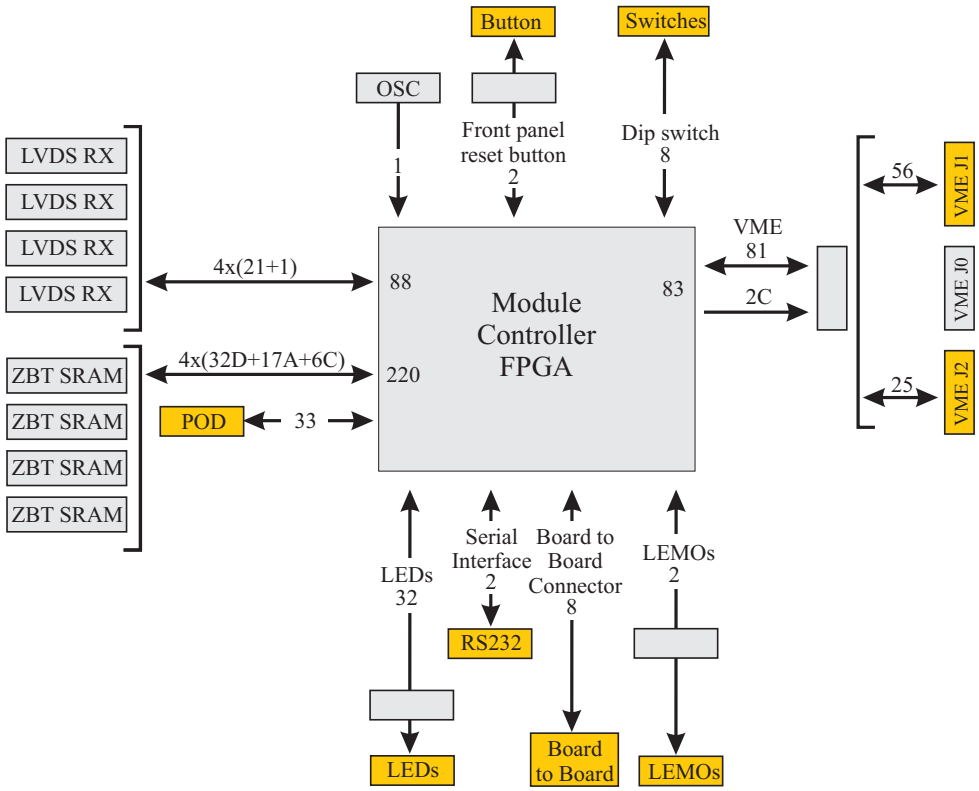

Figure 10.1, Module Controller FPGA pin usage

Pin Use	*Number of pin used*
VMEbus	56 (J1) + 25 (J2) +2C= 83
LVDS Links Receivers (SN65LVDS96)	4x(21D +1CLK) = 88 (4 Global Clock pins)
Memory Interface (CY7C1351F)	4x(32D +17A + 4C) = 212
Analyzer Diagnostic PODs	32 signals + 2 clocks = 34
LEDs	32
External trigger (LEMO)	2 signals
Serial Interface (RS232)	4
Front panel reset buttons	2 (soft and hard reset)
Dip-switches	8
53MHz Local Clock	1 (1 Global Clock pin)
Board to board interface	8 signals (1 Global Clock pin)
TOTAL	

Table 10.1, Module Controller FPGA pin usage

10.3 ZBT Memory

The VLSB Module uses four banks of Cypress CY7C1351F SRAM ZBT memory. Each bank is used to store the data received from one of the LVDS links.

11 Appendix E - D0 CTT System

Scintillating Fiber Detector

Scintillating fibers are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders (or layers). When a particle passes through a scintillating fiber, a brief flash of light occurs. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it, reaching a very sensible light detector, a Visible Light Photon Counter (VLPC). The light generated in each of the 40960 detector's scintillating fibers goes to an independent VLPC.

Visible Light Photon Counters (VLPCs)

The VLPCs are a derivative of solid-state photomultipliers (SSPM) but different than their predecessor in that they are blind in the infrared region. VLPCs are solid-state detectors capable of detecting single photons having wavelength of 0.4 to 28 um. Their operational temperature is between 6 and 14 K, requiring a cryogenic environment to operate. They are used in the CTT system to convert the scintillation light into an electrical signal, which is discriminated and digitized by the Analog Front-End boards (AFEs).

Analog Front-End Boards (AFEs) [Ref.]

The AFEs, process the analog signals from the VLPC channels, and supply the generated data to the mixer system. An Analog Front-End (AFE) board hosts 8 Multichip Modules (MCMs).

The digital data generated by the analog front-end will be used by the logic responsible for the level 1 trigger decisions. But before the data can be used for trigger generation it needs to be reorganized into trigger sectors, this is done by the mixer system.

Mixer system [Ref.]

The mixer system reorganize in “trigger sectors" the data received from the AFE system and send it to the logic generating the level 1 trigger (Digital Front-End boards).

Being the mixer system part of the electronics handling data used to generate a trigger, the data is processed (re-organized) in real-time and with the minimum possible delay. The mixer system consists of a 21 slot 6U VME type subrack with custom backplane. Slot 1 is occupied by a custom subrack controller, slot 2 to slot 21 hosts twenty mixer boards.

Digital Front-End Boards (DFEs) [Ref.]

The "trigger sector organized" data produced by the mixer system is passed to the Digital Front End boards (DFEs) system that does the triggering. Following the Digital Front End, there is other electronics that concentrate the information, look for trigger information and send/broadcast it up to the framework (collectors and broadcasters).

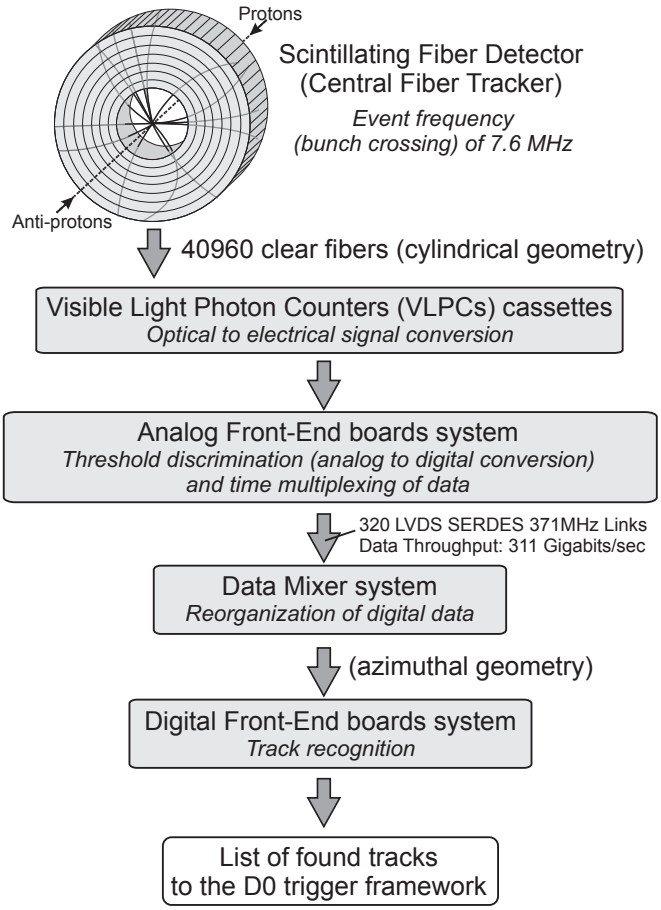

Figure 11.1, D0 CTT System

12 Glossary

AFE: acronym for Analog Front-End Board.

Analog Front-End Board (AFE): It has the function of receiving charge signals from the Central Fiber Tracker (CFT) and providing digital hit pattern for those charge signals. The AFEs are located on the VLPC cassette cryostat. More details in Chapter 11 and [Ref.].

ANSI: American National Standards Institute. More information is available on the Internet: http://www.ansi.org/

BIST: Built-In Self Test, the method of designing circuits with additional logic that can be used to test correct operation of the primary (functional) logic.

BSDL: Boundary Scan Description Language. IEEE 1149.1-1993b defines a language that describes IEEE 1149.1 architecture for an integrated circuit. This language is known as the Boundary Scan Description Language (BSDL). Updated BSDL files for the XILINX devices used on the VLSB Module can be found at: http://support.xilinx.com/support/sw_bsdl.htm

Compact Flash card: is a removable mass storage device. The card is designed based on the PC Card (PCMCIA) standard [Ref.].

CFT: Central Fiber Tracker.

CPS: Central Pre-Shower.

DFE: Digital Front-End board.

Digital Front-End Board: it has the function of generating the trigger using the data received from the mixer system. More details in Chapter 11 and [Ref.].

EDIF: Electronic Data Interchange Format. Industry-standard for specifying a logic design in text (ASCII) form.

File types:

JEDEC files

JEDEC files are CPLD programming files generated by the CPLD fitter. They are ASCII text files containing programming information and, optionally, functional test vectors that can be used to verify the correct functional behavior of the programmed device. One JEDEC file is required for each device in the JTAG programming chain. The extension for JEDEC files is .jed.

BSDL Summary files

The Boundary-Scan Description Language (BSDL) files use a subset of VHDL to describe the boundary scan features of a device. The Xilinx JTAG Programmer automatically extracts the length of the instruction register from the BSDL file to place non-Xilinx devices in bypass mode. The JTAG Programmer locates Xilinx BSDL files automatically. The name of the BSDL file is assumed to be <device name>.bsd.

BIT Files

Bit files are Xilinx FPGA configuration files generated by the Xilinx FPGA design software. They are proprietary format binary files containing configuration information. One BIT file is required for each Xilinx FPGA in the JTAG boundary-scan chain. The extension for BIT files is ".bit".

(MCS/EXO) PROM Files

The Xilinx PROM file formatter generates PROM programming files. The files are ASCII text files used to specify configuration data. One PROM file is required for each

Xilinx PROM in the JTAG boundary-scan chain. Use the device properties (Edit>Properties) dialog to specify the location of the MCS/EXO files for each Xilinx PROM. The required extensions for MCS and EXO files are ".mcs" and ".exo" respectively.

FPGA: Field Programmable Gate Array. An integrated circuit that contains configurable (programmable) logic blocks and configurable (programmable) interconnect between these blocks.

IEEE: Institute of Electrical and Electronics Engineers, Inc. More information is available on the Internet:
http://www.ieee.org/

Jedec: The JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council) is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. More information is available on the Internet:
http://www.jedec.org/

Jitter: The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

JTAG: Joint Test Action Group. Older name for IEEE 1149.1 boundary scan, a method to test printed circuit boards and also integrated circuits. See also BSDL.
Design complexity, difficulty of loaded board testing, and the limited pin access of surface mount technology led industry leaders to seek accord on a standard to support the solution of these problems.
The standard defines a hardware architecture and the mechanisms for its use.
The standard itself defines instructions that can be used to perform functional and interconnect tests as well as built-in self-test procedures. Vendor-specific extensions to the standard have been developed to allow execution of maintenance and diagnostic applications as well as programming algorithms for re-configurable parts.
The top level schematic of the test logic defined by IEEE Std 1149.1 includes three key blocks:

The *TAP Controller*

This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the other circuit blocks.

The *Instruction Register*

This shift register-based circuit is serially loaded with the instruction that selects an operation to be performed.

The *Data Registers*

These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

The *JTAG Test Access Port* (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data. The four pins of the TAP are: TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data In) and TDO (Test Data Out). The function of each TAP pin is as follows:

TCK - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers.

TMS - this pin is the mode input signal to the TAP Controller. The TAP controller is a FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. TMS has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven.

TDI -this pin is the serial data input to all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven. TDI is sampled into the JTAG registers on the rising edge of TCK.

TDO - this pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times.

LVDS: Low Voltage Differential Signaling, otherwise known as TIA/EIA-644. Is a signaling method used for high-speed, low-power transmission of binary data over copper [Ref.].

LVTTL: Low Voltage TTL. Is one of the several switching standards used in digital electronics.

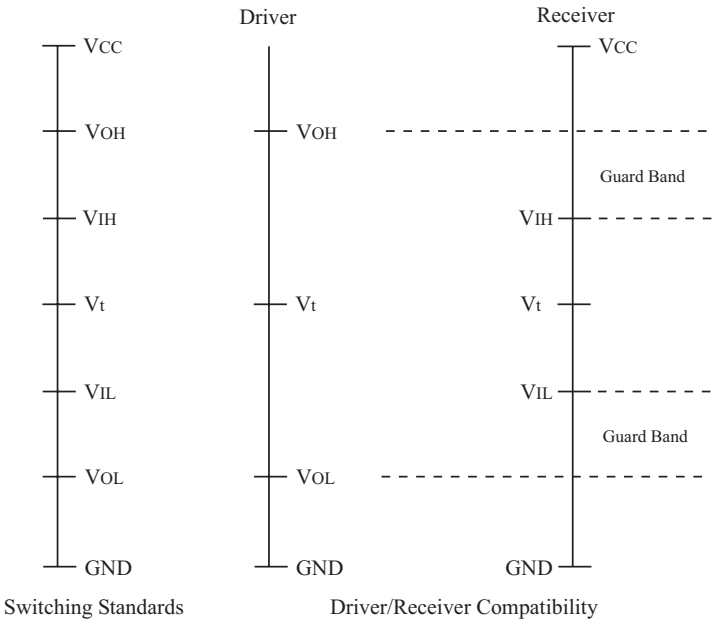

Figure 12.1, Switching standards.

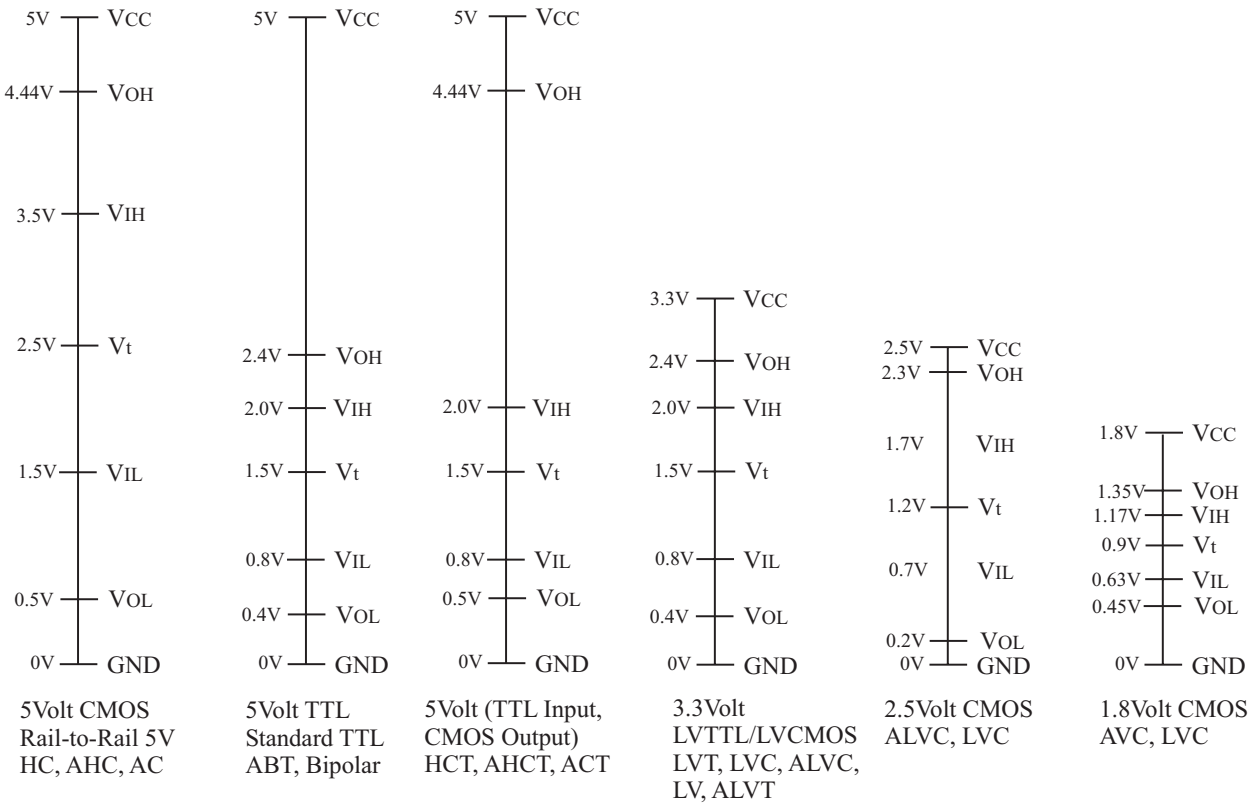

Figure 12.2, Comparison of switching standards.

SERDES: Serializer/Deserializer. Used to indicate LVDS components using data serialization (also called Data Channel Compression) to reduce the number of physical connection required for a data channel.

Skew: The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

VHDL: "V" stands for Very High Speed Integrated Circuit and "HDL" stands for Hardware Description Language.

VITA: VMEbus International Trade Association.
http://www.vita.com/

VME/VME64/VME64X: [Ref.] The VME (VERSAmodule Eurocard) standard was first defined in 1979 by Motorola Corporation. The VMEbus is an asynchonous bus that utilizes a *Master/Slave* architecture. The leftmost slot is the *Master*, and the remaining slots are *Slaves*. The VMEbus is composed of four sub-buses called the *Data Transfer Bus*, the *Data Transfer Arbitration Bus*, the *Priority Interrupt Bus*, and the *Utility Bus*. The original VMEbus standard maximum transfer speed is 40 Mbytes/sec. With the features of the newer VME64X standard described below, that transfer speed has quadrupled to 160 Mbytes/sec. Other features of VMEbus are:

-) 16, 24, or 32-bit addressing
-) 8, 16, 24, or 32-bit data path width
-) Allows unaligned data transfers
-) Error detection through *BERR signal
-) 7 levels of interrupts
-) System diagnostic capability using the *SYSFAIL signal
-) Mechanical standard allows 3U, 6U, or 9U printed circuit boards

The VME64 standard is a superset of the VME standard. Some of the added abilities for VME64 are:

-) Larger 64-bit data and address paths for 6U boards
-) 2 times the bandwidth (80 Mbytes/sec)
-) lower noise connector system
-) Cycle retry capability
-) Bus LOCK cycles
-) First slot detector
-) Automatic ‘plug and play” features

The VME64X standard is a superset of the VME standard. Some of the added abilities for VME64X are:

-) 4 times the bandwidth of VME (160 Mbytes/sec)
-) A new 160-pin connector family
-) A 95-pin J0 connector
-) 3.3V supply pins
-) Geographical addressing
-) 141 more user-defined I/O pins

The VME64X standard utilizes 3 sets of connectors that plug into the backplane. They are a 95-pin connector J0/P0, and two 160-pin connectors, J1/P1 and J2/P2.

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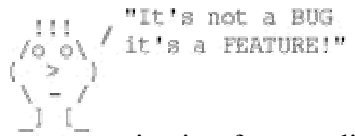

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[ ] Private communication from John Smith.