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Testing of the TriP Chip Running at 132 nsec Using a Modified AFE Board.

J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov

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DØ note 4076

1 Introduction

In this note we describe the first set of tests done with a sample of TriP chips that were mounted on a modified AFE board. The modifications consisted of different firmware and the replacement of one power supply switch. The board used was a standard AFEIc board (red type) on which new MCMs (MCMIIs) were mounted. The new MCMs were designed to support the TriP and emulate the SVX for readout when mounted on an AFEIc board. The TriP and the MCMs are described in Ref. [1].

Two versions of the MCMII were designed and built: one (MCMIIb) supports two TriP chips wirebonded directly to the MCM substrate. The other, (MCMIIc) supports one TriP which can be either wirebonded directly or packaged into a standard TQFP surface mount package. Due to space constraints, this MCM can support only 1 TriP.

We tested 6 TriP chips on 3 different MCMIIb (MCMIIb-1, MCMIIb-2 and MCMIIb-3) and 2 other TriPs were tested on MCMIIc, one of them with an unpackaged TriP (MCMIIc-1) and the other with a packaged TriP (MCMIIc-2).

A set of 10 programable internal registers control the TriP operation, the description of these registers can be found in [1]. Table 1 shows the values used for the tests described in this note.

Table 1: Table of registers values for the operation of the trip. (1): does not correspond to the default value for the register. (2): the discriminator threshold is set to VTH=210 unless otherwise noted.

Name	Register address	Register value
IBP	1	130 (1)
IBBNFol1	2	120
IFF	3	20 (1)
IBPIFF1REF	4	160
IBPOMAMP	5	138
IBPFol2	6	24
IFFP2	7	42
IBCOMP	8	10 (1)
VREF	9	150 (1)
VTH	10	210 (1) (2)

In Ref. [1] there is a description of the signals that are needed to operate the TriP chip. We implemented in a Field Programable Gate Array (FPGA), also part of the MCM, a set of shift registers that allow us to download via the 1553 interface to the AFE board, any desired timing for the signals that the FPGA has to send to the TriP chip. These registers are run with a 121.21 MHz clock (which is 16x the crossing clock and phase locked to it), which means that each bit corresponds to a time interval of 8.25 nsec. Finer control of timing is possible, but this changing the programing of the FPGA and recompiling. The bits downloaded to these shift regiters inside the TriP are listed in Table 2.

Table 2: Timing diagram for the operation of the TriP. Two different option for DIGEN are considered in this report, they correspond to options (A) and (B) in this table. Other signals are fixed inside the FPGA.

description	byte0	byte1
DIGENUP	00000000	00000010
DIGRSTB	01111111	11111111
PRE2BRSTB	00000011	11111100
PRERST	00000000	00011110
DIGEN(Option A)	11111111	11111111
DIGEN(Option B)	00000000	00000111

2 Discriminator Scan

As a first step in geting an understanding of the performace of the TriP we performed charge injection scan on each of the chips. The scans were done with the registers described in Table 1 and the timing specified in Option (A) of Table 2. Charge was injected on one channel at a time using the programable charge injection mechanism in the Trip. For each value of the input change, the occupancy of the discriminator output of the injected channel was registered for a total of 200 events and the results are shown in Figs. 1, 2, 3, 4, 5 and 6. Because the TriP chip has 32 channels separated in two banks of 16 channels and we want to understand possible difference between the two banks, the discriminator occupancy curves are plotted independently for each bank.

There is no scan for MCMIIb-3-Trip1, because that chip could not be turned on. It was determined that the chips has a short in the VDDA (analog power) net. This is a fabrication failure and should be considered when we estimate the yield for the TriP fabrication process. If we include the two chips tested on the bench by A.M. (the chip designer), the yield is 9/10.

In order to measure the active time window of the TriP chip when it is operated accoding to Option (A) in Table 2, we varied the delay of the charge injection pulse and recorded the discriminator occupancies. This was done injecting 20 fC charge in one channel at a time, and 200 events were recorded for each step. The results of MCMIIc-1 are shown in Fig. 7.

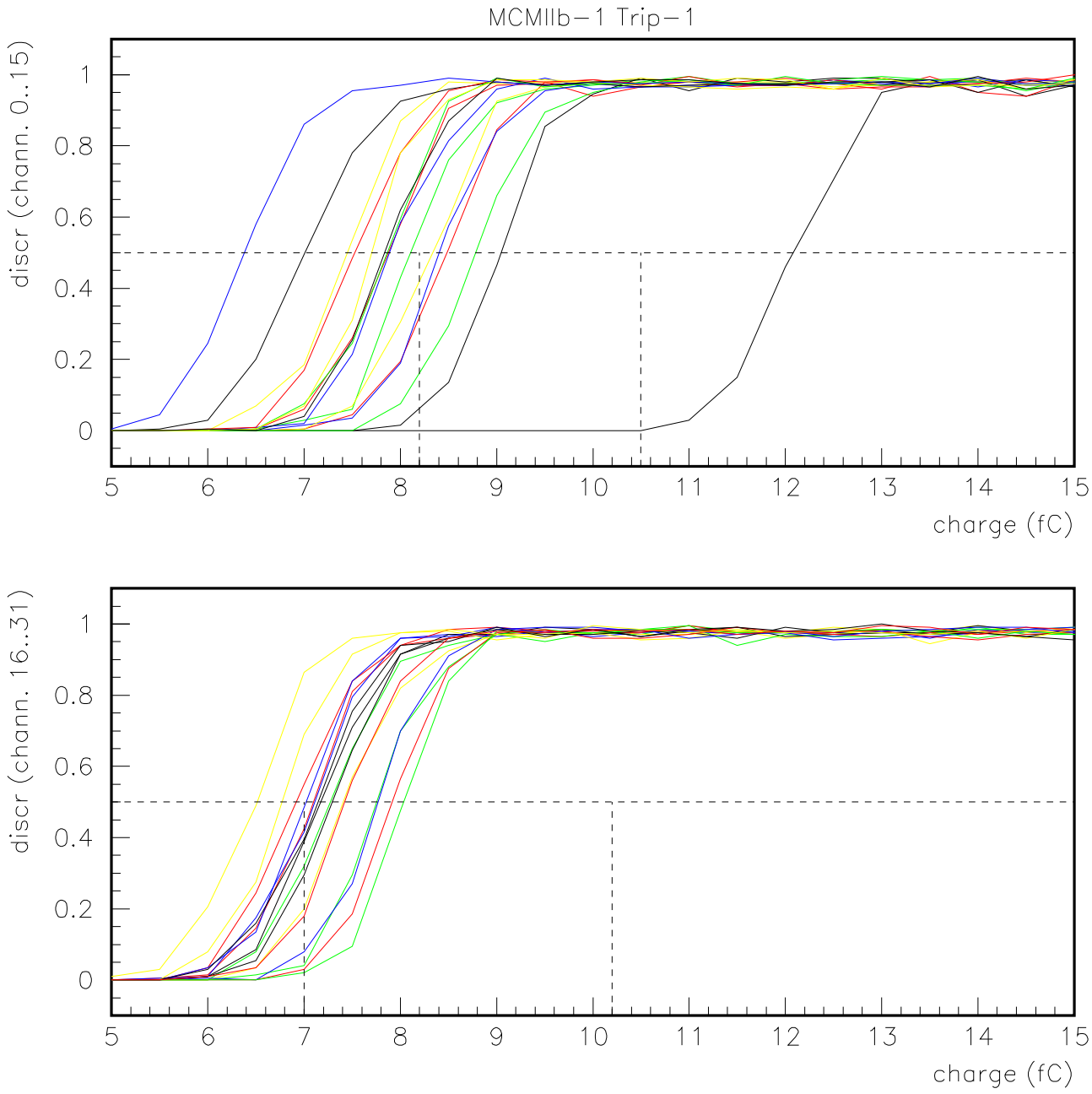

Figure 1: Discriminartor scan for MCMIIb-1-Trip1.

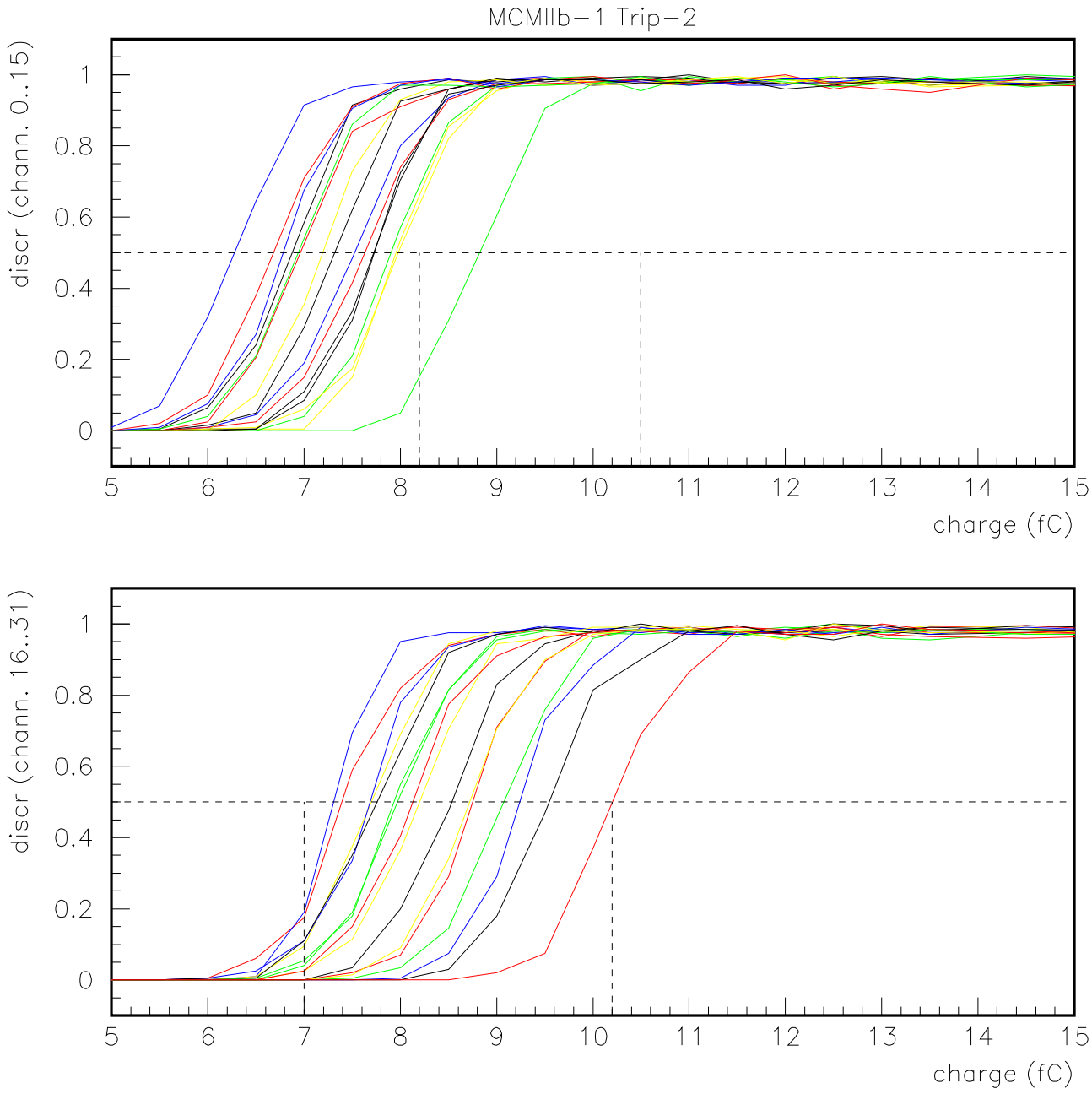

Figure 2: Discriminartor scan for MCMIIb-1-Trip2.

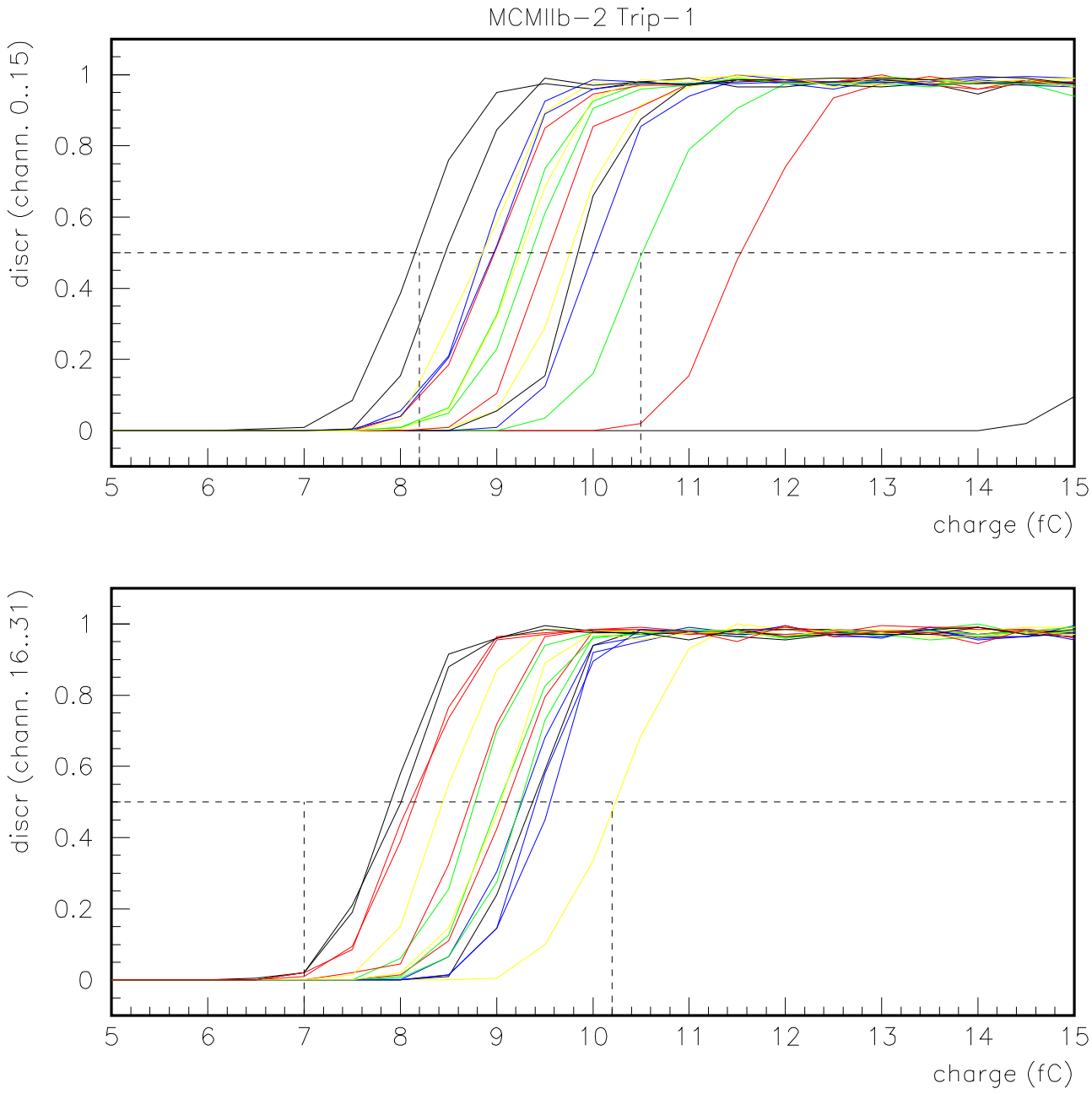

Figure 3: Discriminartor scan for MCMIIb-2-Trip1.

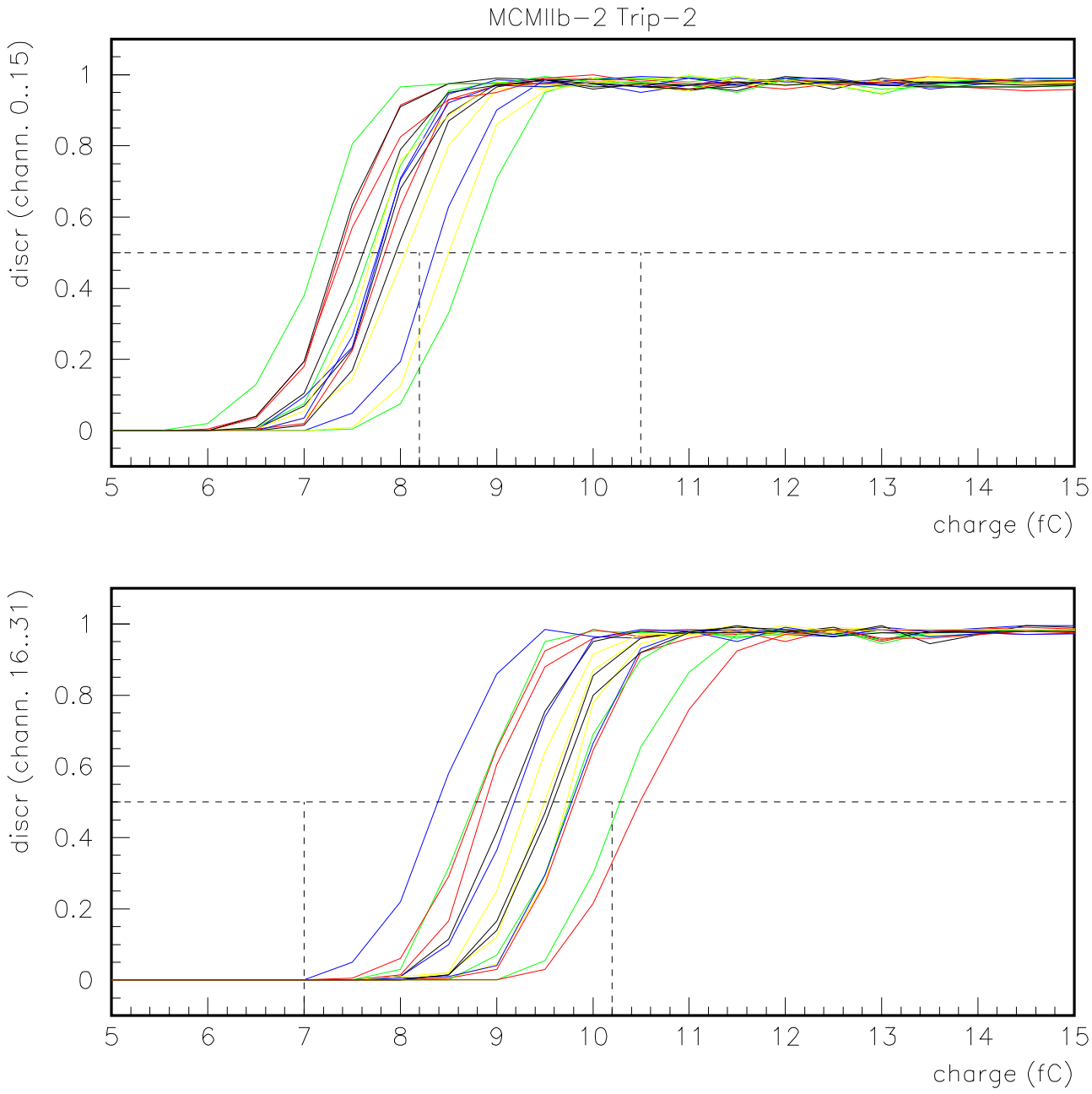

Figure 4: Discriminartor scan for MCMIIb-2-Trip2.

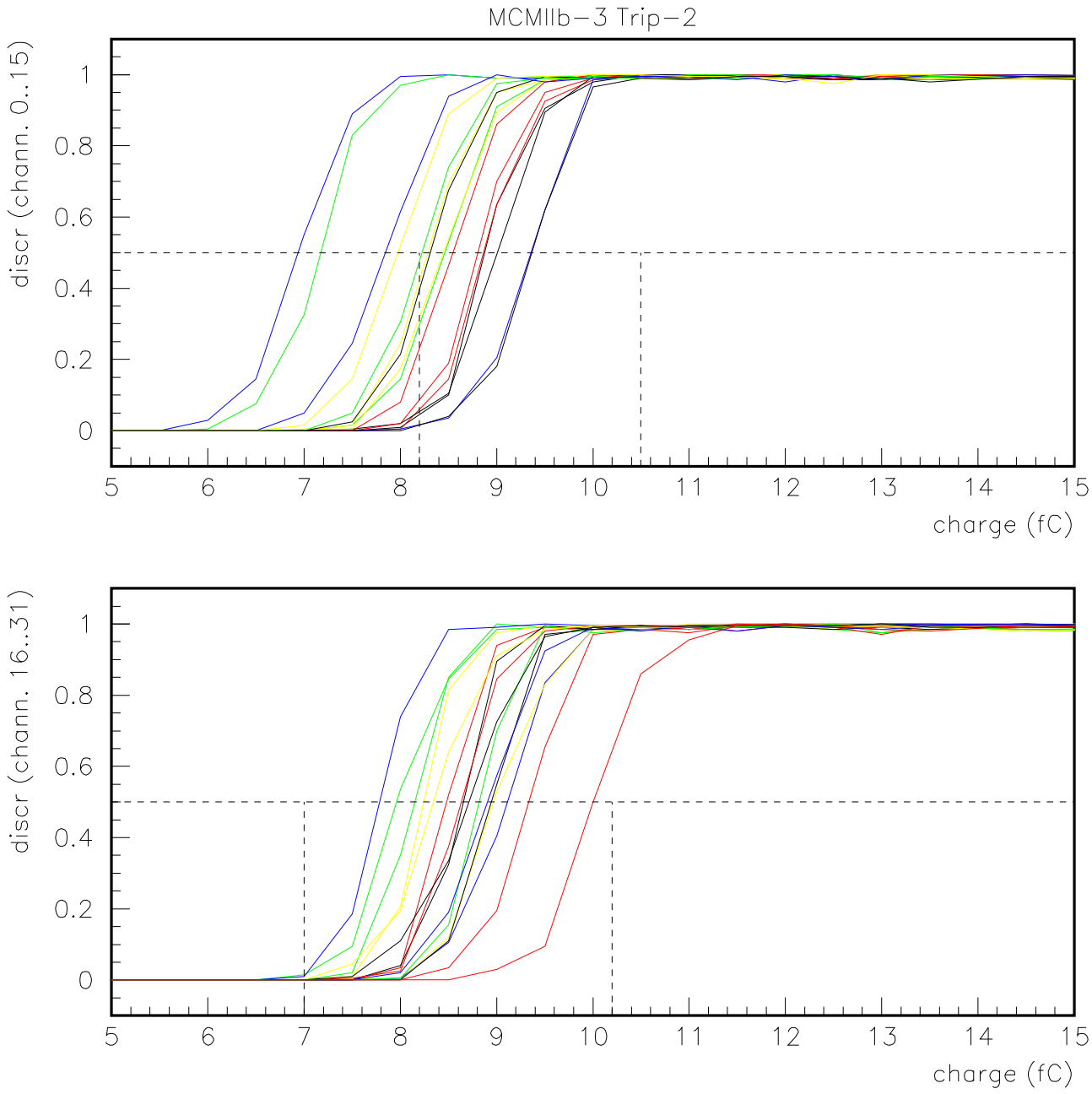

Figure 5: Discriminartor scan for MCMIIb-3-Trip2.

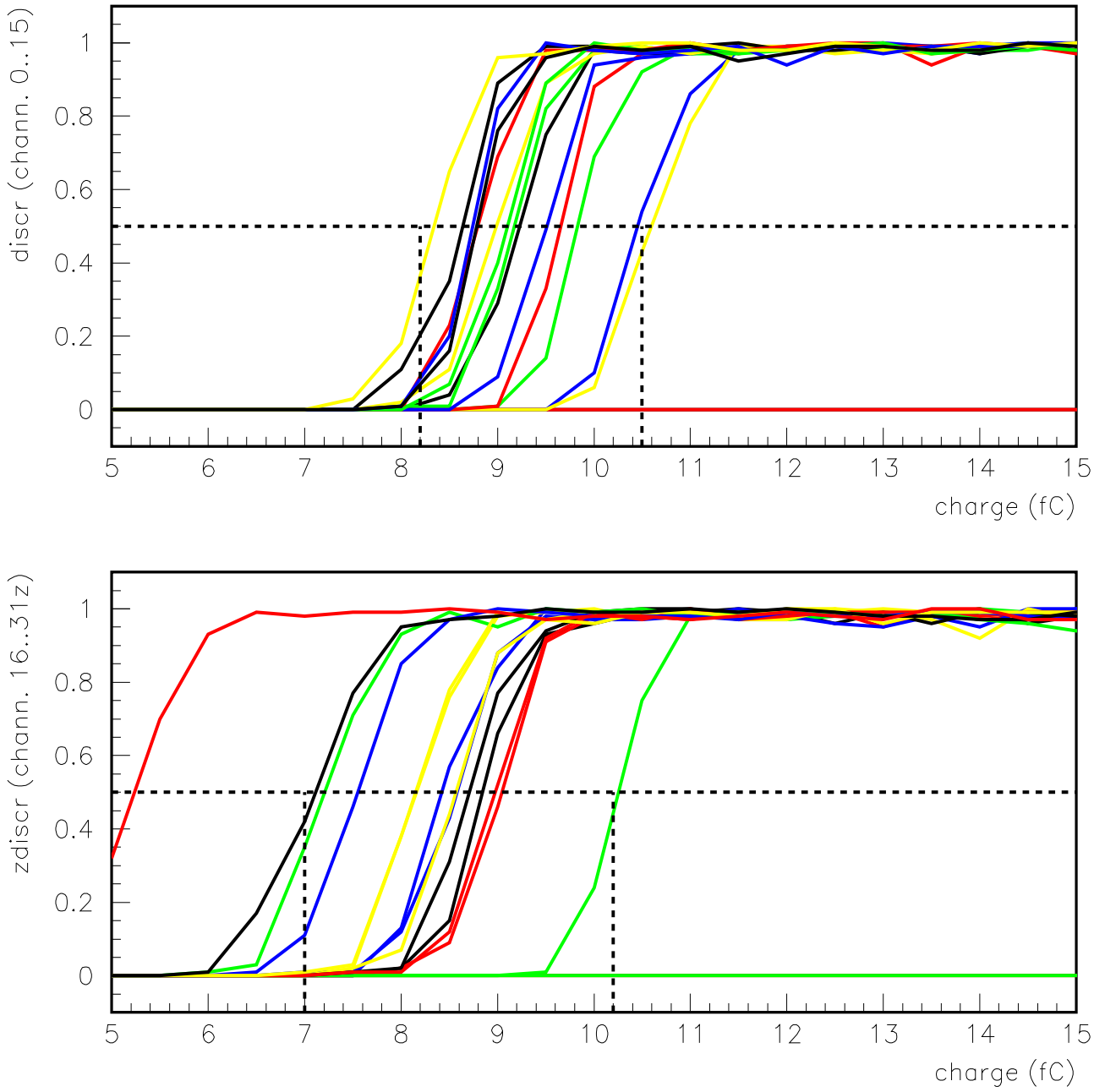

Figure 6: Discriminartor scan for MCMIIc-1-Trip2. (MCMIIc has only one TriP, that for layout reasons we call TriP 2.)

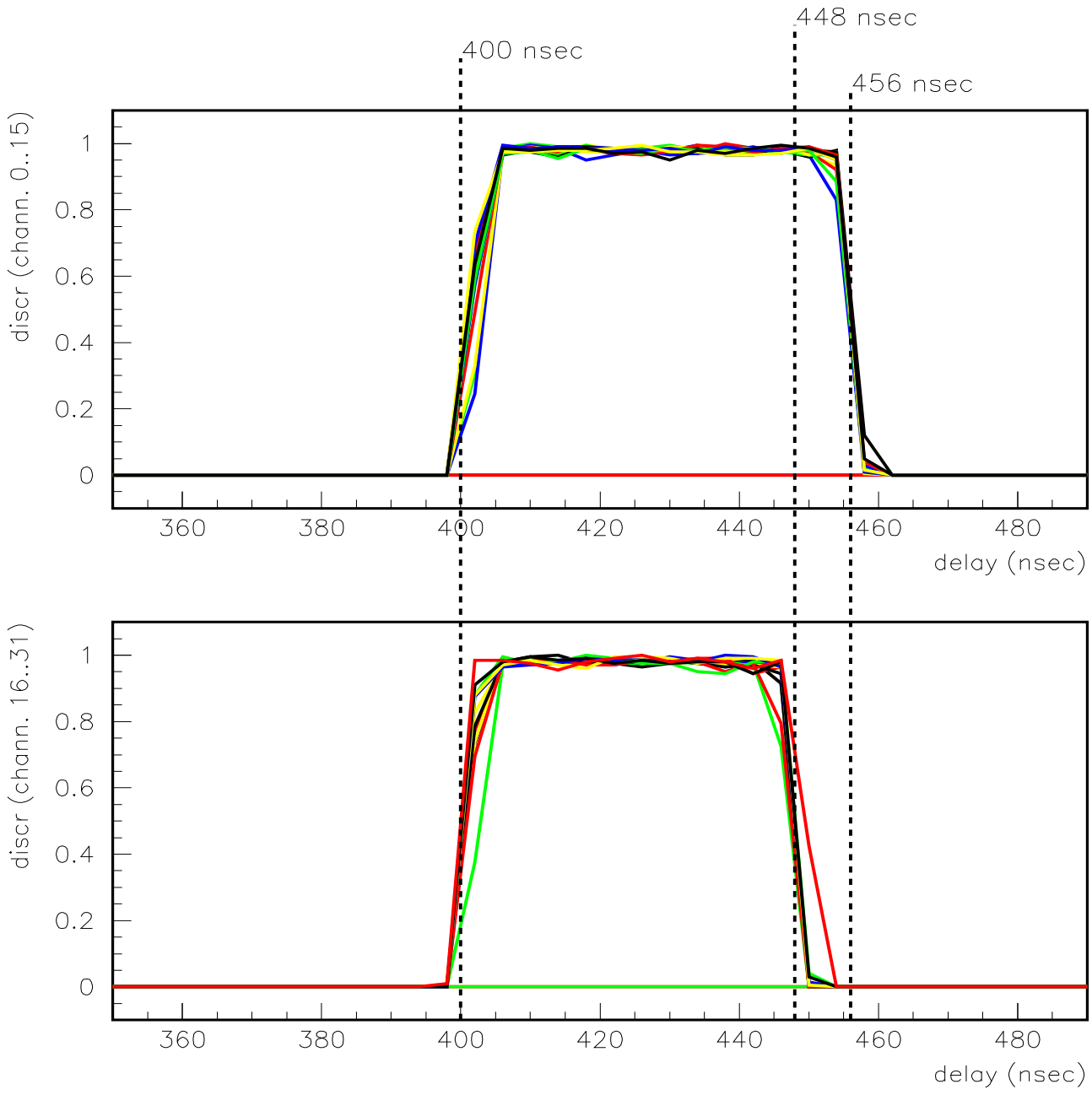

Figure 7: Timing scan for MCMIIc-1-Trip2.

2.1 Summary of the Charge Injections Scans.

From the discriminator turn-on curves presented in Figs. 1, 2, 3, 4, 5 and 6 we conclude:

- In MCMIIb, there is a layout problem that causes several low numbered channels in TriP 1 to turn on for larger input charge than most of its neighbors. The problem is caused by too close physical proximity of the discriminator output lines to the input lines.
- In MCMIIc-1, has one noisy channel that turns on eralier than expected (50% occupancy around 5 fC), this will have to be studied further with other MCMIIc. It appears to be a layout problem similar to the case for Trip 1 on MCMIIb. For MCMIIc-1, there are also 2 channels where the discriminator never fires, this is due to a problem in an electrical contact between the TriP chip and the FPGA in MCMIIc-1, the problem was caused by the repeated probing of the trace that was needed in the debugging stages of MCMIIc-1.
- Except for the 2 problems described above, that are most likely features of the layout and can be corrected in a future version of MCMII, the seven chips studied here present a total spread in the the discriminators of 4 fC or smaller. This is within the design specificationd for the TriP chip. (This total spread is measured along the 50% occupancy line.).
- We observed a 40 nsec window where the discriminator efficiency is 100% for a 20 fC charge injection. This window is acceptable for the operation of the TriP chip.

3 Analog Readout

In MCMII the analog output of the TriP chip is presented to a commercial ADC (AD9201), there is one AD9201 for each TriP. The digital output of this ADC is read by the FPGA (also mounted on the MCM) and combined with the discriminator information before it is sent to the Stand Alone Sequencer (SASeq) for readout. In this section we do some tests of this aspect of the system. The ADC has 10 bits, for these tests we have discarded the two least significant bits.

The signals required for the analog readout of the TriP chip are described in Ref. [1]. A scope picture of these signals is shown in Figs. 8 and 9.

The analog output of the TriP chip can also be studied as a function of the delay of the charge injection pulse, the results are shown in Fig. 10. This scan was done for MCMIIb-1-Trip1 and using Option (B) of Table 2 (the difference between the Options (A) and (B) will be discussed later in this note).

Another interesting aspect of the TriP that we need to consider is the spread in the analog pedestal. For this we have registered the analog pedestal on each channel when no charge is injected and the results are shown in Figs. 11 and 12.

As part of these studies of the analog readout of the TriP chip we also performed a calibration of the ADC output. The ADC output as a function of the input charge is shown in Fig. 13.

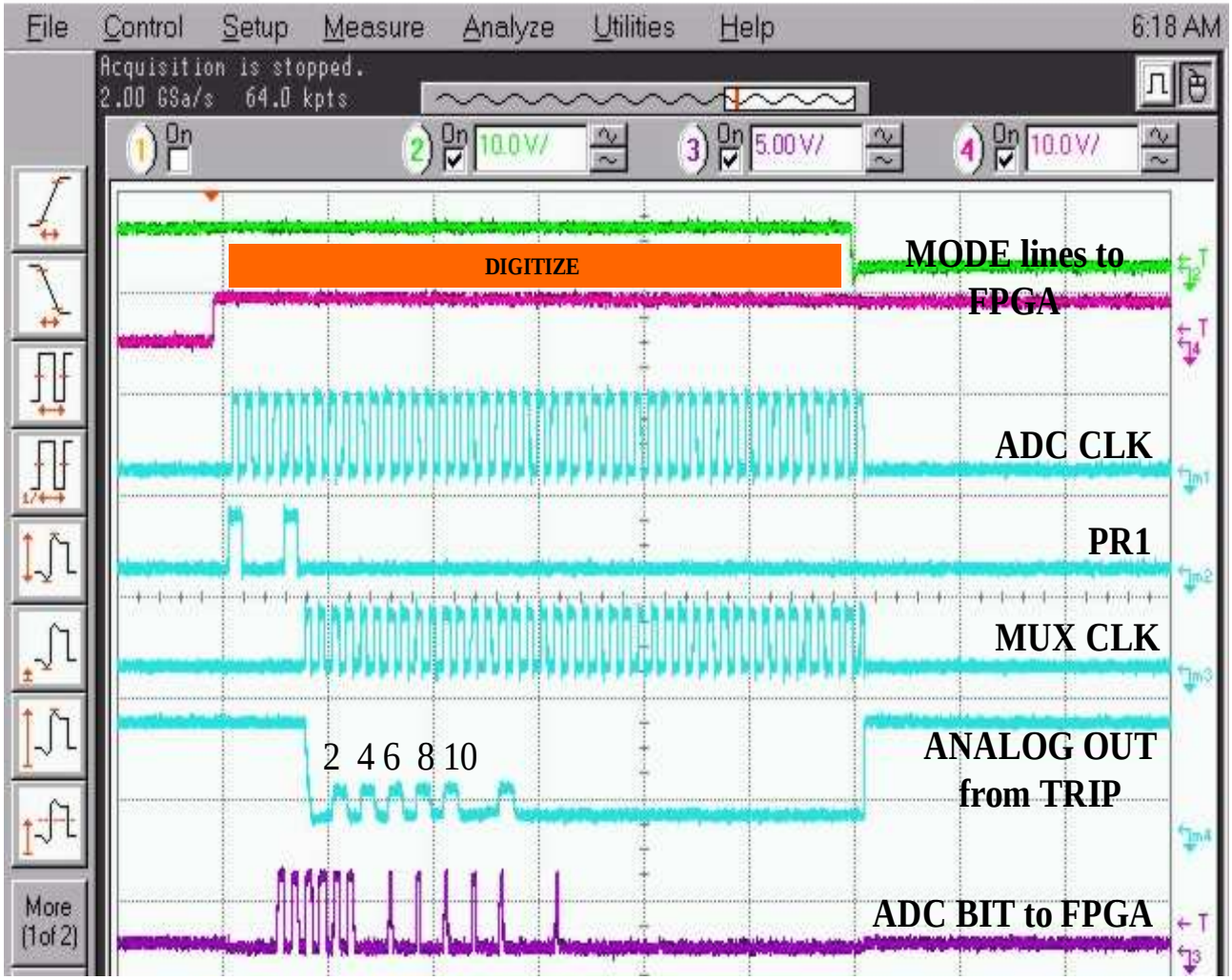

Figure 8: The two top signals in this picture are set by the SASeq and determine the mode for the MCM (green=Mode 0, purple= Mode 1). The system is in ACQUIRE mode until the purple MODE1 raises and starts the DIGITIZE mode, in which the analog output if presented to the AD9201, digitized and read by the FPGA. The ADC clock (3rd signal from the top) starts running in DIGITIZE mode, and the MUXCLK signal starts the analog output of the TriP. One can also see in the picture the ADC output as seen by the FPGA after the digitization was done.

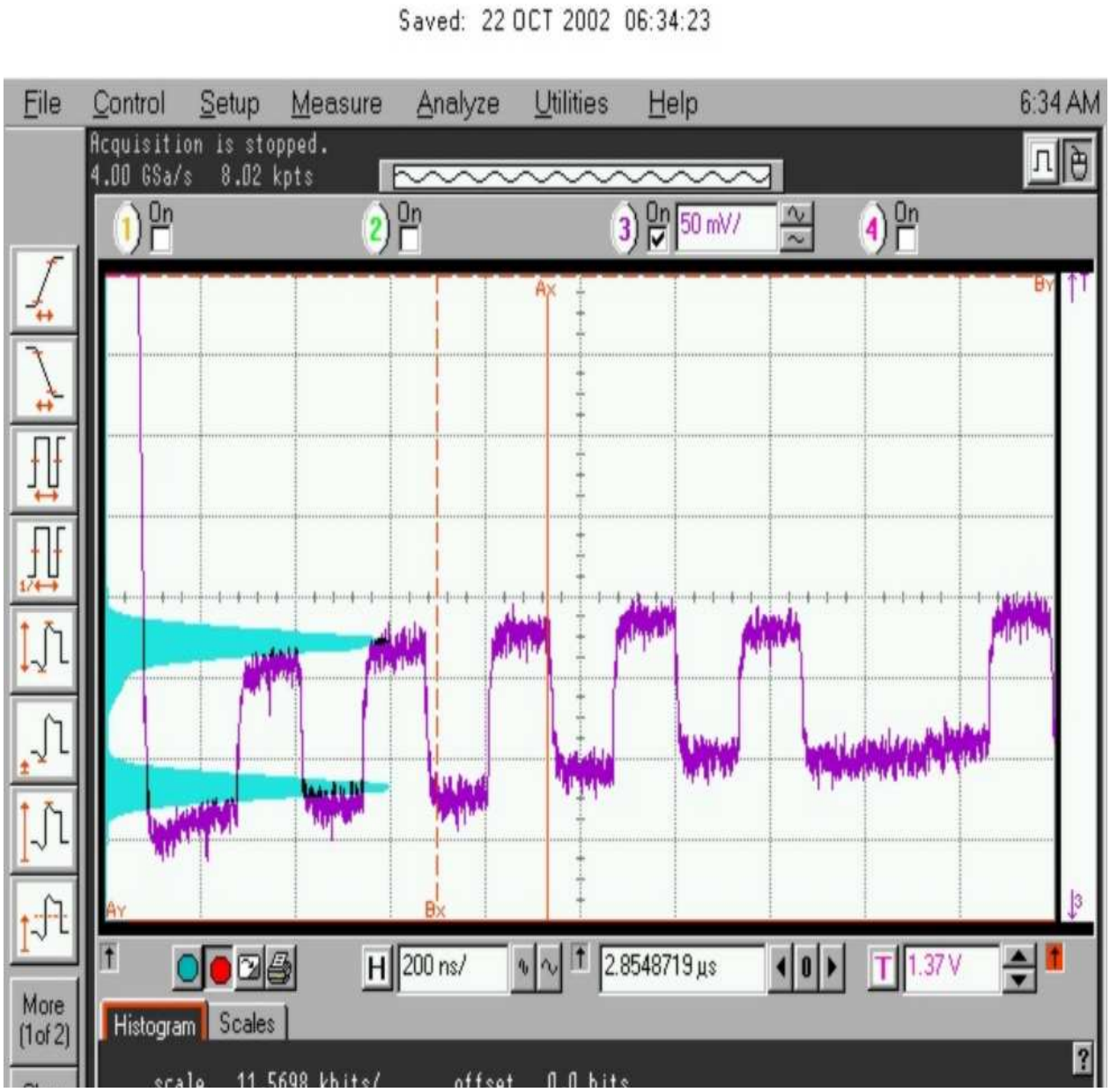

Figure 9: Noise in the analog readout at the imput of the ADC. Input charge 10fC corresponds to approximately 100 mV at the analog output, the observed with at the analog output of the TriP is 25 mV.

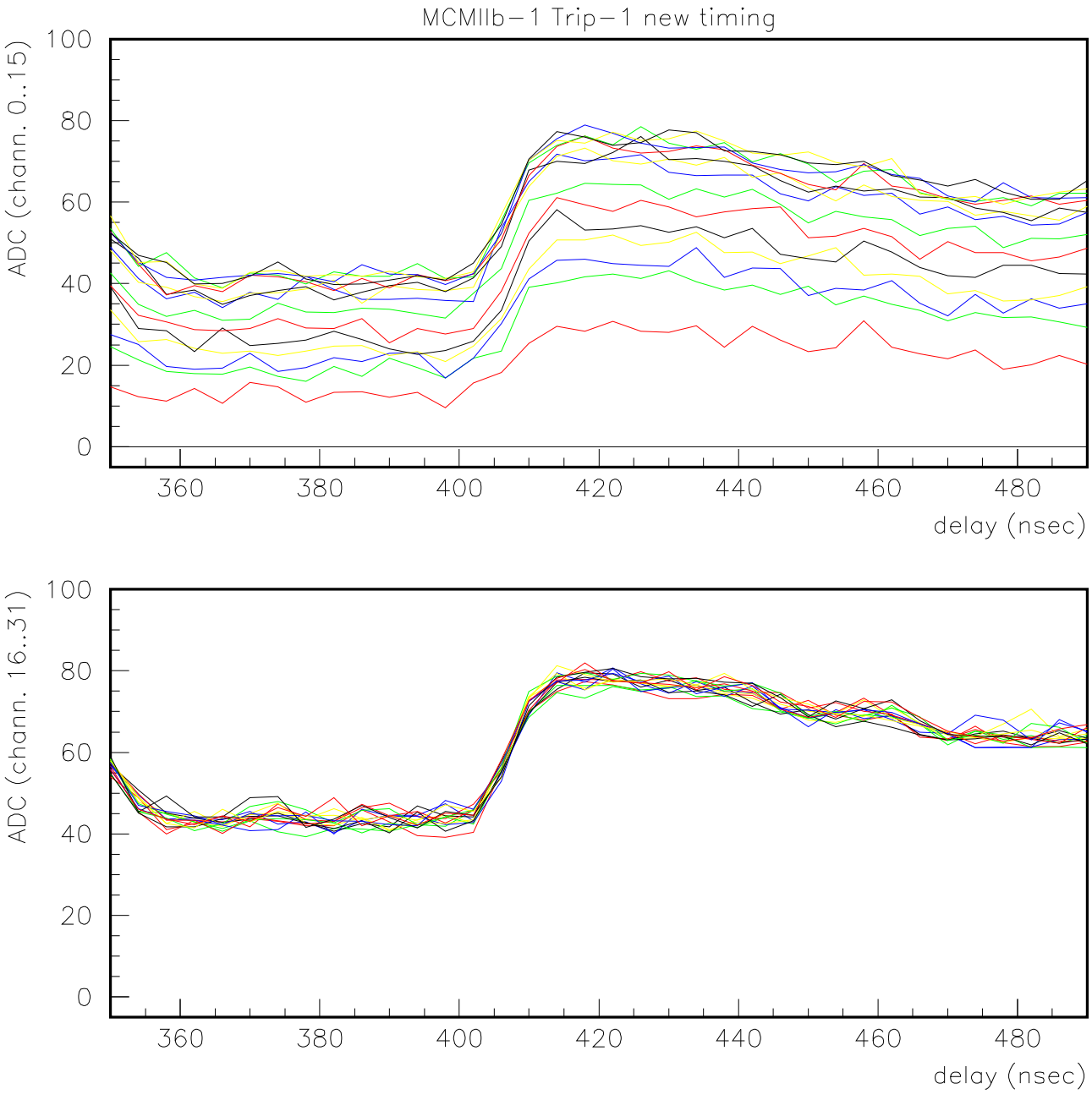

Figure 10: Analog output for timing scan in MCMIIb-1-Trip1

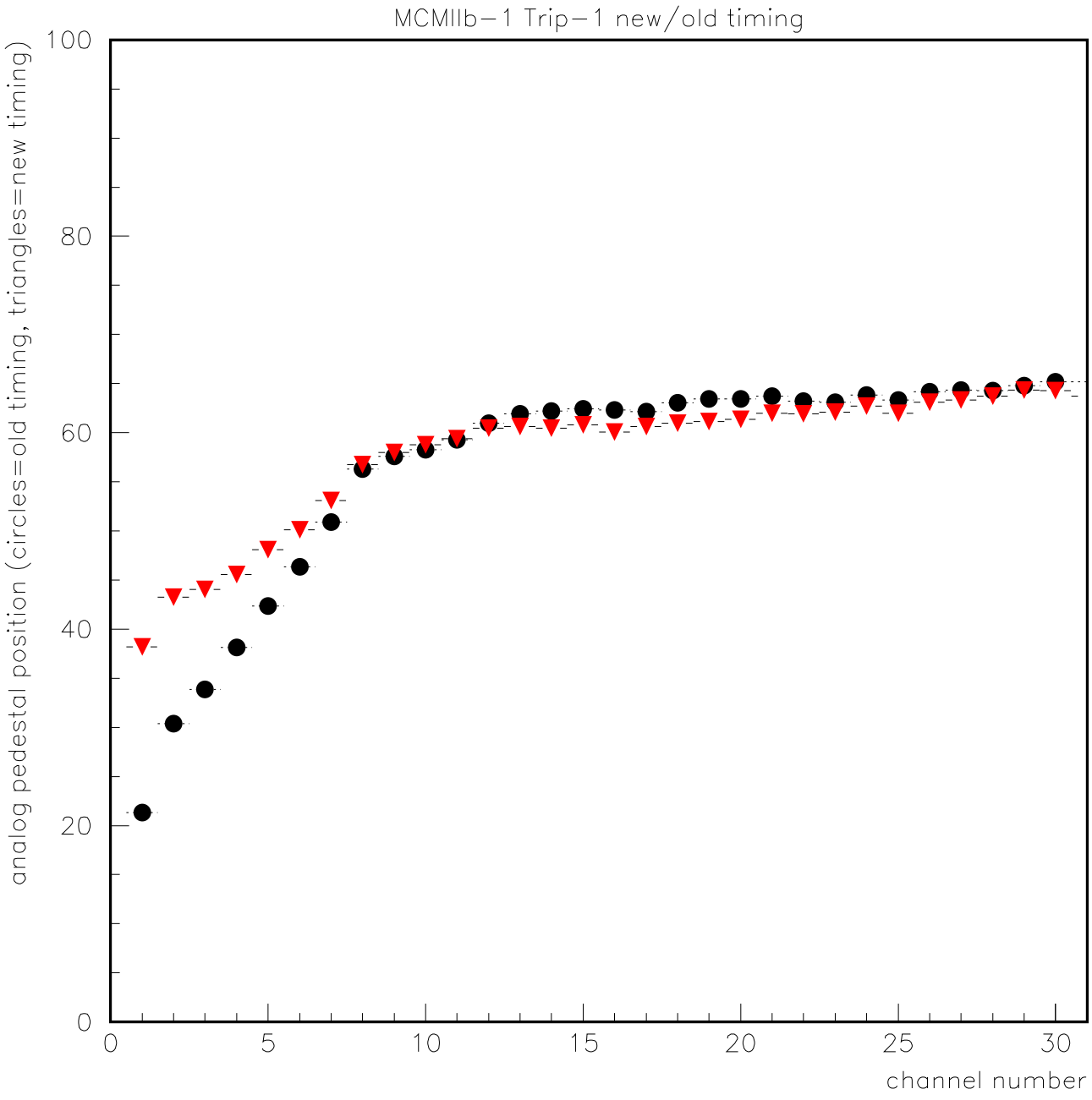

Figure 11: Analog pedestal position for the 32 channels in MCM1-trip1 for the new timing and the std timing

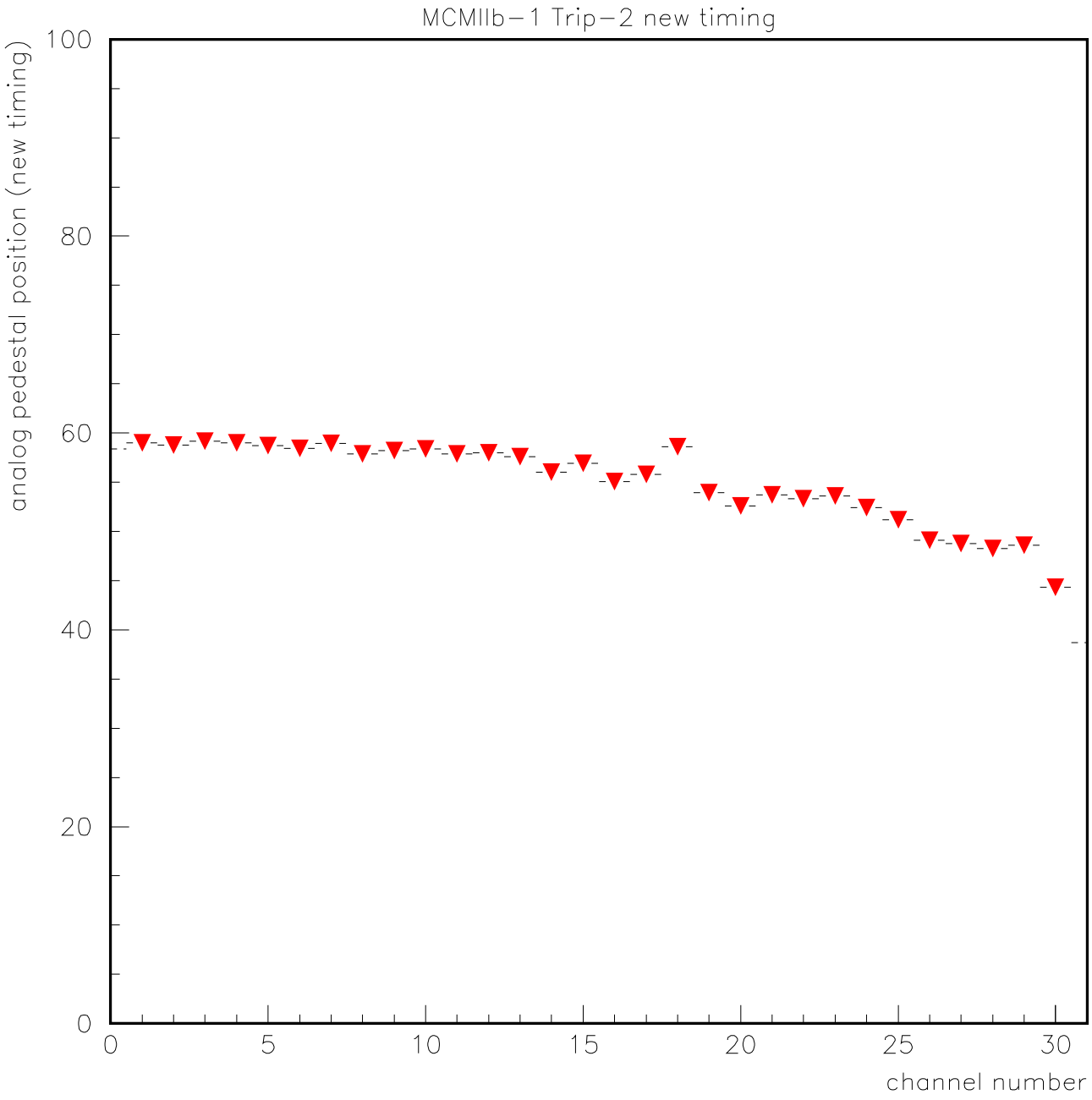

Figure 12: Analog pedestal position for the 32 channels in MCM1-trip2 for the new

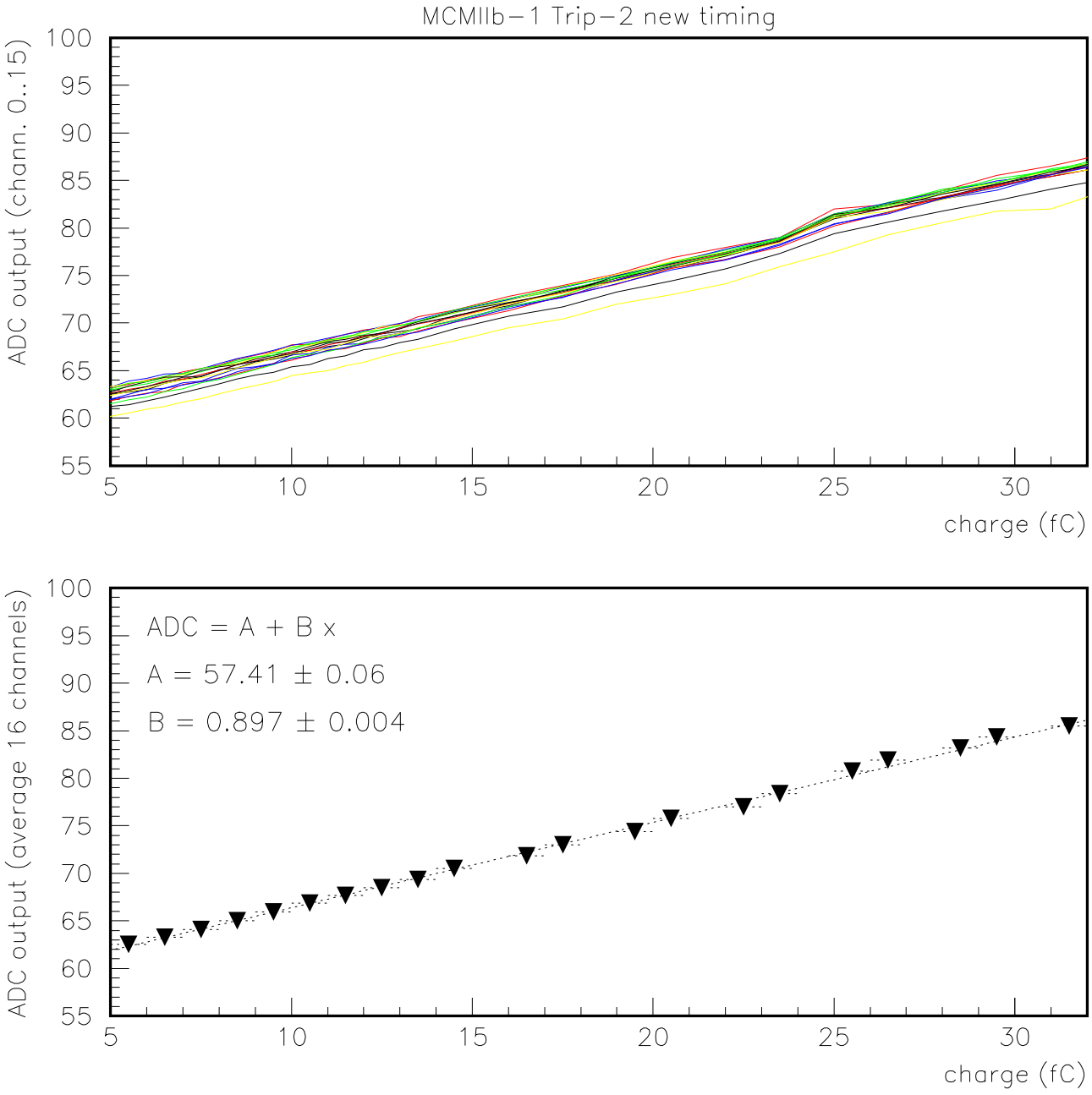

Figure 13: Calibration of ADC readout. The upper plot shows tha analog readout for different cvalues of the injected charge, for 16 channels in MCMIIb-1-Trip2. The lower plot shows the average of the 16 channels, together with a linear fit giving the calibration constant $B = (0.897 \pm 0.004)$ counts/fC.

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3.1 Summary of the Analog Readout

- The analog readout functionality of MCMIIb and MCMIIc have been tested succesfuly. Figure 9 shows a change of 100 mV in the analog output for an input charge of 10 fC (this data is taken at the higest gain settings). As expected, the analog readout for the delay scan shows fast turn on (≈10 nsec) and a slow decay (see Fig. 10).

- MCMIIb-1-Trip1 has a significant spread in the analog pedestals that can be seen in timing scan in Fig. 10 or in Fig. 11. The structure of this pedestal spread points to a possible issue in the layout of MCMIIb for Trip 1. Trip2 does not show this large spread in the analog pedestal.

- The calibration curve shown in Fig.13, shows a good linearity response of the ADC and gives the calibration constant of $B = (0.897 \pm 0.004)$ counts/fC.

4 Timing Options for the Operation of the TriP

As mentioned in Section 1, from the previous studies discussed in [1], we have two options for the operation of the TriP chip.

Option (A) (or standard) has always one discriminator output bank enabled, and it prevents the TriP from having to swing all 16 channels at once, as happens in Option (B) (or new) when both banks are disabled at the same time (see Table 2). In order to understand the performance of the discriminators for this two operating options, we performed discriminator scans on MCMIIb-1 for Option (B). The results are shown in Figs. 14 and 15. The delay for the charge injection pulse was also scanned and the results are presented in Fig. 16.

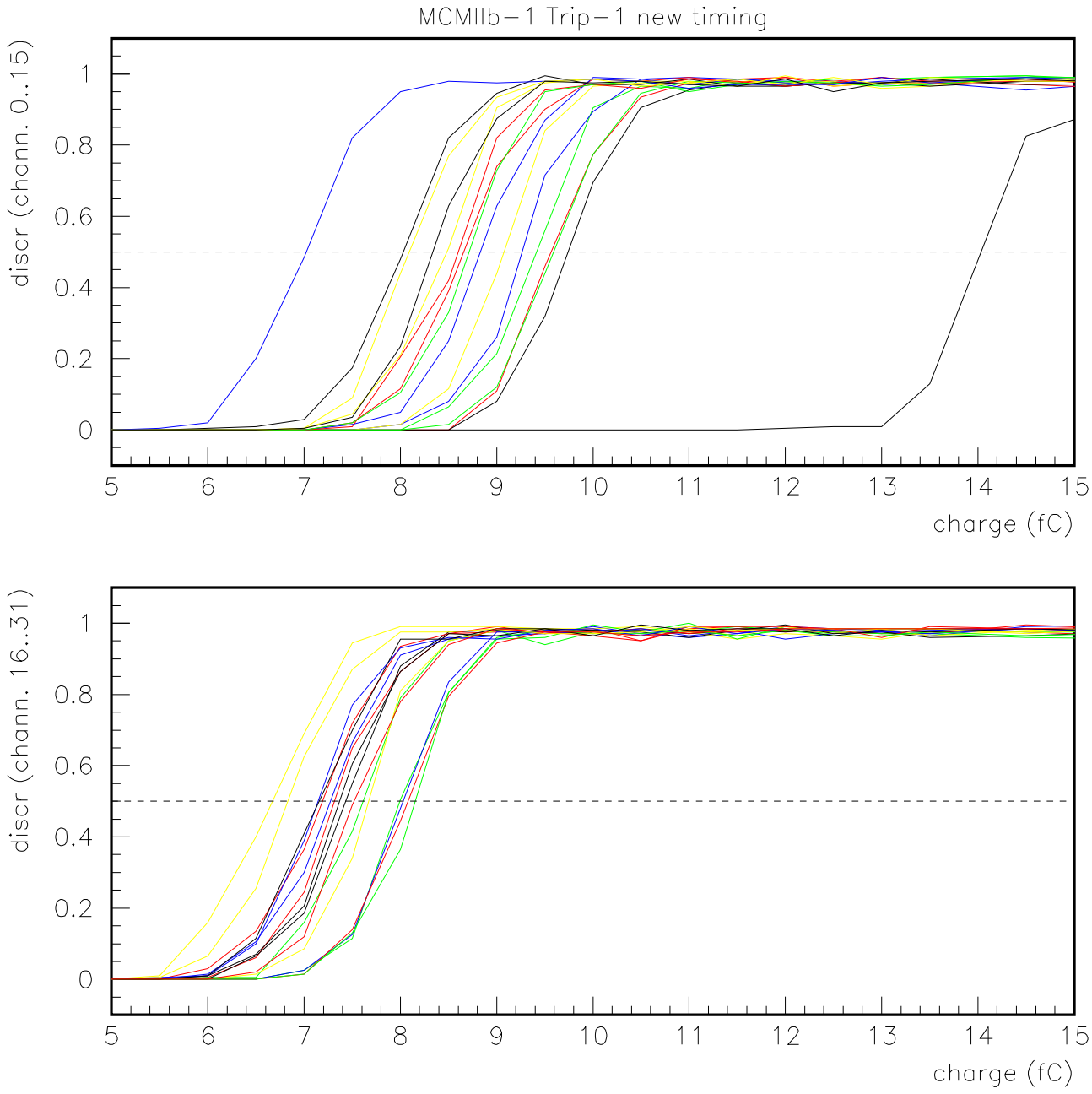

Figure 14: Discriminator scan for MCM1-trip1, for Option (B)

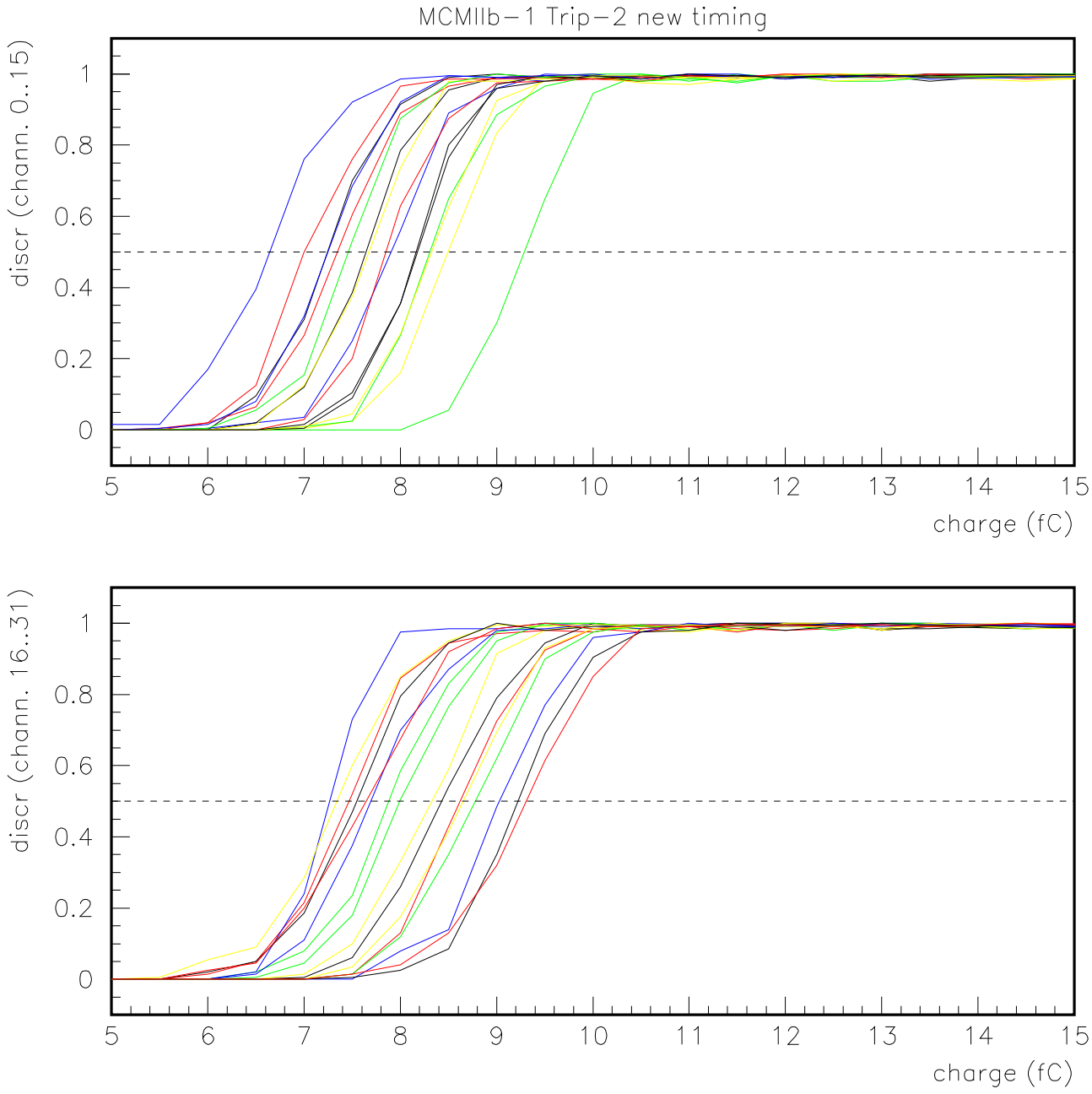

Figure 15: Discriminator scan for MCM1-trip2, for Option (B)

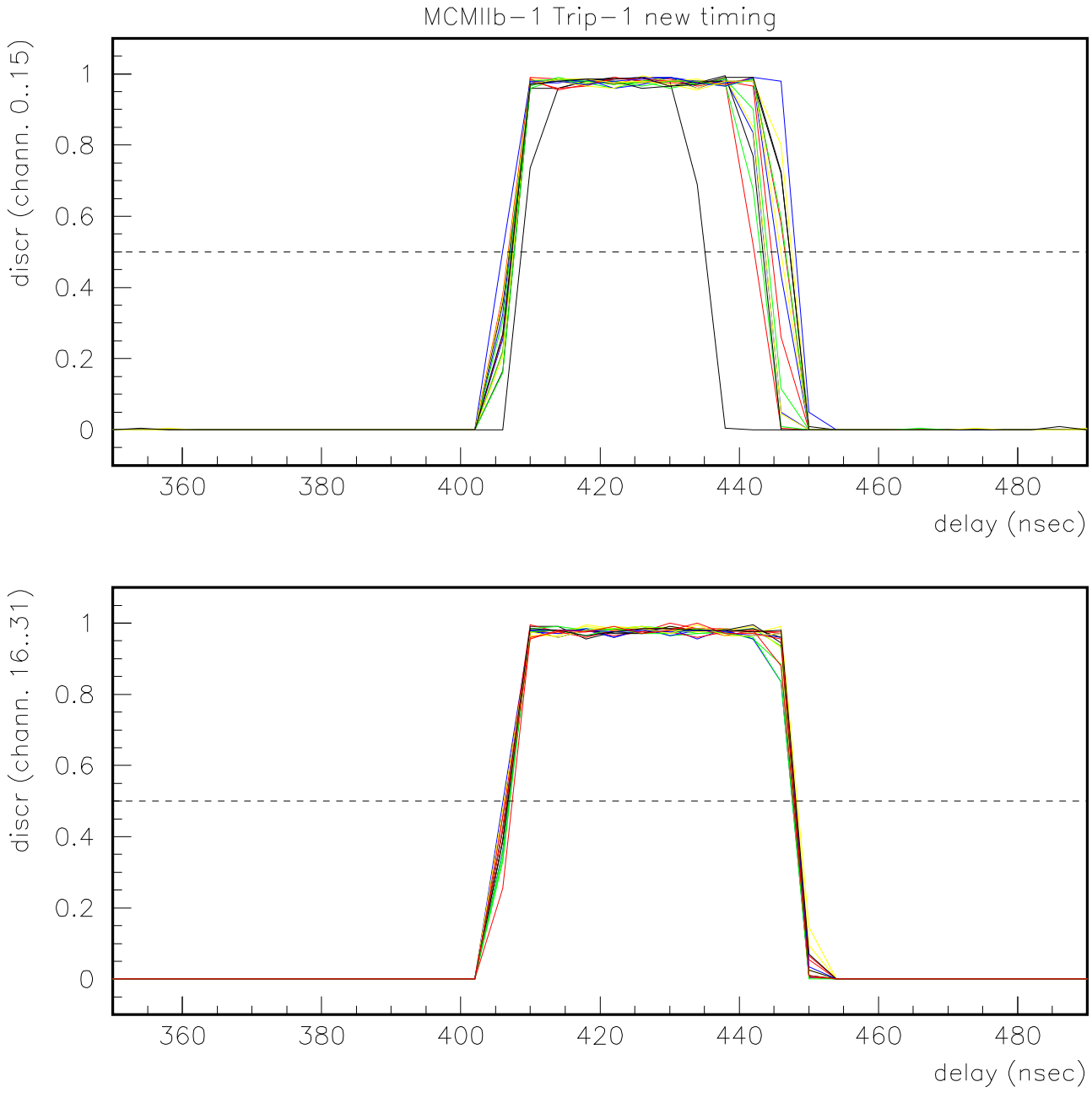

Figure 16: delay scan for MCM1-trip1, for Option (B)

4.1 Summary for Timing Options.

- The studies done in this section indicate that both timing option are well within the specifications for the desgin of the TriP chip. We observe slighty less spread in the discriminators for Option (B). However, the final decision on which operating mode to select for the experiment has to be done in the basis of real signal, that is, the TriP chip reading out signals from the VLPC cassettes.

- Option (B) does not solve the problem with channel 0 observed with Option (A) in Section 2. Option (B) does not help with the analog pedestal spread observed in MCMIIb-1-Trip1 in Fig.11.

5 Effect of a 25 fC Pulse an Earlier bucket.

All the tests done in earlier sections of this note were done injecting one pulse every 7 μsec. In this section we investigate the effect of a pulse in the previous bucket (132 nsec earlier than the charge injection that we are reading out). The discriminator occupancies as a function of the injected charge in the readout bucket are shown in Fig. 17, with and without a 25 fC pulse in the earlier bucket. It can be seen from this study that the pulse in the earlier bucket moves the discriminator turn-on by approximately 1 fC. This effect has to be considered as an extra spread in the discriminator curves.

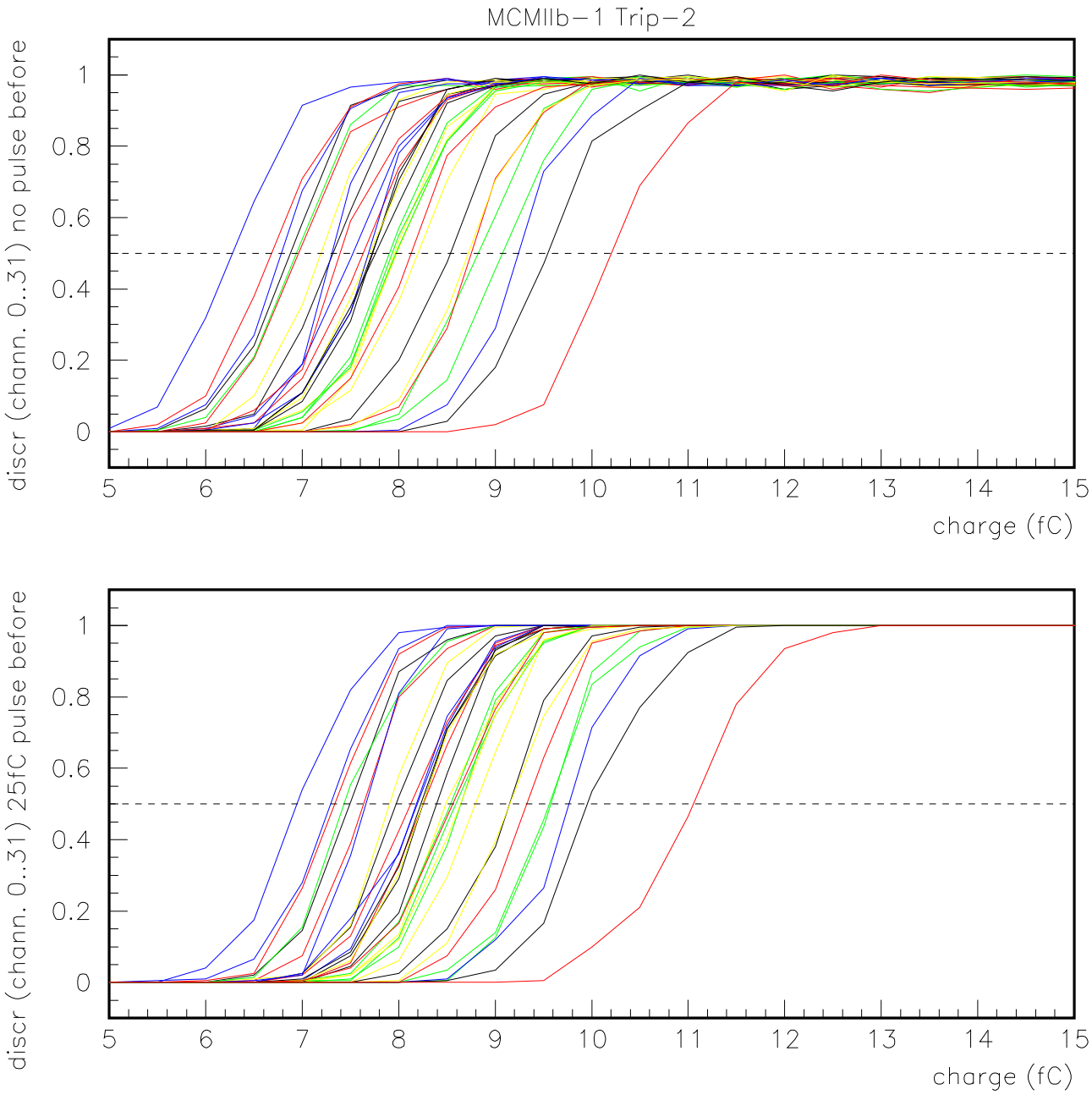

Figure 17: pulse before

6 Effect of 33 pF Coupling to Ground.

All the tests done so far have been based on TriP chips with nothing connected to their inputs. In the real application, we expect between 30 and 40 pF of stray coupling to ground (mostly due to the flex circuit). For this reason, the final characterization of the operation of the TriP chip will be done connecting the input to VLPC channels at DØ.

In our test stand we simulate the conditions at the detector by connecting 33 pF capacitors in the input of the AFE, where the MCM with the TriPs is mounted, and connect the other end of this capacitors to ground.

The charge injection scan were then repeated for MCMIIb-1-Trip2 with this new configuration and Option (A), The results are presented in Fig.18 and a comparison is done for the same TriP without the 33 pF coupling to ground. The distributions of analog pedestal were also studied in this new configuration and the results are presented in Fig. 19.

In order to understand any differences between Option (A) and Option (B) for this new configuration, we repeated the charge injection scan for Option (B), the results are presented in Fig. 20.

We also performed a delay scan with this new configuration and Option (A) and the results are shown in Fig. 21. Based on this scan we did a charge injection scan with 2 different values of the delay $d_1 = 350$ nsec and $d_1 = 370$ nsec, the comparison between these two scans is shown in Fig. 22.

6.1 Summary of the of 33 pF Coupling to Ground.

- The 33 pF coupling to ground deteriorates the performace of the TriP chip in Option (B) beyond the desgin specification. The spread in the discriminators turn on curve becomes more than 10 fC. This will have to be confirmed with VLPCs connected at the input of the TriP, but seems to indicate that this is not a working operating mode (see Fig. 20).

- The spread in the discriminators turn on curve is still within the design specifications when the 33 pF coupling is present and the TriP is opetated in Option (A), the spread in this case in less than 6 fC (see Fig.19).

- The analog pedestal spread is acceptable with the 33 pF coupling using Option (B).
- The analog pedestal spread is acceptable with the 33 pF coupling using Option (A).
- The 100% efficiency window is of the 40 nsec, with 33 pF coupling and Option (A).

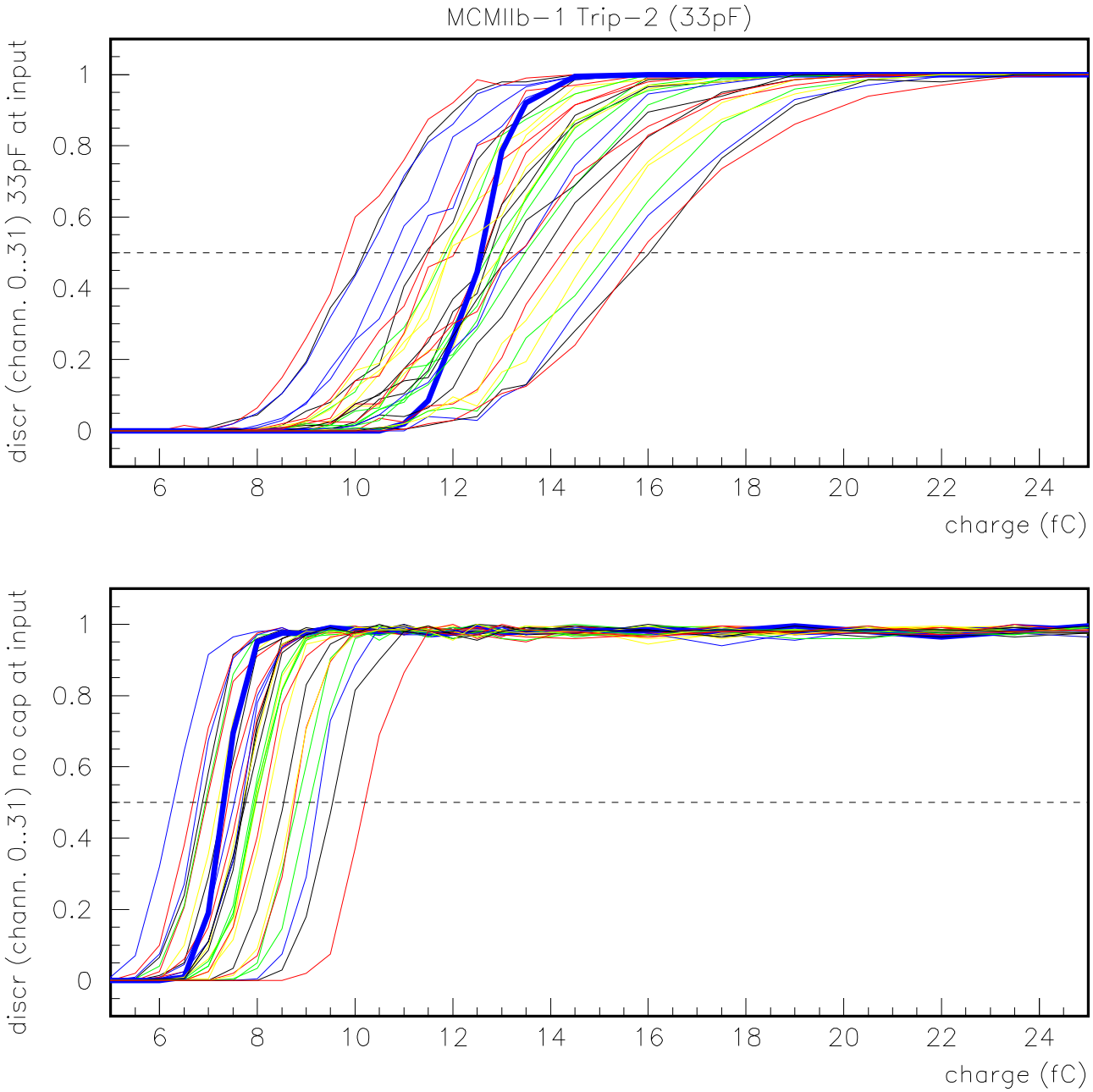

Figure 18: Comparison of the discriminators turn on curve for MCM1-trip2, with the coupling capacitors (33fC) and witout them.

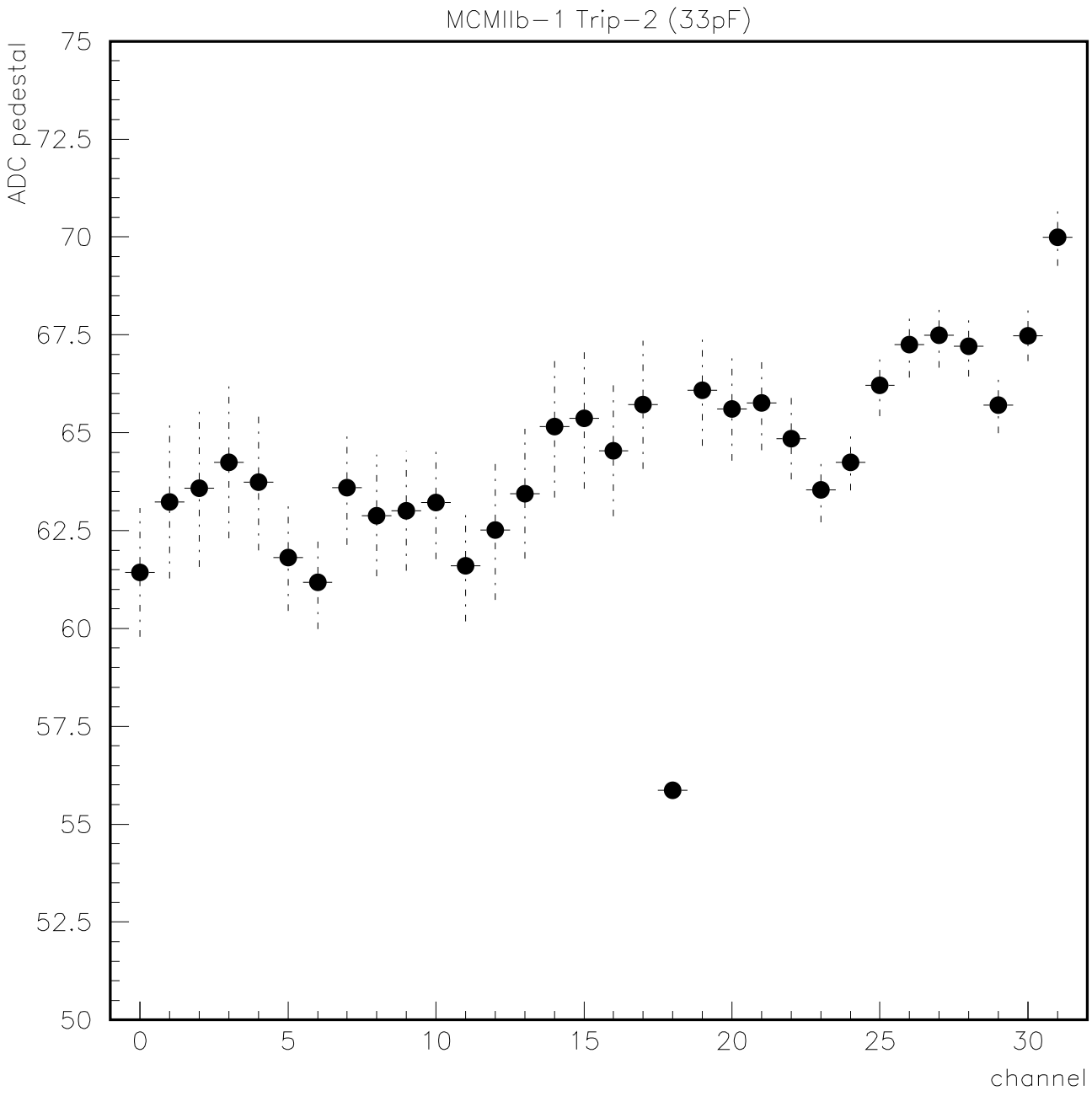

Figure 19: Analog pedestal for MCMIIb-1-Trip1 wih 33pF coupling to ground.

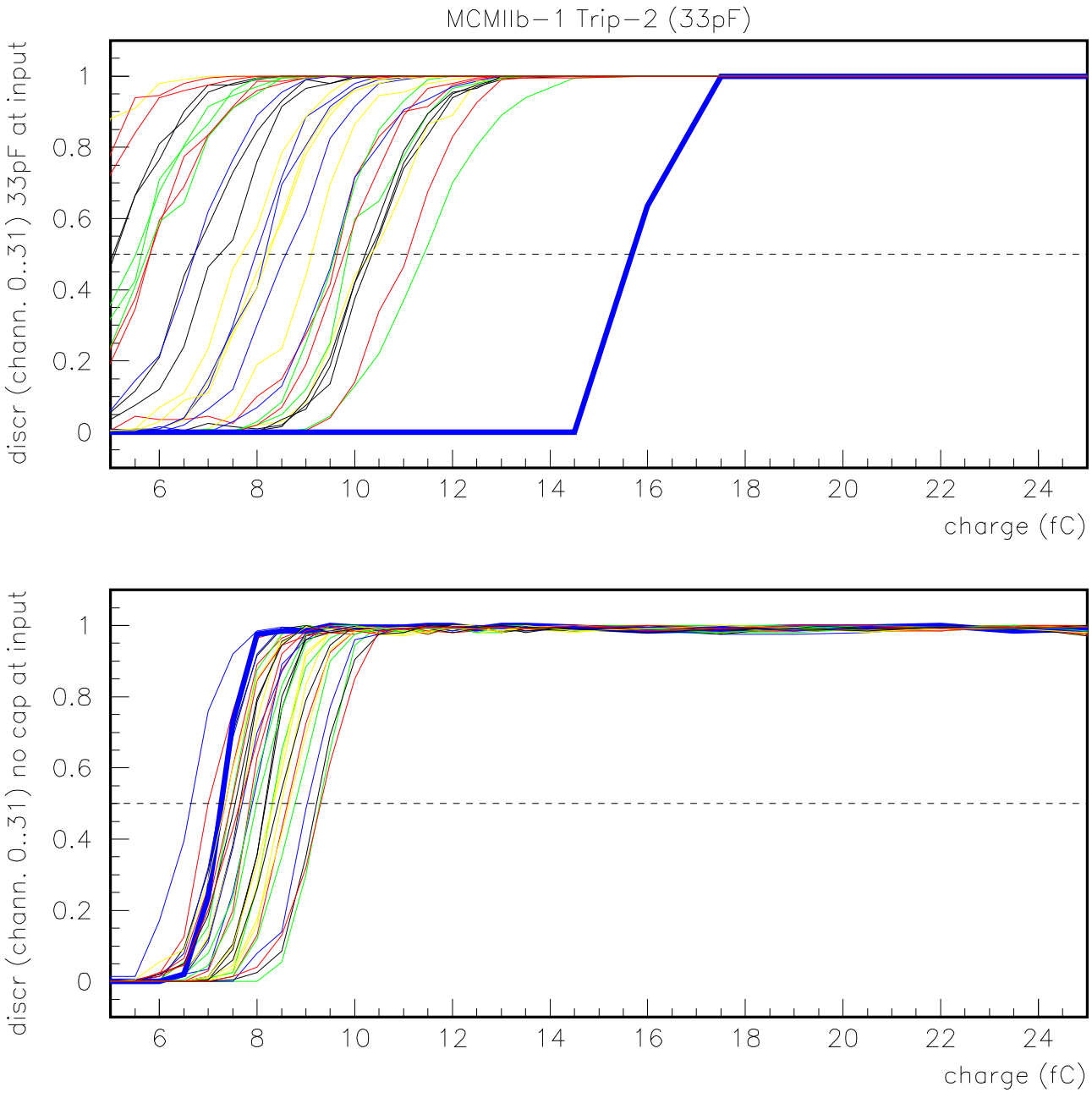

Figure 20: Same as Fig.19, but using Option (B).

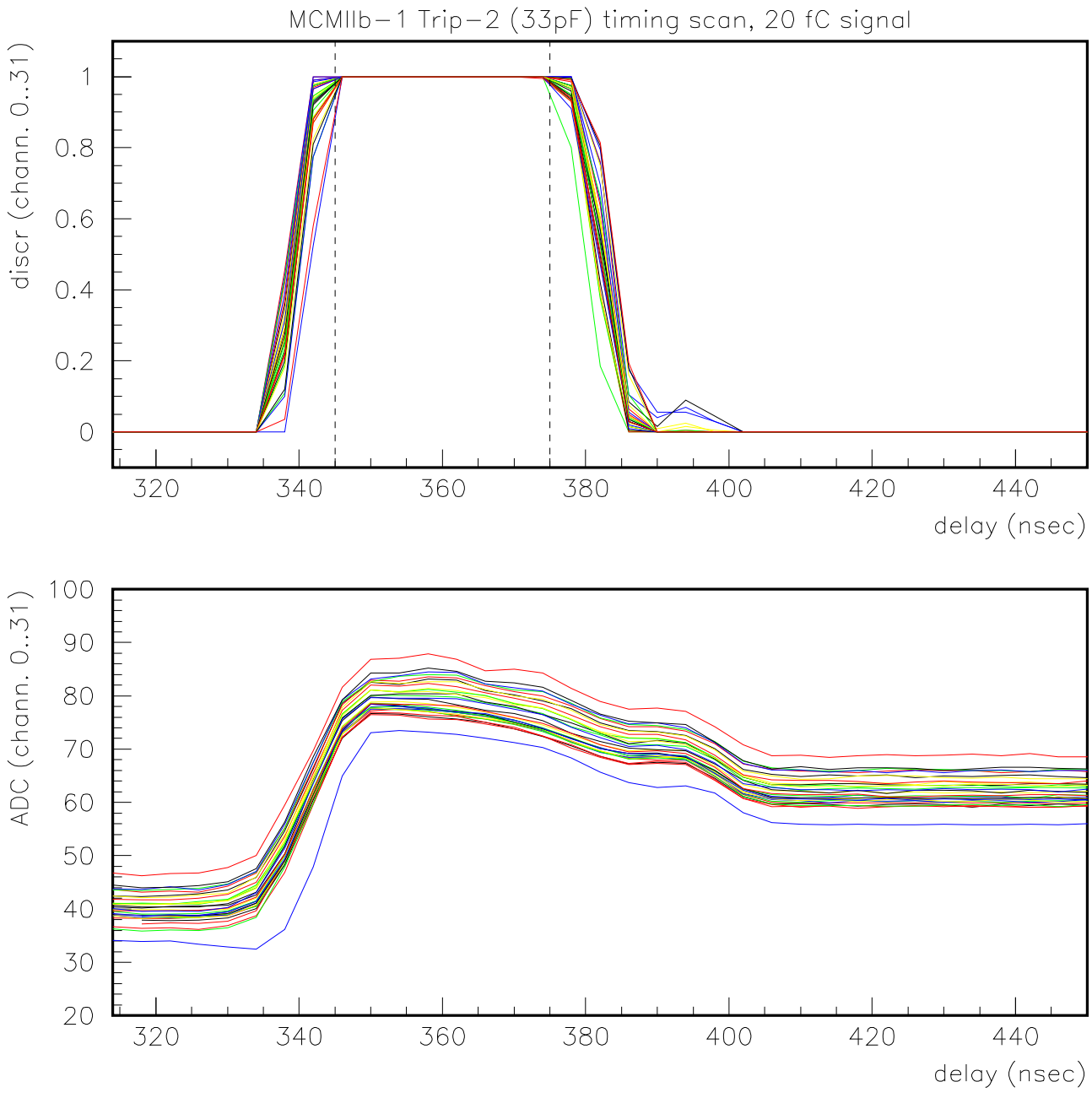

Figure 21: Timing scan for MCMIIb-1-Trip1 with 33pF coupling to ground.

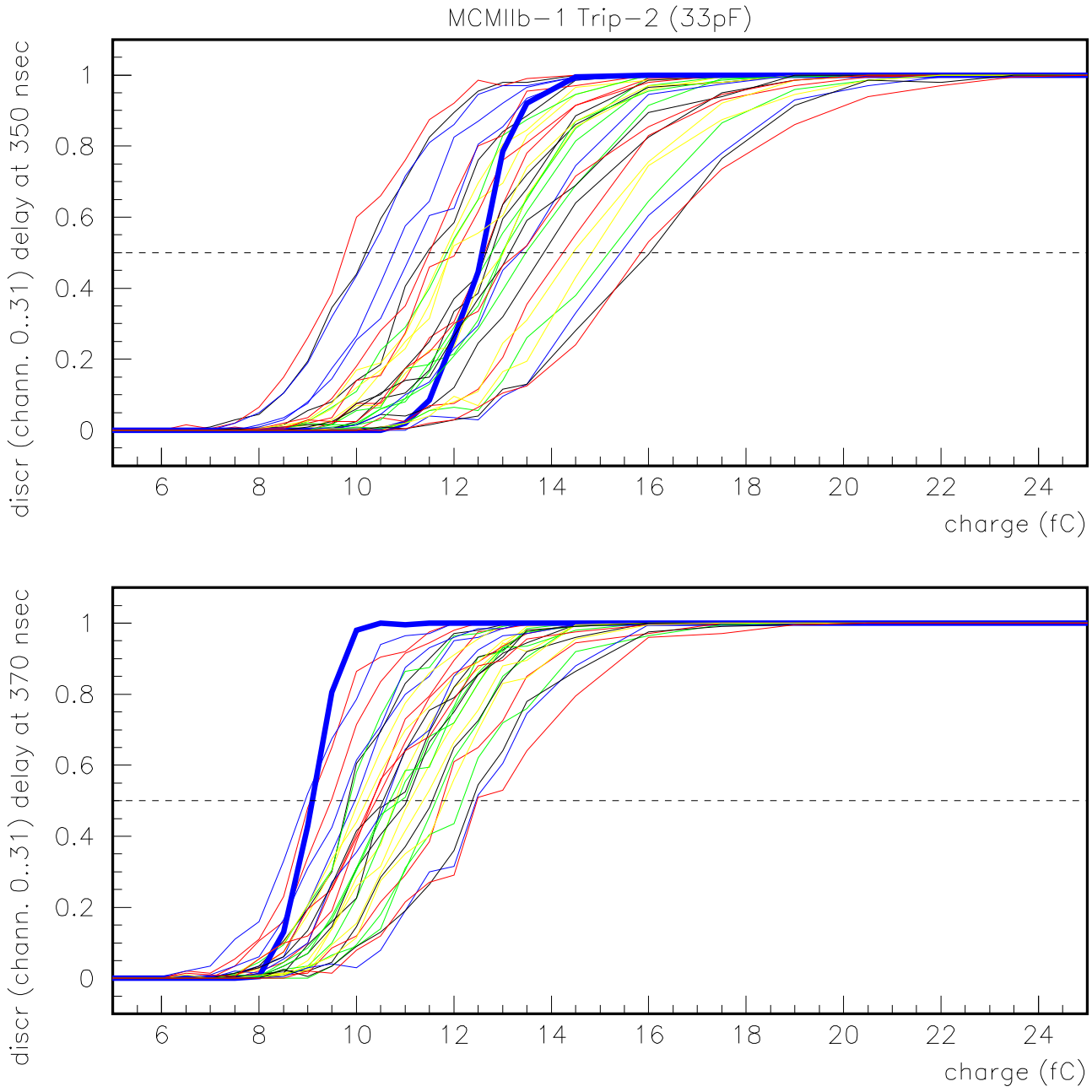

Figure 22: Comparison of the discriminators turn on curve for MCMb-1-trip2 with 2 diff values for the delay.

References

[1] "MCM II and the TriP Chip", J. Estrada, C. Garcia, B. Hoeneisen and P. Rubinov, FERMILAB-TM-2226.