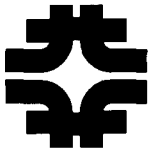

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Capacitor Mismatch Caused by Oxide Thickness Variations in Submicron I.C. Processes

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Capacitor Mismatch Caused by Oxide Thickness

Variations in Submicron I. C. Processes

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3/3/99

In the high energy physics community, chips are often designed which contain large arrays of capacitors. This is usually due to the fact that many identical channels are placed on one chip. For example, each channel may have a capacitor used as a feedback element to set the charge gain of an integrator. In many cases, it is highly desirable to have the capacitor values match as closely as possible. Unfortunately, a good share of the processes which are available to us do not have explicit capacitor structures built in (such as double poly). Some processes, such as HP 0.5u, do have an NWELL thin oxide capacitor structure available, but this capacitor may not be stable enough due to its linear and quadratic voltage coefficients. The value of this capacitor can change by a few tenths of a percent or even up to one percent depending on the voltage across it. As a result, many times we are forced to use interconnect layers to build good quality capacitors. A typical example is a sandwich of poly-metal1-metal2 in which one plate is the metal1 layer and the other plate is the poly and metal2 layers in parallel.

In the past, the matching in large arrays of capacitors formed from interconnect layers has proven to be quite good, indicating that field oxide thicknesses remain essentially constant over different areas of the chip. This experience is based on designs which use 0.8u or larger dimension processes. In 1995, an amorphous silicon detector array readout chip (MASDAR) for medical imaging was designed at Fermilab for researchers at the University of Michigan. MASDAR was fabricated in the HP 0.8u process and contains a large array of poly-metal1-metal2 capacitors as integrator feedback elements. Matching of these capacitors is quite acceptable and no systematic variation across the chip is seen. Recently, an updated and improved readout chip, MASDAX, was designed and fabricated in the HP 0.5u process. The move to smaller dimension process was made since the "older" processes (such as HP 0.8u) will soon be unavailable to us. Quite unlike MASDAR, MASDAX shows a substantial systematic variation in capacitance across the chip. Figure 1 shows the layout of the MASDAX chip. The capacitors at the edge of the array have a value which is 10% higher than the capacitors in the middle of the array. Figure 2 shows an oscilloscope photo of the readout of all channels of the chip after an identical charge is injected into the integrators of all channels. The height of the scope trace is proportional to the inverse of the integration capacitance. As can be seen, the capacitance at the edges is significantly higher, about 10%. Even more striking is how far this effect extends into the interior of the array. Moving in toward the interior of the array, the capacitance gradually decreases and reaches the nominal "interior" value only after moving about 1500 microns in from the array edge!

Initially at a loss to explain this effect, we sent a chip to a focused ion beam (FIB) service to have cross sectioning of capacitors performed at the edge of the array and in the interior. Figure 3 is the cross section of the Channel 1 capacitor on the array edge, and Figure 4 is the cross section of the

Channel 18 capacitor, which is close to where the capacitor value stabilizes. By comparing these two pictures, it is obvious that the difference in capacitance is caused by oxide thickness variation. The thickness of metal and poly layers is equal in both cases, but the poly-metal1 and metal1-metal2 oxides are about 10% thinner at the edge.

A conversation with Dr. Vance Tyree at MOSIS helped to explain this situation. A method called chemical-mechanical polishing (CMP) is used after oxide deposition to planarize the chip surface in preparation for depostion of the next layer. This method is not the equivalent of simply grinding down the oxide surface so that it is perfectly flat. A combination of chemical and mechanical methods are used to achieve as planar a surface as possible. In larger dimension processes, an approximately flat oxide surface is obtained with little dependence on what lies below it. However, as the process dimension shrinks, the contour of the oxide surface becomes much more sensitive to the average density of the interconnect layer below it. This gives rise to rules for submicron processes which specify that the local average density of metal and poly layers must be within certain bounds. Large variations in interconnect density will give rise to significant oxide thickness variations. This effect apparently becomes much more pronounced as the process dimension shrinks.

HP has instructed MOSIS that for the 0.35u and smaller processes, the density rules must be followed. Unfortunately, MOSIS is not allowed to communicate to us exactly what these rules are, since it is considered proprietary. Thus MOSIS actually goes into submicron designs which are submitted to them and adds metal/poly as required in blank areas of the chip in an attempt to meet the density requirements. For the 0.5u process, HP makes no such requirement of MOSIS. However, according to MOSIS, density related effects definitely do occur on this process, but HP has allowed them to ignore the density rules since the effects in this process are not extreme and the main result will simply be somewhat lower yield. Since MOSIS is considered a prototyping service, a somewhat lower yield is considered acceptable and MOSIS is allowed to "squeak by" on this process without addressing density rules. Dr. Tyree states that HP has told them that for a large density discontinuity, oxide thickness variation effects can extend up to 1500 microns. This is in fact exactly what we observe on the MASDAX.

In summary, chip design in submicron processes will present new challenges and problems which were not present in designs with larger dimension processes. One effect in the newer processes is the field oxide thickness variation due to interconnect density variations. This effect becomes much more extreme for the smaller dimension processes. Large density discontinuities can cause lower yield and will also result in capacitor value mismatch over substantial distances from the edges of a large array when using poly/metal capacitors. If good matching in this type of large area capacitor array is required, the only way to achieve this is to guarantee nearly constant metal/poly density for at least 1500 microns (this distance will likely depend on the process) around the edges of the array. If the array boundary is close to the chip edge, then dummy capacitors should be placed up to the chip edge, and another layout with similar density must be placed as close as possible to the relevant edges of the chip in the reticle. When using a standard MOSIS reticle size, this may entail placing dummy chip layouts around the chips of interest in order to guarantee that identical density exists for the required distance outside of any chip's borders.

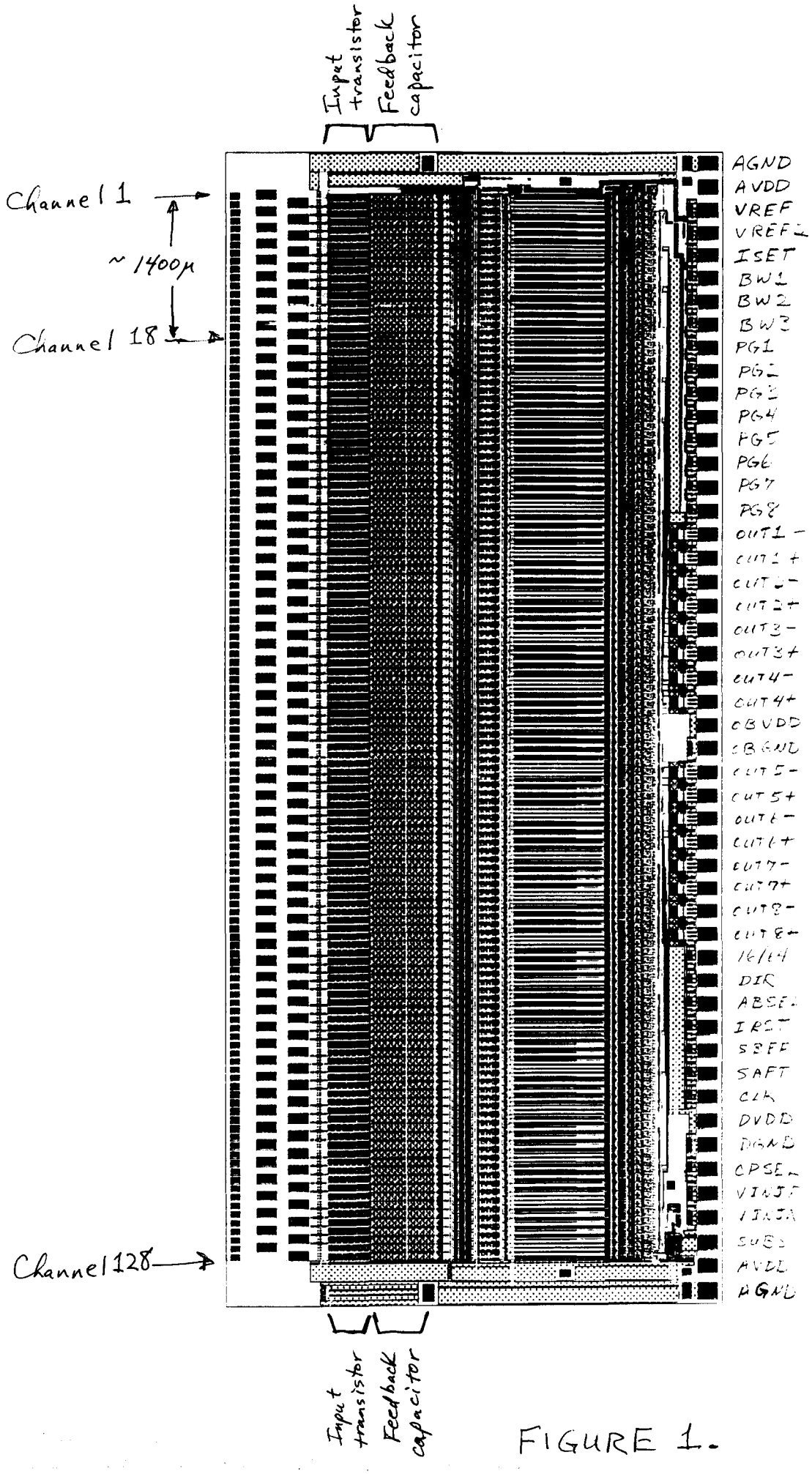
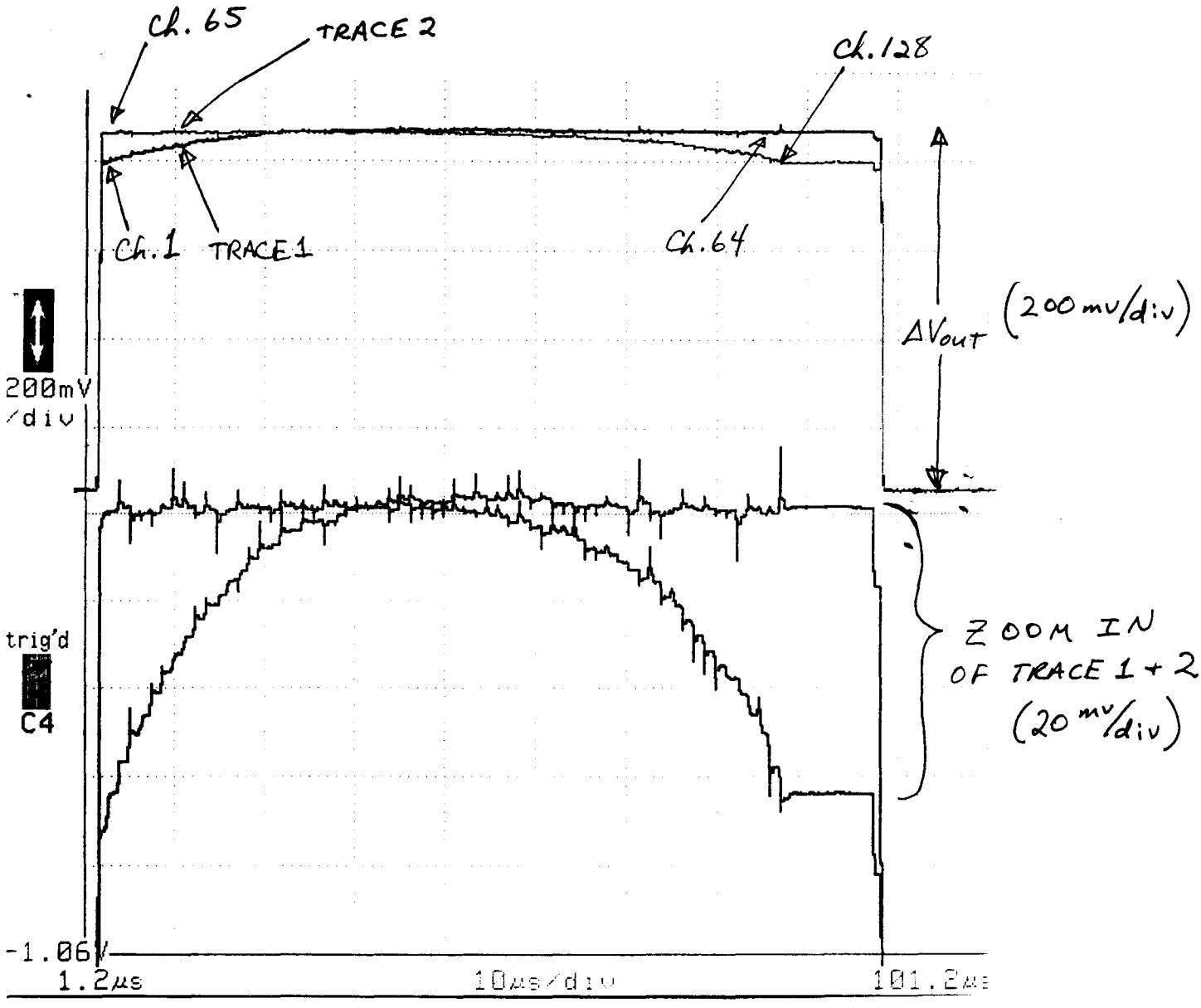

Input transistor
Feedback capacitor
Channel 1
~ 1400μ
Channel 18
Channel 128
AGND
AVDD
VREF
VREF-
ISET
BW1
BW2
BW3
PG1
PG2
PG3
PG4
PG5
PG6
PG7
PG8
OUT1-
OUT1+
OUT2-
OUT2+
OUT3-
OUT3+
OUT4-
OUT4+
OBVDD
OBGND
OUT5-
OUT5+
OUT6-
OUT6+
OUT7-
OUT7+
OUT8-
OUT8+
16/14
DIR
ABSEL
IRST
SEFF
SAFT
CLK
DVDD
DGND
CPSEL
VINJT
VINJA
SUBS
AVDD
AGND
Input transistor
Feedback capacitor

FIGURE 1.



ΔVout of all channels in response to charge injection.

TRACE 1 is readout of Channels 1-64.

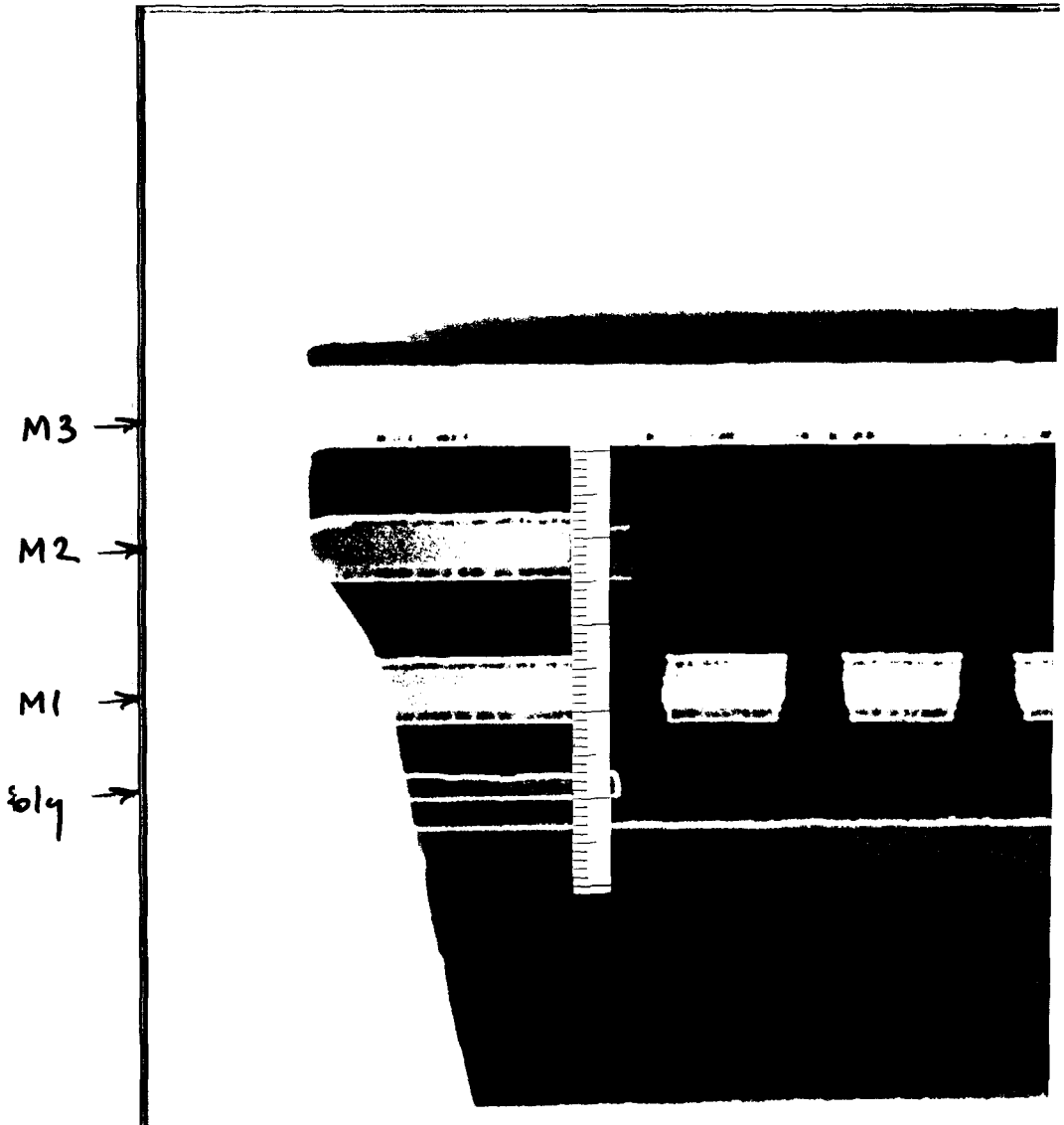
TRACE 2 is readout of Channels 65-128.

Bottom two traces are TRACE 1 and 2 expanded vertically.

FIGURE 2.

FIGURE 3.

Channel 1 capacitor cross section.



Substrate to poly : 0.3μ

Poly thickness : 0.3μ

Poly to M1 : 0.58μ

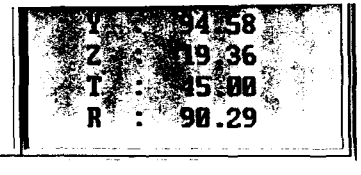
M1 thickness : 0.79μ

M1 to M2 : 0.88μ

M2 thickness : 0.80μ

M2 to M3 : 0.78μ

M3 thickness : 0.93μ



channel 1

Cross Section of MASDA-X capacitor

FIGURE 4.

Channel 18 capacitor cross section.

Substrate to poly: 0.3μ

Poly thickness: 0.3μ

Poly to M1: 0.62μ

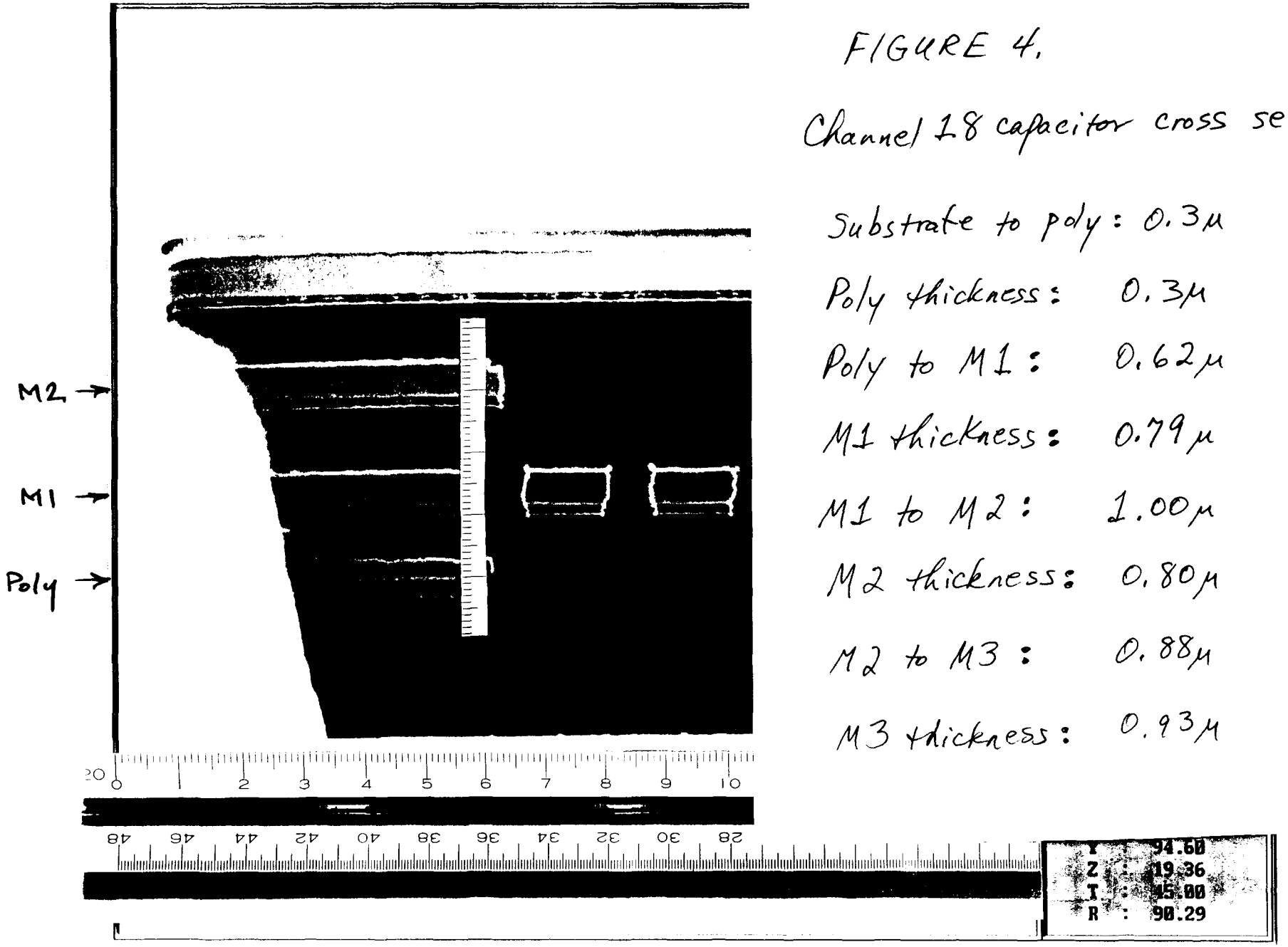
M1 thickness: 0.79μ

M1 to M2: 1.00μ

M2 thickness: 0.80μ

M2 to M3: 0.88μ

M3 thickness: 0.93μ



Cross Section of MASDA-X Capacitor