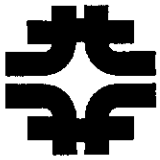

Fermi National Accelerator Laboratory

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A Beginners Guide to the SVXII

Prepared by R. Yarema for the SVXII design Group: I. Kipnis, S. Kleinfelder, L. Luo, O. Milgrome, M. Sarraj, R. Yarema, T. Zimmerman

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INTRODUCTION

In the late 1980's, several versions of a full custom chip called the SVX were built and tested. The chip was designed to be a second generation silicon strip readout chip incorporating new features such as data sparsification for silicon strip detectors. The SVX designed by Stuart Kleinfelder and others at LBL contained 128 channels of electronics and proved to be very popular. Initially the chip was fabricated in 3.0 micron process and later transferred to a 1.2 micron radiation hard process. Based on the success of the first SVX (referred herein as SVXI), a need arose for a third generation device. This new 128 channel device called the SVXII was developed by a collaboration of engineers at Fermilab and Lawrence Berkeley Laboratory. The SVXII, designed in a 1.2 micron process, contains many new features including analog storage and digitization of the analog information. In addition to the new features, the SXVII is intended to operate with interaction times approximately 25 times faster than the original SVX, have the same or better noise characteristics, and have a minimal increase in power. The SVXII is an engineering challenge. This report is a first detailed attempt to introduce the SVXII to the user. Knowledge of the original SVX and its operation would be helpful and can be obtained from references 1-3.

GENERAL OVERVIEW

Design and Layout Philosophy

The SVXII was designed to meet the silicon strip upgrade requirements for both the CDF and D0 experiments at Fermilab. A major requirement was that the device be capable of operating at an interaction rate as fast as 132 nsec. Another criteria was that the readout device have optimal performance for detector capacitances between 10 and 35 pf. To accomodate the various interaction rates and input capacitances, the chip may be externally programmed to have optimal performance for any interaction time from 132 to 396 nsec and any capacitance from 10 to 35 pf.

In early discussions, members of both CDF and D0 agreed that an on chip analog pipeline with a delay of about 4 usec was necessary to allow time to form a trigger signal. Also, experimenters agreed that a deadtimeless data acquisition system was not necessary since readout of the remainder of the detector required a long deadtime. When a trigger signal is sent to the SVXII, data acquisition stops until the chip is completely read out. Separate acquisition and readout cycles allow a reduced silicon area on an already overcrowded chip and significantly reduce the problem of coupling from the digital output section to the very sensitive analog input.

To improve the readout speed and accuracy, an on chip ADC is provided on the SVXII. Both a single ADC and multiple ADC options were considered. The added power dissipation for the chip was minimized by using a separate Wilkenson type ADC for each of the 128 channels. The maximum number of bits (8) in the ADC is determined by the time required to digitize a signal, the dynamic range of the input signal, and the accuracy of digitization required to obtain the desired track resolution.

Accuracy of the digitized signal could be compromised by pileup in high occupancy situations. A switched capacitor approach was adopted for the integrator and analog pipeline design to avoid pileup problems. Reset time of the amplifiers is a real concern in switched capacitor designs. The problem was circumvented by performing preamplifier (integrator) resets during the major beam gaps which exist in the Fermilab beam structure and resetting the pipeline amplifier every interaction interval. Operation of the amplifiers is discussed in greater detail later.

Silicon strip detectors are intended to provide high resolution track location. In order to obtain high resolution, the detector must have a high degree of mechanical stability which can only be achieved with low power dissipation in the electronics attached to the detector. Thus the SVXII circuitry is designed to keep the power dissipation as low as possible.

The SVXII chip is designed for daisy chained operation to reduce the number of control and readout connections in a multichip system. For daisy chained operation with silicon strip detectors, the chips are generally butted together. Thus there is essentially no space for pads on the two sides of the chip adjacent to other readout chips. All of the control and readout pads must be at the back end of the chip. To reduce the number of pads, bidirectional and multifunctional pads are used wherever possible. The 128 inputs from the silicon strip detector to the chip are all located on the side opposite the control and readout.

Simplified Operation

The SVXII is comprised of 128 channels of identical electronics along with some digital circuits which are common to all the channels. Figure 1 shows a simplified diagram of one of the identical channels of electronics and some of the common circuitry. Charge is received from the

silicon strip detector via the input bond wire and integrated on a small feedback capacitor, Cf, which sets the gain of the input amplifier to be 5 mv/fc. In addition to the detector input, a small

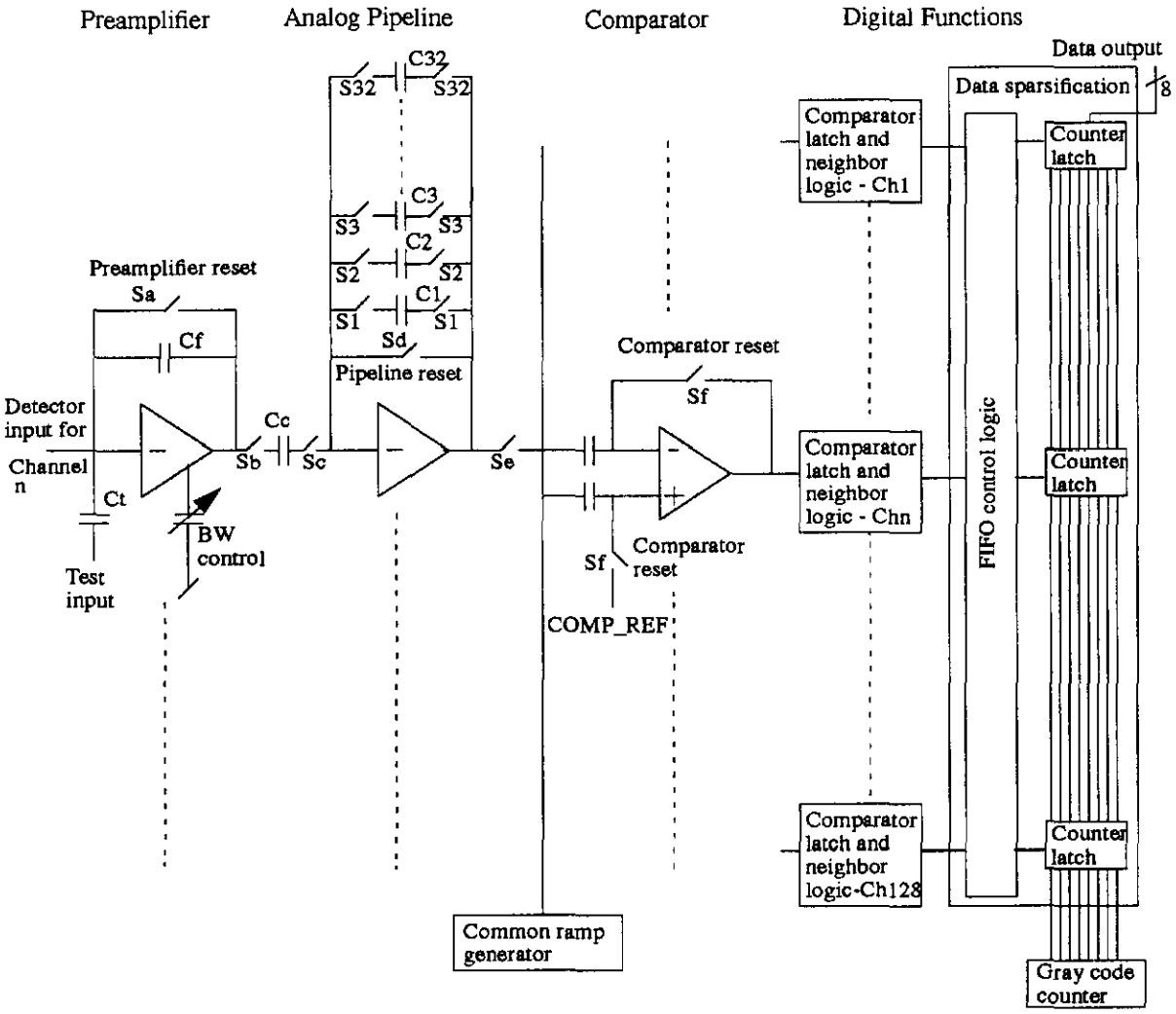


Figure 1 - Simplified Single Channel Block Diagram

separate programmable test input capacitor, Ct, is connected to each integrator. That capacitor allows each channel to be pulsed independently or simultaneously to 1) study channel operation, or 2) provide simulated events through the SVXII to the data acquisition system. Speed of the front end electronics is determined primarily by the integrator response. For different interaction times and input capacitances, the response or bandwidth of the preamplifier is adjusted by means of internal switches and capacitors to provide the optimal preamplifier output risetime and hence minimum noise.

The output of the preamplifier (integrator) feeds the analog pipeline which has a maximum length (32 stages) set by the minimum interaction time and maximum required time delay. The pipeline has a fixed voltage gain of three determined by the ratio of the value of the input coupling capacitor, Cc, and the storage capacitor, Cn. Depth of the pipeline is the same for all channels and can be set via digital control to have any value from 0 to 31 samples. The pipeline

operates by sequentially sampling the output of the preamplifier on one of 32 storage capacitors in the pipeline. After each interaction period, switch Sd in the pipeline resets the next sampling capacitor causing the output of the preamplifier to be stored on the coupling capacitor, Cc, and thus performing a double correlated sample on the preamplifier output. The integrator output is allowed to build until it can be reset by switch Sa at a convenient time as shown in Figure 2.

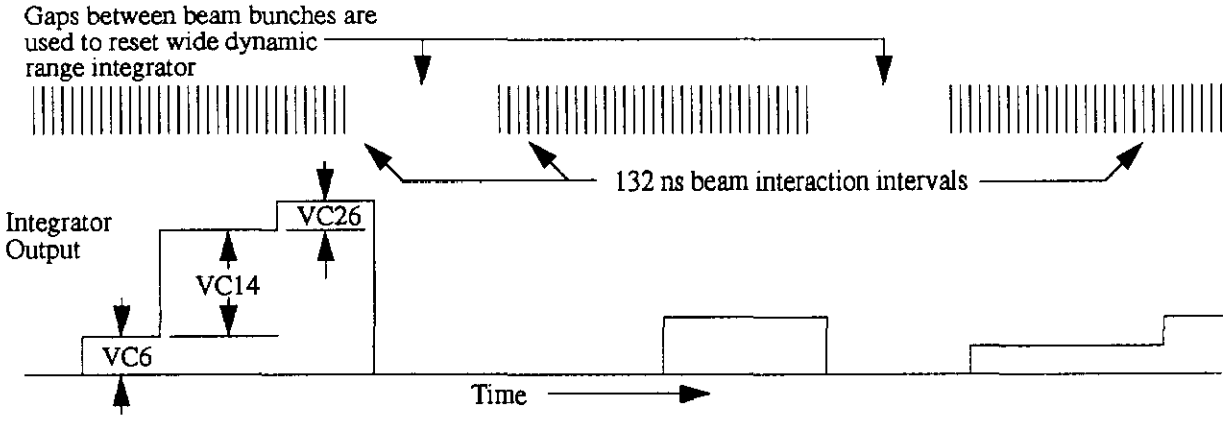


Figure 2 - Resetting Integrator Output During Large Beam Gap

Only the voltage change indicated by VC6, VC14, and VC26 is stored on a sample capacitor for subsequent read out. Charge injection from opening Sd and the sample switches is stored on the sample capacitor along with the desired signal. These charge injection effects are compensated during the pipeline readout. Resetting a storage capacitor can be done relatively quickly. The preamplifier reset however requires a couple hundred nanoseconds and therefore is performed only during the major beam gaps in the main ring beam structure or during a readout. The dynamic range of the preamplifier is 350 fc before saturation begins to occur.

A control signal (derived from the system trigger) to the SVXII indicates when pipeline acquisition should stop and pipeline readout of the appropriate storage capacitor should begin. When the pipeline is read out, a pedestal correction is performed on the stored signal in the pipeline to correct for variations in switch charge injection and other errors.

The output of each pipeline feeds a Wilkenson type 8 bit ADC. The ADC is formed by a separate analog comparator, R-S latch, and counter latch for each channel and a common ramp generator and Gray Code counter which is used for all of the channels. A digital conversion is initiated by starting the ramp generator and then the Gray Code counter. The ramp is applied to the analog comparator along with the input signal to be digitized. When the comparator output changes, the counter latch is set which stores the output of the Gray code counter for that channel. The number stored in the digital latch is a measure of the amount of charge that was integrated by the preamplifier from a given interaction. When the number in the Gray Code counter latch exceeds a programmed threshold setting, that channel is considered to have a hit and it is tagged for readout. Hit channel information is used in two of the three of the readout modes described later in this section.

The SVXII is designed to work with double sided detectors and thus is able to accept both positive and negative current input signals. Several signal inversions take place inside the SVXII chip. The output of the preamplifier is inverted as shown in Figure 1 (e.g. the output signal level is negative going for positive input current and positive going for negative input current). The pipeline inverts the preamplifier signal. The technique used to read out the pipeline causes a third

signal inversion to occur. Thus during pipeline readout which occurs prior to digitization, the signal level to the analog comparator is negative going for positive input current or positive going for negative input current.

For proper operation, externally programmed polarity signals are used to choose either positive or negative input operation for the chip. On the first SVXII (referred to as SVXIIa) three bits (Pipeline Select, Ramp Polarity, Comparator Polarity) are provided for maximum flexibility to set levels inside the chip and establish the proper operation. On later chips these three control bits may be combined.

The three polarity signals perform three different functions inside the SVXII chip. First the Pipeline Select sets the reset point in the pipeline amplifier to one of two different values so that the output range of the pipeline can be maximized for a given polarity. The Ramp Polarity bit controls the direction (positive or negative) of the ramp generator to correspond to the polarity of the input signal. The third polarity bit, Comparator Polarity, is used to either pass or invert the comparator output so that the signal delivered to the following logic has the same meaning for both positive and negative current input signals.

In addition to the three polarity control bits, the SVXIIa has the added ability to set the quiescent operating point in the preamplifier via a separate external control line called PA-REF. The ability to set PA-REF allows maximum dynamic range in the preamplifier for both input signal polarities. Future SVXII designs should generate different quiescent operating points internally which are then chosen by the common external polarity bit.

As shown in Figure 1, the analog comparator feeds a latch and neighbor hit logic. The SVXII data readout can take one of three different forms depending on the status of two control bits called Read Neighbors and Read All in the neighbor hit logic. If both of these bits are low, the channels to be read out are only those channels (i.e. hit channels) whose digitized outputs exceed the threshold level which was digitally downloaded. If the Read Neighbor bit is set high, then hit channels and the channel immediately on each side of the hit channel are also read out. When chips are daisy chained together, neighbor information is passed from one chip to another so that if an end channel is hit, a neighbor channel on the adjacent chip is read out. Readout of neighbor channel amplitudes allows interpolation to obtain higher hit location accuracy. Under some situations such as testing, all channels on a chip can be read out regardless of signal level by setting the Read All bit high. If by accident both Read Neighbors and Read All are set high, all channels are read out.

The hit threshold level for an SVXII chip is set digitally and is the same for all channels on that chip. Normally the threshold is set at some fraction of a MIP which results in a relatively coarse threshold resolution (e.g. 2200 e). To overcome this problem, external control of the A/D ramp start voltage is provided which allows fine tuning of the noise hit rate. Adjusting the ramp start voltage (RAMP-PED) effectively allows the threshold to be adjusted with 400 e resolution.

The output of the neighbor logic circuit from all the channels form an ordered array of the channels to be read out. Before the chip is read out, the address and data for each channel to be read is stacked in a asynchronous FIFO for fast readout. A few hundred nanoseconds are required for the information to be stacked before readout can begin. When readout does begin, channels are read out sequentially beginning with the lowest address channel. Channel 1 is at the top for a chip which has its detector inputs on the left hand side of the chip.

Control of the SVXII and data readout is handled by the digital and bias pads in the I/O section on the right hand side of the chip. There are three pads called MODE0, MODE1, and CHANGE-MODE which are used to select one of the four possible operating modes (Initialize,

Acquire, Digitize, and Readout) for the SVXII. Eight pads, called BUS0-7, are used to output address and data information from the SVXII during the Readout Mode. The same eight pads are used for real time control of internal switches in the other three operating modes. For these three modes, the last information on the pads prior to a mode change is held on internal latches before switching to the next mode. Two other pins, Bottom Neighbor and Top Neighbor, are used to communicate with the control system and adjacent chips. These two pins carry different information for each of the four different operating modes. The last two digital pins in the I/O section are for the differential CMOS clock, which makes a total of 15 digital pads in the I/O section. The remaining 20 pads on the right hand side of the chip carry DC voltages or set bias levels within the chip. In chip versions after the SVXIIa, the number of digital I/O pads should remain the same, while the number of bias and power supply pads should decrease.

Floorplan and Pinout

Figure 3 shows a simplified floorplan of the SVXII chip. On the left hand side are the inputs from 128 silicon strip detectors. The input pads are placed in a double row with an effective pitch of 48 microns. At the extreme top and bottom of the left side there is a detector bias pad which simply provides a direct connection from the detector to two pads on the I/O side of the chip. These two pads allow a detector bias voltage to be applied to the detector through either the top or the bottom of the chip depending on the mounting orientation which is used. The channels of electronics are laid out on a 42 micron pitch to allow space at the top and bottom of the chip for bus routing and common logic. Starting from the left, the preamplifier or integrator section is followed by the analog pipeline section and the A/D section. Following the A/D is the Neighbor and Latch section which feeds the asynchronous FIFO section. Address and data information is passed from the FIFO to the bidirectional I/O pads for readout from the chip. The pads on the I/O side of the chip are in a single row with a 200 micron pitch. On the top and bottom sides of the chip on the I/O side are two additional pads. The PA-VREF and FROUT are test pads, while the BN (bottom neighbor) and TN (top neighbor) pads are used to communicate between adjacent chips or the control system.

The following is a list of the pads and their function on the I/O side of the SVXII chip starting in the lower right hand corner and moving counterclockwise. The pads with multiple functions are described in more detail in the next section. (In the following list B=bottom side, R=right side, T=top side, L=left side of the chip. Detector connections are made on the left side of the chip.)

Pin #	Name	Function
B1	BN	Multifunctional pad: serial data in during initialize, bottom neighbor pad during digitize, and priority out during readout.
B2	PA-REF	Preamplifier reference used to monitor preamplifier bias point.
R1	DET-B1	Bias connection to detector along the bottom side of chip.
R2	SET	Sets pipeline bias current via an external 25K resistor to GND.
R3	VI1	Sets preamp bias current via an external 18K resistor to AVDD.
R4	COMP-B	Sets A/D comp bias current via an external 350K resistor to GND.
R5	RAMP-B	Sets ramp op-amp bias current via an external 1K resistor to GND.
R6	RAMP-RA	Sets current which fixes A/D ramp rate via a 70K resistor to GND.

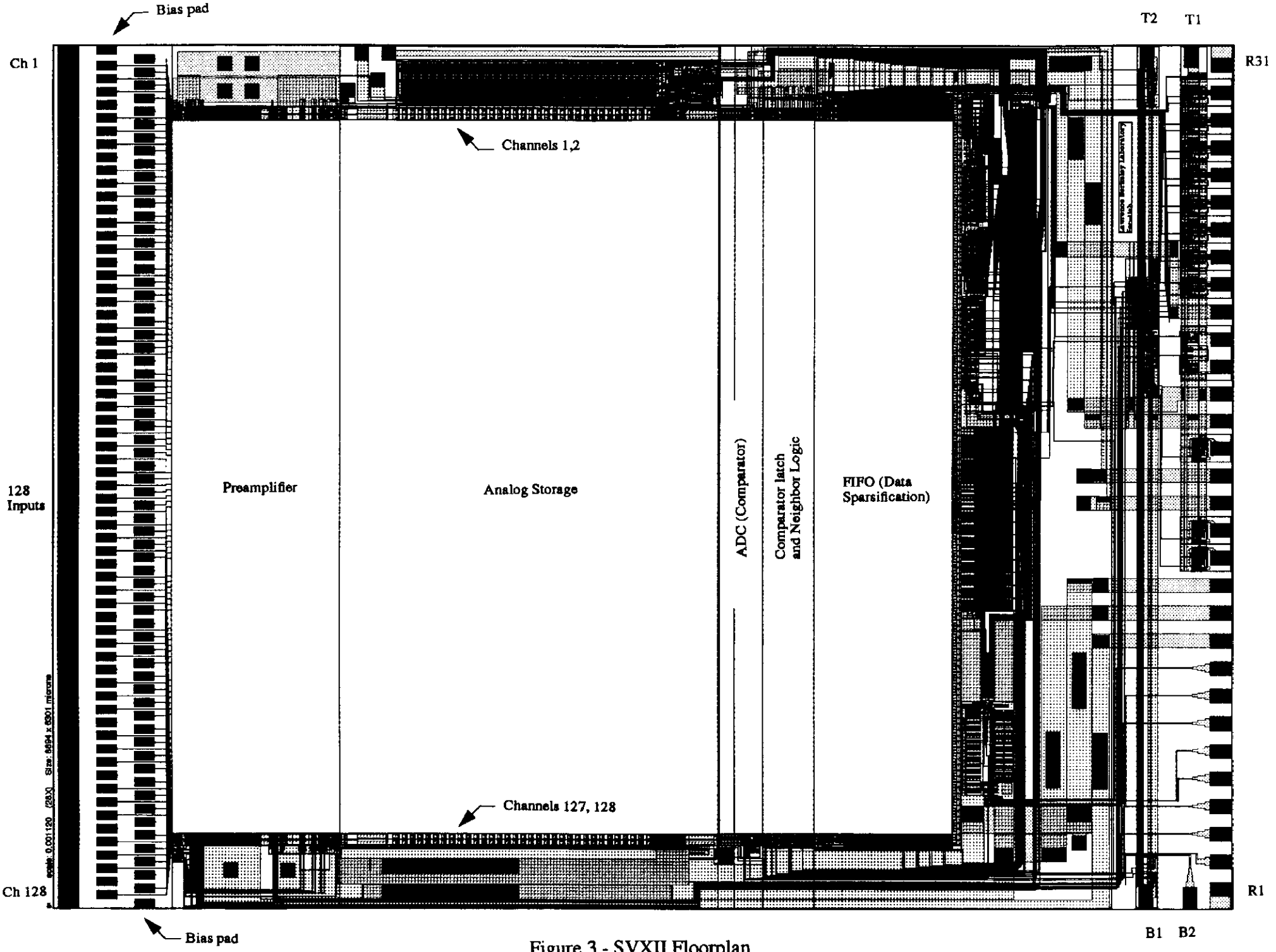


Figure 3 - SVXII Floorplan

R7	RAMP-PD	External voltage which sets an offset pedestal for the comparator.
R8	RAMP-RF	External voltage which sets the ramp start reference point and the comparator reset point.
R9	CAL	External voltage that sets the amplitude of the test pulse.
R10	AVDD2	Analog power source for amplifier input transistor (+2 to 5 V nominal).
R11	AGND	Analog Ground
R12	AVDD	Amplifier and pipeline analog power source (+5 V nominal).
R13	MODE0	One of two mode control bits.
R14	MODE1	One of two mode control bits.
R15	QVDD	Quiet digital power supply for pipeline sample switches (+5 V nominal).
R16	QGND	Quiet digital ground associated with QVDD.
R17	CHNG-MD	Change mode bit is used as a strobe for the 2 mode control bits.
R18	DVDD	Noisy digital power supply. (+5 V nominal)
R19	DGND	Noisy digital ground.
R20	CLK	Differential clock input.
R21	CLKB	Differential clock input.
R22	SUB	Substrate contact for the digital section of chip. (connect to ground in SVXIIa).
R23	BUS0	Bit 0 of the multifunction I/O bus.
R24	BUS1	Bit 1 of the multifunction I/O bus
R25	BUS2	Bit 2 of the multifunction I/O bus
R26	BUS3	Bit 3 of the multifunction I/O bus
R27	BUS4	Bit 4 of the multifunction I/O bus
R28	BUS5	Bit 5 of the multifunction I/O bus
R29	BUS6	Bit 6 of the multifunction I/O bus
R30	BUS7	Bit 7 of the multifunction I/O bus
R31	DET-B2	Bias connection to detector along the top side of chip.
T1	FROUT	Test point to look at the hand shake signal from the FIFO which indicates data remaining in the FIFO.
T2	TN	Multifunctional pad: serial data out during initialize, top neighbor pad during digitize, and priority in during readout.

Operation of the SVXII is controlled through the above list of pads and from a series of bits which are serially downloaded through BN to control parameters within the chip. These parameters which include such things as test inputs and analog pipeline length are described later in more detail in the section on downloading chip parameters.

The SVXII chip, as shown in Figure 3, measures 6.3 x 8.7 mm. This is more than twice the size of the SVXI radiation hard device. There are approximately 85,000 transistors on the SVXIIa.

Modes of Operation

The SVXII operates in four distinct modes: Initialize, Acquire, Digitize, and Readout. The Initialize mode is used at power up to serially load internal control registers and download a

hit test pattern for diagnostic purposes. In the Acquire mode, two separate operations take place. First, the preamplifier integrates charge from the detector, and the pipeline samples and stores the integrator output at the predetermined interaction rate (e.g. 132 nsec). Then sampling of the input signals stops and the sample with the proper delay is selected and presented at the pipeline output. In the Digitize mode, the analog information for all 128 channels is simultaneously digitized to 6, 7, or 8 bits of resolution and then sparsified. In the Readout mode, the digitized data is read out on an eight bit parallel bus. The information that is on the bus changes with each half cycle of the clock. When readout of a chip begins, the chip ID number appears first on the high part of the clock cycle and then an 8 bit status word (currently not used) appears on the following low half of the clock cycle. After the first complete clock cycle, data and address appear on alternate halves of the clock cycle until the chip is completely read out. The actual data that is read out is selected by the Read Neighbor and Read All bits which were downloaded during the initialize mode. The primary reason for changing modes is to change the function of some or all of the multifunctional pads. A typical operating sequence of modes for an SVXII chip is as follows:

Initialize>>Acquire>>Digitize>>Readout>>Acquire>>Digitize>>Readout>> Acquire>>etc.

Operation in one of the modes is set by the two mode control pads, MODE0 and MODE1, in the following way:

MODE1	MODE0	FUNCTION
0	0	Initialize
0	1	Acquire
1	1	Digitize
1	0	Readout

Table 1 - SVXII modes of operation

The CHANGE MODE pad is used as a strobe along with the mode pads to actually change modes. To change modes, the CHANGE MODE pad is raised high which temporarily latches the data on the write through register. The two mode bits are then changed and the CHANGE MODE pad signal lowered to complete the transition to the new mode of operation. Figure 4 shows the

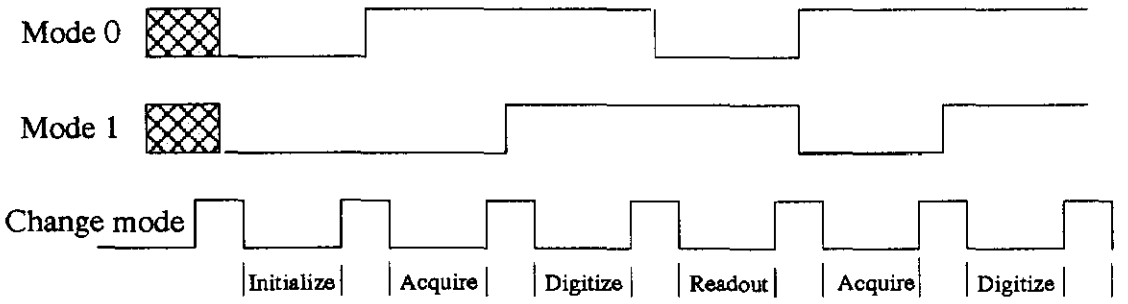


Figure 4 - Change mode signals

sequence for changing between several different modes.

The SVXII has 10 pads which can change function when modes are changed. Eight of the

pads, called BUS0-7, are used for parallel data readout and for independent real time control of internal switches. The other two pads, called TN (top neighbor) and BN (bottom neighbor) are used for communicating between adjacent chips or the control system and provide three very different functions as described below. Table 2 summarizes the signals on the multifunctional and clock pads in the different operating modes.

Pad	Name	Initialize	Acquire	Digitize	Readout
B1	BN	Serial data in	(no connection)	/BOTTOM HIT	/PRIORITY OUT
R20	CLK	SERIAL-CK	PIPE-CK	COUNTER-CK	FIFO-CK
R21	CLKB	SERIAL-CKB	PIPE-CKB	COUNTER-CKB	(no connection)
R23	BUS0	PA-RST	PA-RST	PA-RST	DOUT0
R24	BUS1	(no connection)	CAL-INJECT	RREF-SEL	DOUT1
R25	BUS2	ACQ	ACQ	ACQ	DOUT2
R26	BUS3	PIPE-SREF	PIPE-SREF	PIPE-SREF	DOUT3
R27	BUS4	CNTR-RST	CNTR-RST	CNTR-RST	DOUT4
R28	BUS5	RAMP-RST	RAMP-RST	RAMP-RST	DOUT5
R29	BUS6	COMP-RST	COMP-RST	COMP-RST	DOUT6
R30	BUS7	SR-LOAD	(no connection)	FIFO-RST	DOUT7
T2	TN	Serial data out	(no connection)	/TOP HIT	/PRIORITY IN

Table 2 - SVXII pad functions versus mode

The TN (top neighbor) and BN (bottom neighbor) pads have similar functions. During the Initialize mode, the BN acts as an input for serial data (parameters) to be loaded into the SVXII. TN acts as an output for serial data passing through the chip to the next adjacent chip or acts as a monitor for checking data which was previously loaded into the chip(s). The TN and BN pads have no function during the acquire mode. During the Digitize mode, the BN pad passes neighbor hit information back and forth between the bottom neighbor chip and the TN pad performs the same function with the top neighbor chip. In the Readout mode, several chips share the same data bus and a priority bit is passed between chips to acknowledge which chip has access to the bus. In the Readout mode, the TN pad acts as a priority input pad from a previous chip or the control system and BN acts as a priority out signal to feed an adjacent chip.

The signal names shown in Table 2 for the tri-state write through bus during the Initialize, Acquire, and Digitize mode refer to those signal functions inside the SVXII which require real time control. Most of the internal signal functions do not change for these three modes. Table 3 explains the signal functions on the five write through bus lines that do not change function during the and Initialize (I), Acquire (A), and Digitize (D) modes.

For simplicity, it would have been nice if all write through bus lines could have had the same function for the Initialize, Acquire, and Digitize modes. However, since 10 real time control functions were required, the signals on BUS1 and BUS7 have more than one function. In future SVX2 versions, some write through register signals may be derived internally and then all the write through register lines would have only one function in addition to data readout. Table 4 explains the signals on BUS1 and BUS7.

When a mode change takes place as shown in Figure 4, the last state of the input data to the chip on the write though register is latched and held for the internal signals used in the previ-

ous mode. This is particularly important when changing from the Digitize to Readout mode where the bus lines change from inputs to outputs. Thus control of the internal control signals is transferred between the write through bus and the internal latches as mode changes take place.

Pad name	Signal name	Mode	Signal function
BUS0	PA-RESET	I,A,D	Preamplifier (integrator) reset (1 = reset)
BUS2	ACQ	I,A,D	Acquire line (1 = normal acquisition, 0 = stop acquisition and begin pipeline capacitor readout).
BUS3	PIPE-SREF	I,A,D	Pipeline reference capacitor sample switch. Used to read out pipeline after acquisition is stopped. (1 = switch closed)
BUS4	CNTR-RST	I,A,D	A/D Gray code counter reset (1 = reset)
BUS5	RAMP-RST	I,A,D	A/D ramp reset (1 = reset)
BUS6	COMP-RST	I,A,D	A/D analog comparator reset (1 = reset)

Table 3 - Write through bus lines that do not change function during Acquire, Digitize, and Initialize modes.

Pad name	Signal name	Mode	Signal function
BUS1	(none)	I	(none)
	CAL-INJECT	A	Provides timing pulse to inject calibration pulse into preamp. The magnitude of the pulse is set by CAL pad.
	RREF-SEL	D	Switches the ramp amplifier input from RAMP_REF to RAMP_PED. (1=RAMP-REF, 0=RAMP-PED)
BUS7	SR-LOAD	I	Loads serial register parameters into chip. Also initializes the pipeline shift register pointers in the analog storage section. (1 to 0 transition = load and initialize)
	(none)	A	(none)
	FIFO-RST	D	Controls data in the sparsification FIFO (1=hold hit channel data in the FIFO, 0=collapse hit channels before readout)

Table 4 - Write through bus lines that change function during Acquire, Digitize, and Initialize modes.

It is important to note that the signals on the differential clock pads are different for the four modes. Thus, an intelligent clock (one that changes frequency and duty cycle) is required to control the SVXII. The differential input clock uses PECL logic levels (1=+3.0V, 0=+2.2V). In the Initialize mode, the input clock runs with a 50% duty cycle and is used to clock chip parameters and test hit patterns into the SVXII serial shift register. During the Acquire mode, the input clock signals, CLK and CLKB, are directed internally to the analog pipeline. The CLK and CLKB lines are the only digital lines which are changing while data is being acquired and must have an accurately controlled non-50% duty cycle. In the Digitize mode, the clock lines are run with a 50% duty cycle and are used to increment the Gray Code counter in the A/D converter. In the Readout mode, the input clock is also run at a 50% duty cycle and used to read data out from the SVXII chip onto the data bus. In principle, the input clock could be run at the same frequency

for all the operating modes. However, for optimal performance, the user will probably choose to change the clock frequency when changing modes.

Downloading of Chip Parameters

The SVXII has two programmable features not found on the original SVX: 1) the ability to download many parameters that set up and control the chip, and 2) the ability to program the test inputs for each channel. Both of these features are implemented via a serial shift register input. The parameters are loaded through the BN pad during the Initialize mode.

In the Initialize mode the differential input clock is used to clock 182 bits into each chip. The first 128 bits are used to set a test input mask. The remaining 54 bits are used for internal control and spare bits. Extra control bits were added for flexibility on the SVXIIa. Some bits may be removed on future versions. Table 5 provides an ordered list of the serial link data and the function of each of the data bits.

Bit(s)	Function
1-128	Test input mask for 128 channels, bit 1 controls test input for channel 1 at top of chip, (1 = test, 0 = no test input when CAL-INJECT line is pulsed during Acquire mode)
129	Select the polarity of the input test pulse. (1 selects a positive input charge equal to (AVDD - CAL)*Ct, 0 selects a negative input charge equal to (CAL - AGND)*Ct where Ct is the test input capacitor).
130	Pipeline-Select adds an offset voltage to the pipeline amplifier reset point for maximum dynamic range with bidirectional inputs. (1 = negative detector input current, 0 = positive detector input current)
131-136	Adjusts preamp bandwidth for different detector capacitances and interaction time. Bits add binary weighted capacitors to the preamp. (bit 131 = 1 adds smallest cap)
137-143	Binary coded chip ID number. (bit 137 = MSB, bit 143 = LSB)
144-149	Six spare shift register cells.
150	Read Neighbor bit (1 = Read nearest neighbors)
151	Read All Channels bit (1 = Read all channels)
152	Ramp Polarity bit selects polarity of A/D ramp (1 = ramp up, 0 = ramp down)
153	Comparator polarity bit (use "1" for ramp up, use "0" for ramp down)
154-158	Binary Pipeline Depth number to set analog storage delay from 0 to 31 samples (bit 154 = MSB, bit 158 = LSB)
159-166	Threshold set in digital comparator (bit 159 = MSB, bit 166 = LSB)
167-174	Counter Modulo sets the stop value for the A/D Gray Code counter. (bit 167 = MSB, bit 174 = LSB)
175-182	Ramp Trim adjusts the ramp capacitor value over a 20% range by adding binary weighted capacitors (bit 175 = largest capacitor, bit 182 = smallest capacitor)

Table 5 - Serial Link Data Bits

Table 5 shows that there are four bits which control internal polarity switches in the SVXII. The normal settings for these switches are shown in Table 6 for both positive and nega-

tive input signals.

Bit	129	130	152	153
Bit Name	Test pulse	Pipeline select	Ramp Pol.	Comp Pol.
	----------Bit signal level----------			
Pos input charge	1	0	0	0
Neg input charge	0	1	1	1

Table 6 - Polarity bit settings

To change any bit in the shift register all bits must be clocked into the chip. After the shift register is loaded, SR-LOAD in the write through register is toggled to transfer all the parameters into a shadow register. The test input mask (bits 1-128) does not have a shadow register.

Daisy Chain Operation

The SVXII is designed for daisy chained operation to minimize the number of bus and control lines required to operate the device. (Fewer control lines means less space on the high density interconnect and less mass in the system.) A group of daisy chained chips is shown in

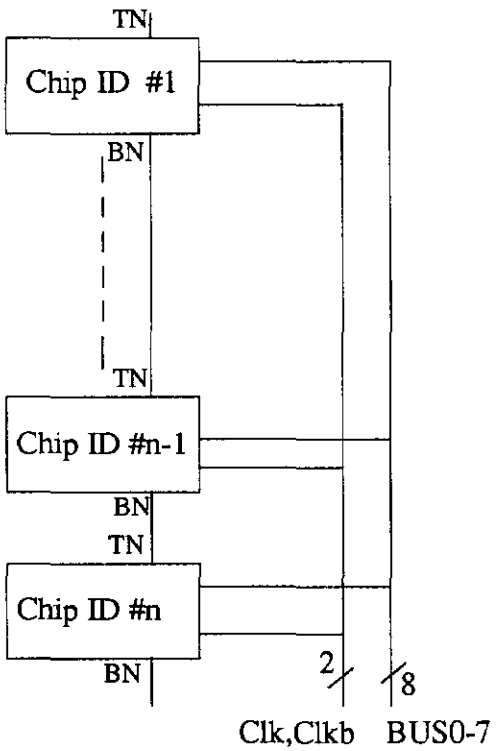


Figure 5 - Daisy chained readout chips

Figure 5. All of the chips share a common communication bus (BUS0-7) and a common differential clock (CLK, CLKB). In addition, each chip has two pins called TN and BN which are used for communication between adjoining chips

After power up of the SVXII's, the chip parameters listed in Table 5 must be downloaded

before useful operation of the readout chips can begin. For each SVXII chip, 182 bits must be downloaded into internal registers. In the Initialize Mode, the TN and BN pads are used as a serial data link to form a very long shift register for downloading parameters to the string of daisy chained SVXII's. Parameters for each of the chips are loaded in sequential order with data for chip #1 loaded first via the BN pad on the last chip in the daisy chain. Data is clocked between cells in the shift register using the common differential clock pads. If there were 10 chips in the chain, exactly1820 bits would have to be downloaded in the Initialize Mode. Downloaded parameters may be checked by shifting the bits out through TN of the first chip while reloading the chips with the same data. To identify each chip in the daisy chain, a separate chip ID number (bits 137-143) is downloaded into each chip during the Initialize Mode. The seven bit chip ID number allows chips to be tagged with numbers from 0 to 127.

In the Acquire Mode, the BUS0-7 and clock pads provide simultaneous real time control of all of the chips in the daisy chain. These pads perform critical timing functions within the chip. The TN and BN pads have no function in the Acquire Mode.

In the Digitize Mode, the BUS0-7 and differential clock pads provide simultaneous real time control of all the chips in the daisy chain. Again, these pads perform critical timing functions within the chip. The TN and BN pads are used to pass neighbor information between adjacent chips for neighbor readout in the Digitize Mode.

In the Readout Mode, the BUS0-7 lines are changed from input lines to output lines. During readout, data from each SVXII chip is placed on the common bus beginning with the top chip in the daisy chain and proceeding sequentially through the remaining chips. Information is placed on the bus in 8 bit bytes. First the chip ID and status of the first chip is read out. Then address and data information for that chip is read out beginning with the channel nearest the top of the chip, channel 1, and proceeding downward. Priority for the output bus is passed from pad BN of the first chip to pad TN of the next chip after the first chip has been completely readout. (The top chip in the daisy chain will have a priority first since the TN pad is internally pulled weakly low to initiate readout). Information is read out using both the high and low transitions of the differential clock. Thus, the channel readout rate is approximately equal to the clock frequency.

OPERATION AND TIMING DIAGRAMS

Chip Initialization

The start up procedure for the SVXII is shown in Figure 7 where the I/O control pads for the SVXII are shown on the far left side. Internal signal names associated with the I/O pads in the Initialization Mode are shown adjacent to the pad names. (Some pads are multiplexed to serve several functions, depending on the mode. Signal names shown in parentheses are not used in this mode.)

To avoid latchup, the power supplies should be turned on in the following sequence: DVDD, QVDD, AVDD, and AVDD2 (AVDD2 must be applied last). The chip is placed in the Initialization Mode by raising the Change Mode line and setting Mode 0 and Mode1 low. The BUS0-7 inputs on the write through bus are set to keep the chip in a 'safe' mode during initialization. When the Change Mode signal falls, the chip is latched in the initialize mode and the internal signals shown become active (connected to the pads wherever appropriate). Chip parameter information is then placed on BN to be shifted into the 182 bit serial shift register. At the same time, the clock signals to the chip are started and become the serial shift register clock, Serial-ck and Serial-ckb. Data may be downloaded with a 50% duty cycle clock at speeds up to 53 MHz.

All 182 bits must be loaded to make the chip functional. The waveform for BN shows four of the bits. Bits 1-3 show the first three bits of the test mask for a test pulse on channels 1 and 3. Bit 182 is shown set high to insert the smallest capacitor in the ramp trim section. When the clock for bit 182 goes low, bit 1 that was loaded into the shift register appears on TN and is available for BN of an adjacent chip to load parameters into that chip. Of course, 182 more bits need to be downloaded if a second chip is to be initialized. When all of the bits have been loaded into the shift register, SR-LOAD is raised to load some of the shift register bits into a shadow register as shown in Figure 6. The 128 bits for the test mask do not have a shadow register. When SR-

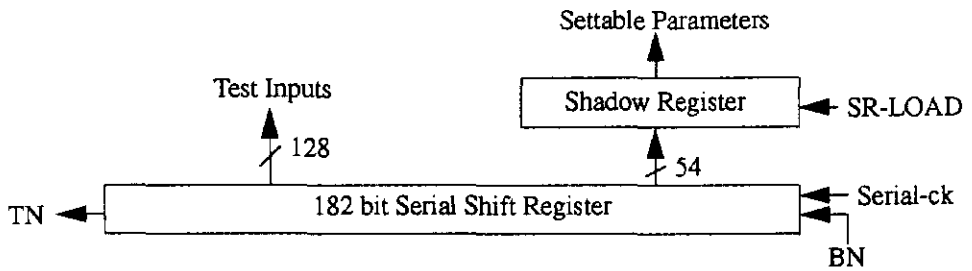


Figure 6 - Serial Shift Register for Downloading Chip Parameters

LOAD is lowered, the initialization parameters are latched in the shadow register. Lowering SR-LOAD also initializes the pointers in the pipeline shift registers. Initialization of the chip is complete and operation can be transferred to the next mode.

It should be noted that the internal register latches which provide the CAL-INJECT, RREF-SEL, and FIFO-RST signals have not been cleared or reset during initialization. These three internal signals will have known internal levels after the Acquire and Digitize Modes have been exercised for the first time.

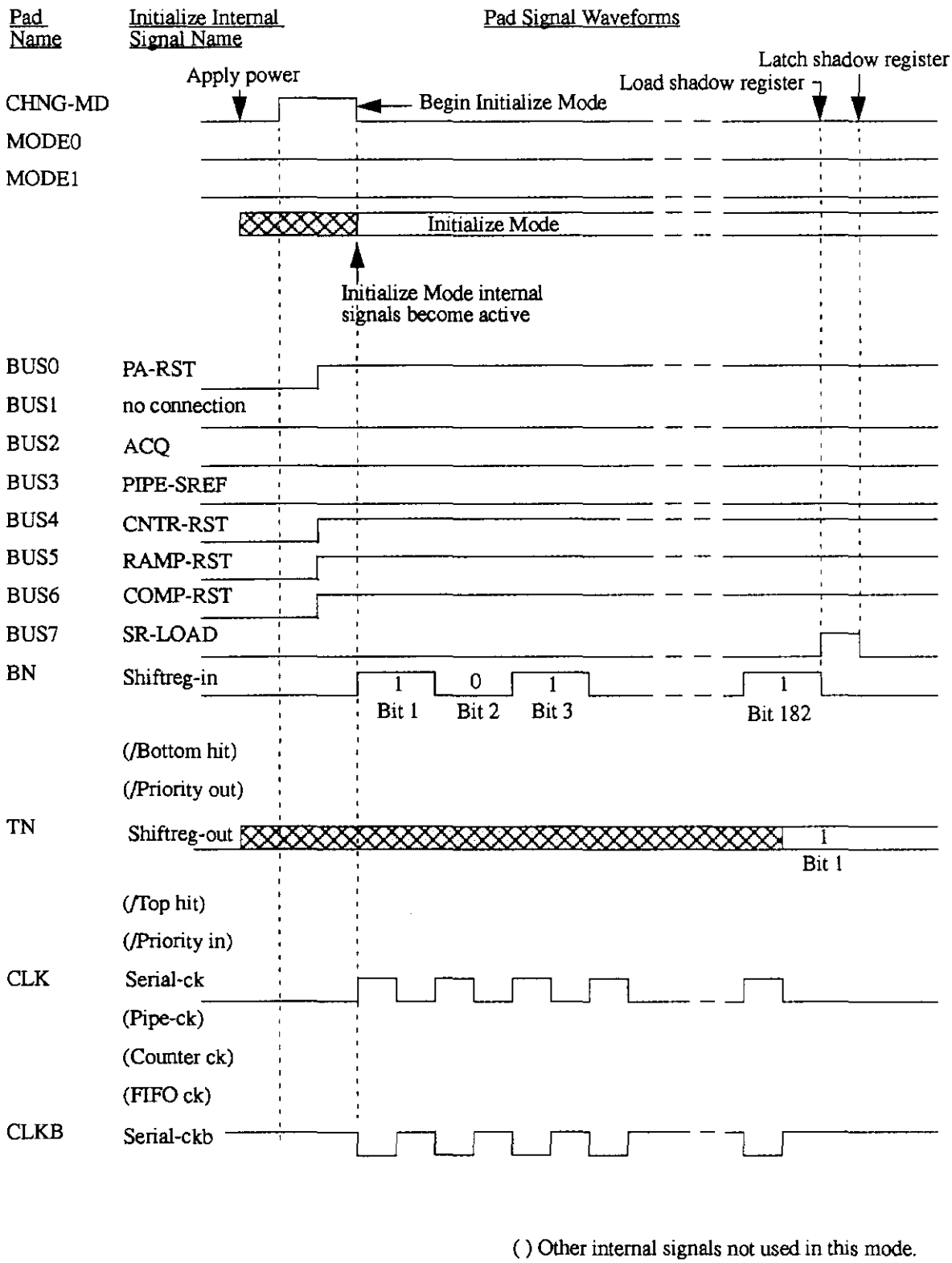


Figure 7 - Initialization Timing Diagram

Data Acquisition and Pipeline Readout

The preamplifier (integrator) and pipeline sections of the SVXII shown in Figure 8 are active in the Data Acquisition mode. There are numerous switches which need to be opened and closed in the proper sequence. Many of the switches and critical timing issues are controlled internally. Critical external timing issues for data acquisition are addressed in this section.

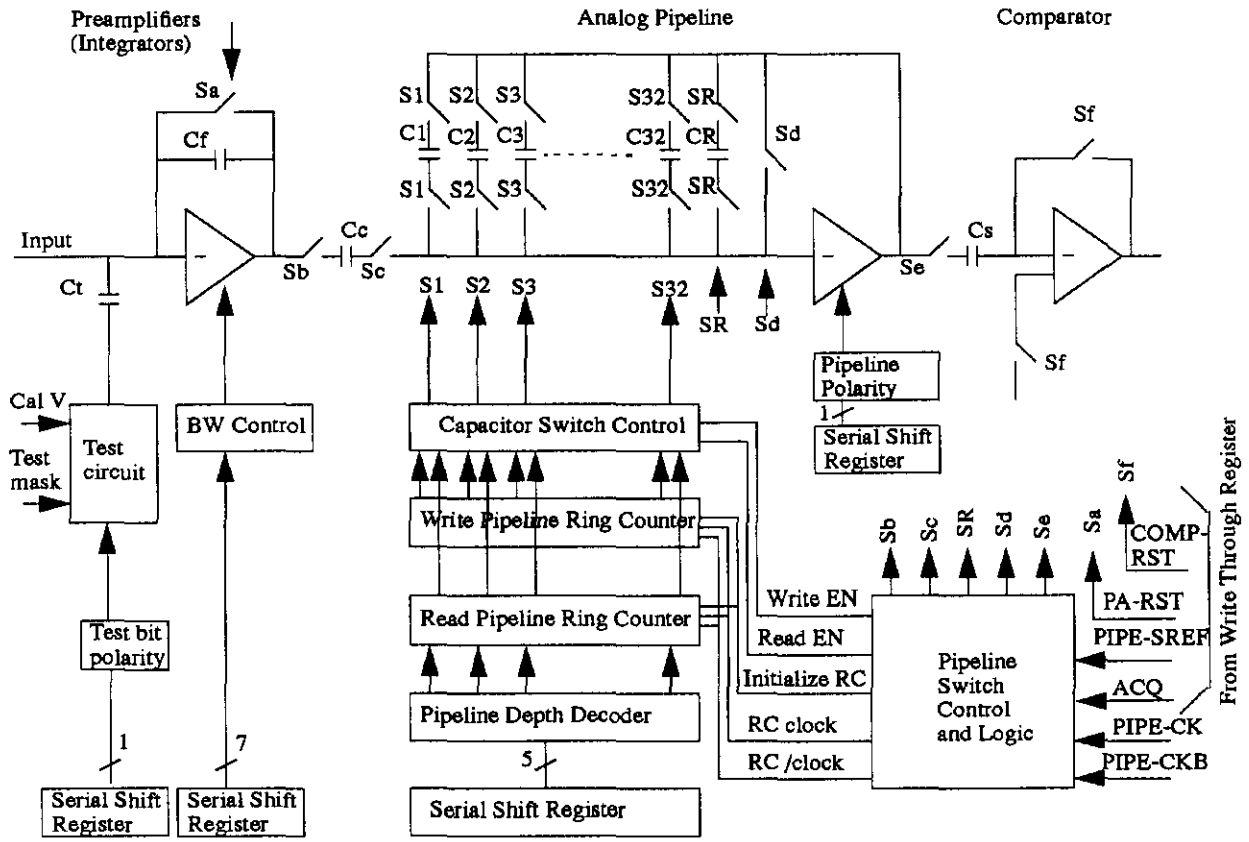


Figure 8 - Preamplifier and Pipeline Control

Before operating in the Data Acquisition mode, the proper parameters for the preamplifier and pipeline must have been downloaded into the serial shift register during initialization. The bandwidth setting of the preamplifier is determined by the interaction time interval. The serial shift register allows preamplifier bandwidth changes to be made by adding binary weighted capacitors to the dominant node of the preamplifier. Since the actual preamplifier response is also determined by the detector capacitance and chip processing, the appropriate shift register bits will be determined by the designers after preliminary tests have been completed. The proper bandwidth is chosen by setting the risetime at the output of the integrator to reach 99% of its final value in approximately100 nsecs (for 132 nsec interval operation). If the risetime is greater, some portion of a given signal is present in the subsequent 132 nsec time interval. If the risetime is less, the signal is noisier than necessary. Fine control of the risetime is necessary to provide optimal chip performance.

The electrical depth of the pipeline is programmable from 0 to 31 samples by a 5 bit

binary number loaded into the serial shift register. The number loaded into the parameter shift register sets an offset between the write and read shift register pointers which address the pipeline cells. Setting a zero into the pipeline depth means that if acquisition is stopped and a pipeline readout is initiated, then the sample which is read out is the last one which was taken. If the pipeline depth is set to 31 and a sample is taken, then 31 additional samples must be taken before that first sample can be read out for digitization.

The proper settings for the pipeline polarity bit, test input polarity bit and 128 bit test mask must also have been loaded into the serial shift register. Operation of the test input using the input test mask and test polarity bit is discussed at the end of this section.

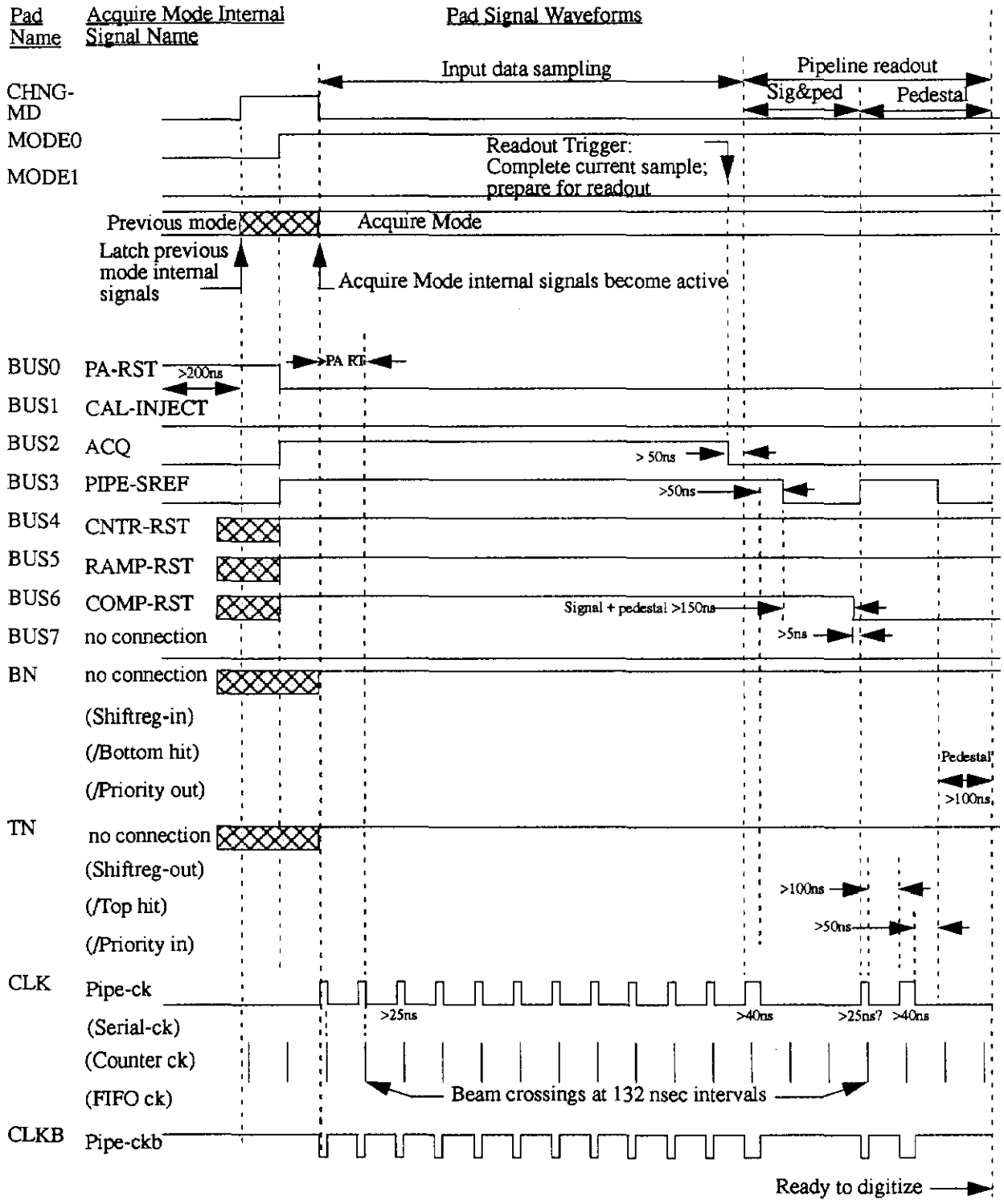
The serial shift register sections shown in Figure 8 for the preamplifier and pipeline are connected in series in the order given in the section on downloading parameters.

The Acquire mode is entered by controlling the Change Mode, Mode0 and Mode1 lines as shown in the timing diagram of Figure 9. When the Change Mode line is raised, the signal levels on the write through bus that were used in the previous mode are latched at their final value. While Change Mode is high, Mode0 is set to 1 and Mode 0 set to 0. The BUS0-7 pads are not connected to any internal signals while Change Mode is high. During this time, signals on the BUS0-7 pads are set up to prepare for the Acquire Mode. BUS2 is set high (to set the chip in a data acquiring condition) and BUS3 is set high (to insert the capacitor CR into the pipeline amplifier feedback loop, which is necessary during acquisition). When the Change Mode line is lowered, the BUS0-7 pads are connected to the Acquire Mode internal signal lines (i.e. signals which are on the BUS0-7 pads when Change Mode goes low appear on the Acquire Mode internal signal lines.) The BUS0-7 pads are then in control of the Acquire Mode internal signal lines.

Prior to raising the Change Mode line, the preamplifier reset switch Sa controlled by PA-RST on BUS0 must have been closed for more than 200 nsec to insure adequate reset of the preamplifier. This is accomplished by having PA-RST set to a high condition at the end of a previous mode (Initialize or Digitize). After the reset switch is opened (when Change Mode goes low), the preamplifier must absorb the charge injection from Sa. Data acquisition should not begin until the preamplifier response stabilizes which takes a time at least equal to the 0-99% rise-time programmed into the preamplifier. If data sampling begins immediately after Change Mode goes low as shown in Figure 9, the first data sample after Change Mode goes low will have a large signal due to charge injection from opening the preamplifier reset switch.

For discussion purposes, operation in the Acquire Mode is divided into two parts: 1) input data sampling, followed by 2) pipeline readout. The only external signal to the chip which is changing during the sampling mode is the differential input clock. This minimizes noise coupling to the sensitive analog inputs. The rising edge of Pipe-ck is used to advance the write and read pointers in the pipeline and initiates reset of the next capacitor in the pipeline. While the clock is high, the pipeline reset switch Sd is closed. The clock should be phased so that the clock goes low (and the reset switch opens) at the instant a beam crossing takes place. To insure a complete reset, the clock should be high for at least 25 nsec. When operating with 132 nsec interaction times, the reset should not exceed 30 nsec in order to allow for maximum integration time and minimum noise. The chip normally remains in the data sampling mode storing voltages on the pipeline capacitors until a readout trigger arrives. A pipeline readout is initiated by lowering the ACQ signal before the next high clock transistion.

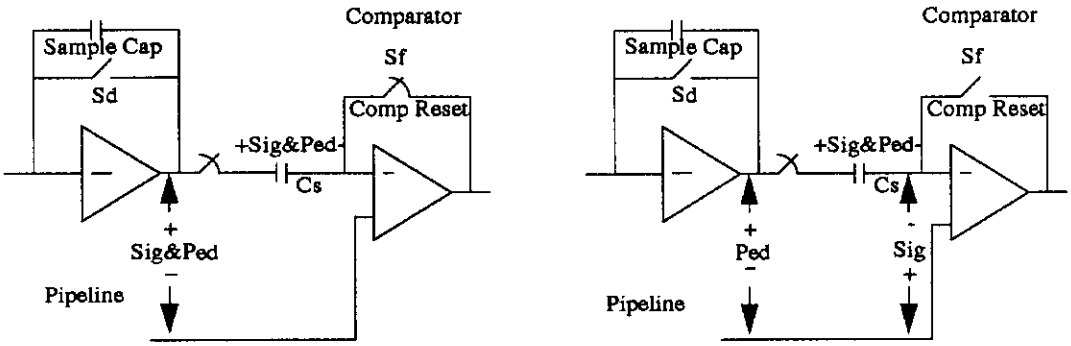
Signals along with pedestals have been stored on the pipeline capacitors during the data sampling period. Data from a cell to be read needs to be processed before digitization to compensate for the pedestals which vary from sample to sample and channel to channel. This correction



( ) Other internal signals not used in this mode.

Figure 9 - Data Sampling and Pipeline Read Timing Diagram

takes place during the pipeline readout section shown in Figure 9. In the first part of the pipeline readout, the desired signal & pedestal stored on one of the sampling capacitors is selected and output from the pipeline. That signal appears across Cs as shown in Figure 10a (Positive signal and pedestal polarities are chosen for illustration purposes.) When switch Sf opens, the signal & pedestal is stored on Cs with the polarity shown. In the second part of the pipeline readout cycle,



a) Place Signal&Pedestal on Cs

b) Output Pedestal from Pipeline

Figure 10 - Pipeline Pedestal Subtraction

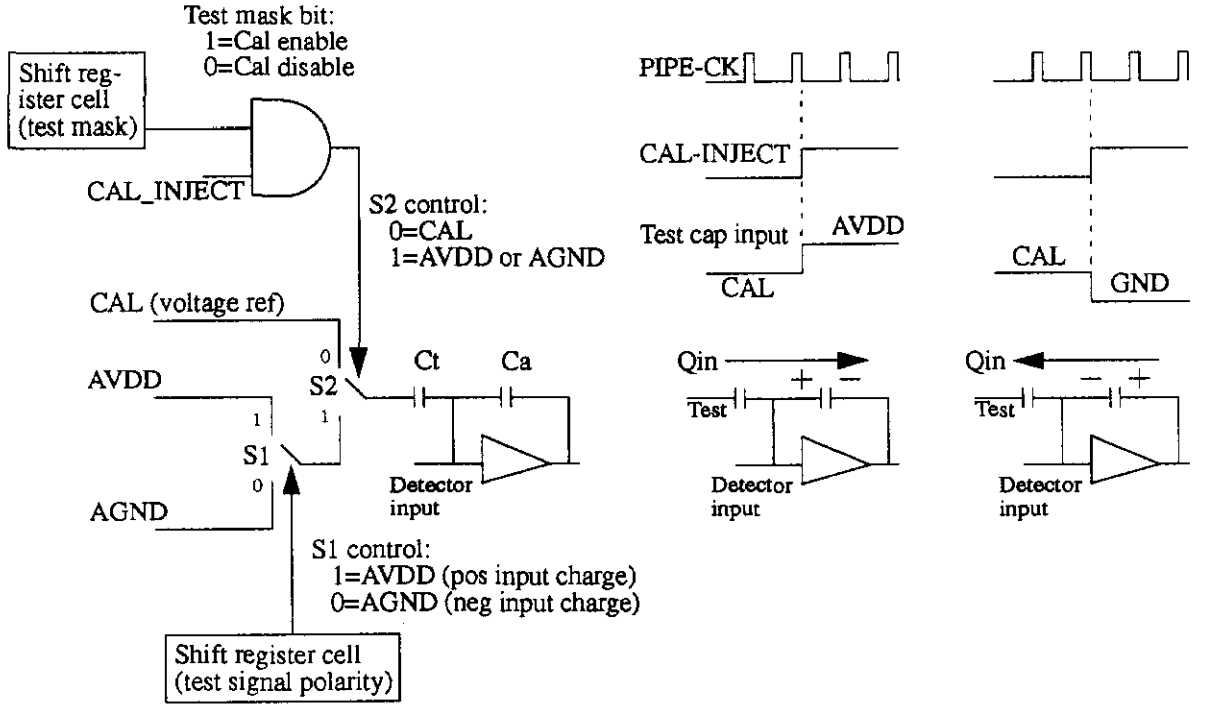
the pedestal voltage is reconstructed using the same capacitor and switches that were used during data sampling, and that voltage is placed at the pipeline amplifier output as shown in Figure 10b. The voltage stored on the coupling capacitor Cs subtracts from the pipeline output voltage to develop a voltage equal to the negative of the stored signal at the input to the analog comparator. Thus the charge injection compensation scheme used during the pipeline readout causes the signal to be inverted between the pipeline and comparator. The critical timing conditions for the pipeline readout section are shown in Figure 9. Note that after the trigger signal arrives, the pipeline requires at least 560 nsec to read out the desired signal before digitization can begin.

The integrator needs to be regularly reset to prevent it from saturating. The best time to reset the integrator is during a major beam gap. During a beam gap, the pipeline clock (Pipe-ck) must keep running to permit possible data readout from earlier interactions. To reset the preamplifier completely, PA-RST must be raised for at least 200 nsec. When PA-RST is lowered, charge is injected into the integrator. The integrator should be allowed to settle for a time greater than the 0-99% risetime of the preamplifier before valid data is taken. (Note, if a readout trigger occurs during the preamplifier reset, then PA-RST must immediately go low along with ACQ in order to read out the pipeline. The preamplifier reset should then be completed during data readout.)

Each channel of the SVXII has a test charge circuit which is programmed by two of the bits in the serial shift register. The test charge can be activated during the data sampling period and read out after the delay set by the downloaded pipeline depth. Test input charges are generated by switching a voltage through a small capacitor into the integrator input as shown in Figure 11a. Polarity of the charge input is controlled by the test polarity bit in the serial shift register which controls S1. The test pulse is generated by switching the test input voltage from CAL to AVDD for positive charge input or switching from CAL to AGND for negative charge input. (Refer to Figures 11b and c.) The magnitude of the input charge pulse is set by the voltage difference between CAL and the final switched voltage level, and the size of capacitor Ct. With Ct=50

fF, a voltage step (CAL to AVDD, or CAL to AGND) of 80 mv gives an input charge of 4 fC or 1 MIP.

A test pulse is initiated with S2 by raising CAL-INJECT in the presence of a test mask bit set equal to 1. For proper operation, the rising edge of the CAL-INJECT should coincide with the



a) Single Channel Test Circuit Block Diagram b) Positive Test Input c) Negative Test Input

Figure 11 - SVXII Test Circuit Operation

falling edge of the clock (opening the pipeline reset switch). CAL-INJECT should stay high for at least one interaction interval.

Digitization and Data Sparsification

Proper operation in the Digitization Mode is dependent on proper downloading of information during the Initialization Mode. The Read Neighbor Bit (bit 150), Read All Channel Bit (bit 151), Ramp Polarity Bit (bit 152), and the Comparator Polarity Bit (bit 153) must be set properly as described in the section on downloading of chip parameters. The maximum count number that the A/D converter can reach during digitization is set by a Gray code number using bits 167-174. To achieve the largest count (256) on the SVXII, the downloaded number is 10000000. For a count of 128, the downloaded number is 01000000; for 64 counts the number is 00100000, etc. The threshold level for a hit channel is set digitally by a Gray Code number using bits 159-166. Normally the threshold level is set well below the maximum A/D converter count setting. If the threshold is set above the maximum A/D converter count setting, no channels on that chip should indicate a hit. In this manner, a chip in a daisy chain is quickly skipped over (except for chip ID and status).

Downloaded bits 175-182 are used to trim the value of the charging capacitor in the ramp generator of the Wilkenson Converters to correct for changes due to process variations. However, the feedback capacitor in the integrator stage and the ramp capacitor in the A/D converter are fabricated in the same manner. Therefore to a first approximation, gain errors caused by integrator capacitor variations are compensated by similar changes in the A/D converter capacitor. Thus, the ability to adjust the ramp capacitor with high precision may not be needed in later designs.

The Digitize Mode is entered by applying the proper signals to the Change Mode, Mode0 and Mode1 lines. When the Change Mode line goes high, the signals present on BUS0-7 are latched for the previous mode internal signals. (Normally the Acquire Mode will precede the Digitize Mode.) While the Change Mode line is high, Mode0 and Mode1 are set high and the signals on the write through bus, BUS0-7, are set for operation in the Digitize Mode. When the Change Mode line is lowered, the Digitize Mode internal signals are connected to the write through bus and operation in the Digitize Mode can begin.

Operation in the Digitize Mode can be divided into three parts: 1) A/D converter setup, 2) digitization, 3) data compression. During the A/D converter setup, random offsets associated with the comparators are zeroed and a fixed offset is added to the ramp generator output to insure that all the analog comparators are biased off when the ramp begins. During digitization, the Gray Code counter is clocked at a high frequency and digital numbers representing integrated charge are latched for each channel. Finally, during data compression, sparsification of hit information takes place.

The A/D converter setup actually begins near the end of the Acquire Mode and continues into the Digitize Mode. Figure 12 shows four sequential snapshots of the switches around the ramp amplifier and the analog comparator. The first two steps occur during the Acquire Mode and the second two steps occur during the Digitize Mode. To help understand operation, typical voltage levels are shown which might occur with positive input current signals. However, in this figure the input signal is assumed to be zero so that establishment of the ramp offset is easily observed.

In step 1, the comparator and ramp amplifier bias points are established by closing the comparator reset and ramp reset switches while RREF-SEL is set to select RAMP-REF (pad R8). This corresponds to the interval of the pipeline readout in which signal plus pedestal is read out. (See Figure 9). Step 2 shows comparator reset switches being opened to float the comparator. Afterwards the pipeline pedestal is applied to the input. This corresponds to the portion of the pipeline readout where the pipeline pedestal appears at the output of the pipeline. (See Figure 9). In step 3 an offset is applied to the ramp generator output by changing RREF-SEL to choose RAMP-PED which is offset from RAMP-REF by a small amount. This small offset insures that the analog comparator is biased in one state and that the ramp generator must run for a short time before the comparator can flip. Step 4 shows RAMP-RST set to 0 and the ramp beginning.

The ramp offset established by RAMP-PED serves important two purposes. First, the nonlinearity at the start of the ramp generator is passed before any comparator can flip. Second, the value of RAMP-PED provides a fine control for adjusting the noise hits observed at any given threshold level. A 1 mv change in RAMP-PED corresponds to a 400 e shift in the threshold level which has been set. The offset between RAMP-REF and RAMP-PED can cause a count offset at the A/D output if the counter clock is started with the ramp. However, this offset can be largely corrected by delaying the start of the digitizing counter clock until the ramp input to the comparator is nearly equal to the zero signal input level.

Step 4 in Figure 12 shows the comparator input and output signals for a zero signal. Fig-

ure 13 shows the comparator inputs and output for non-zero detector input currents and operation for both positive and negative current inputs. For positive input currents, the RAMP-PED level must be higher (50-100mv) than the RAMP-REF level. An increasing detector signal level produces a negative going signal level at the input to the comparator. The ramp direction is set by a polarity bit to go negative and the output polarity of the comparator is as shown. For negative input currents, the RAMP-REF must be higher (50-100mv) than the RAMP-PED level. An

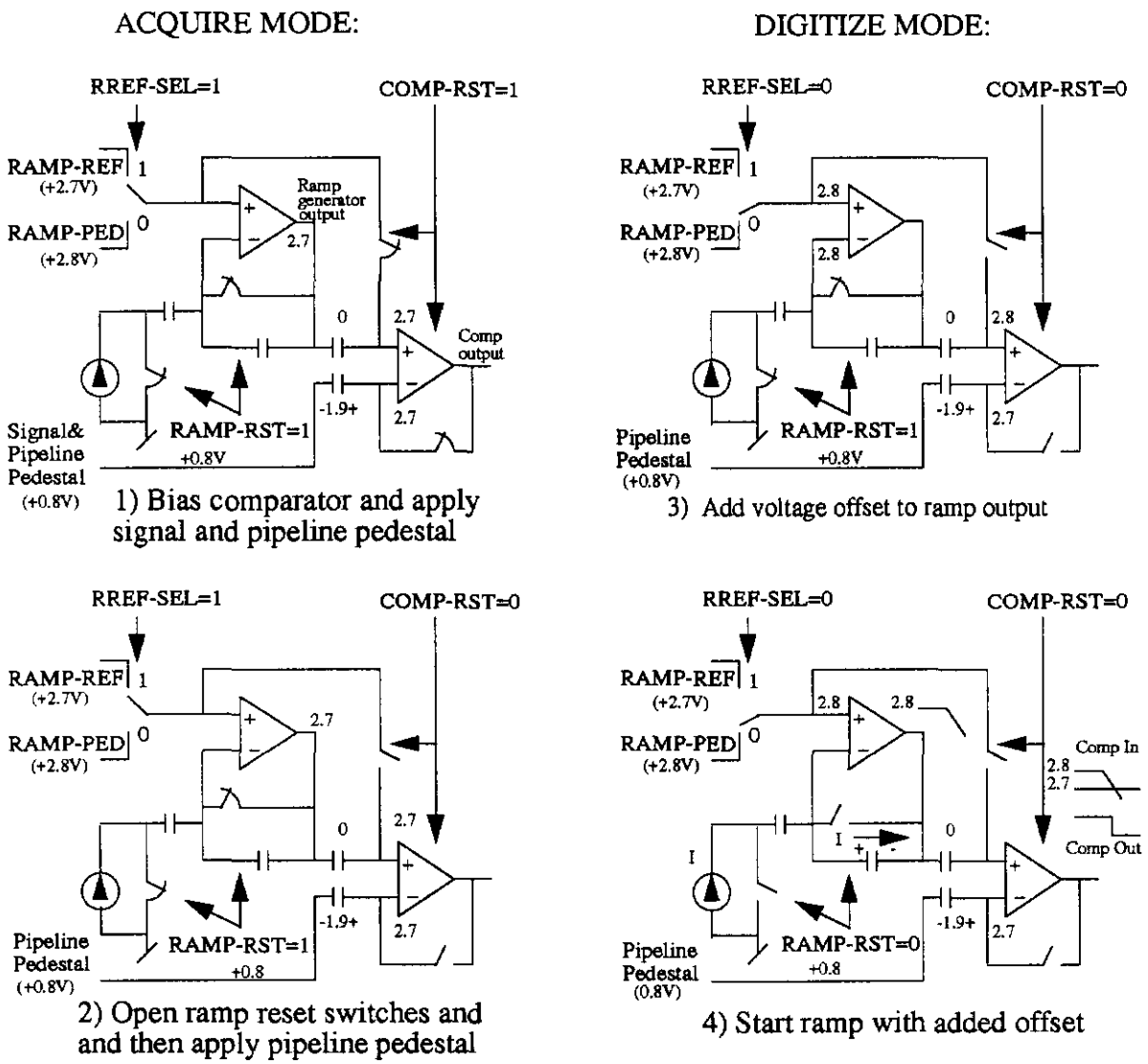


Figure 12 - A/D Setup for Digitization

increasing detector signal level produces a positive going signal at the comparator input. The ramp direction is set by the polarity bit to go positive, and the comparator output is opposite that for positive input currents.

The signals for operation in the Digitize Mode are shown in the timing diagram of Figure 14. The A/D setup period is near the left hand side of the figure. Immediately after the Digitize Mode is entered, RREF-SEL is lowered to add the offset voltage to the ramp output. Then RAMP-RST is lowered to begin the A/D ramp. After a short period of time (to be determined

after testing), CNTR-RST is lowered to start the Gray Code counter.

It should be noted that proper A/D setup and hence digitization requires that RREF-SEL be high before entering the Digitize Mode. With the present design, this cannot be guaranteed for the first digitization cycle after initialization since RREF-SEL has not been set. After the first digitize cycle RREF-SEL will have been set to the correct level and A/D setup is not a problem. In future designs, this "feature" can be corrected by accessing RREF-SEL on BUS1 during the

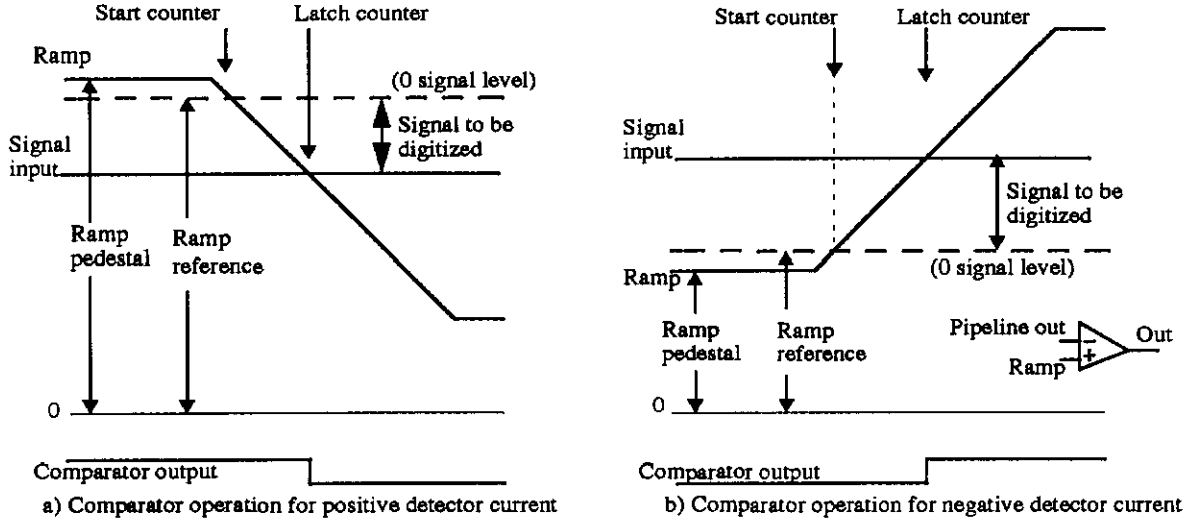


Figure 13 - Analog Comparator Operation

Acquire Mode and moving CAL-INJECT to BUS7 or accessing RREF-SEL on BUS1 during initialization (probably do both).

In Figure 14, the delay between RAMP-RST low and CNTR-RST low is provided to allow the ramp generator output to reach its linear operating region before starting the counter. When the Gray Code counter reset is released, the Gray Code counter begins to count starting from zero. The counter increments on both the positive and negative edges of the counter clock. Thus a 53 MHz clock increments the counter at 106 MHz. In Figure 14, the maximum programmed value for the counter is set arbitrarily at 60. After a few counts, BN is shown going low which indicates that channel 128 on the chip being examined is over threshold (has a hit) and is tagged for readout. (Whenever a hit is detected, the internal logic of the chip determines whether adjacent channels should also be read out. If the Read Neighbor bit was set high, the channel on either side of the hit channel is also tagged for readout. If the Read Neighbor and Read All bits are set low then only the hit channels are tagged for readout. If the Read All bit is high, all channels are tagged for readout as soon as the counter reaches its programmed maximum value.) Two counts after BN went low, TN is shown going low which indicates that channel 128 on the top neighbor chip is over threshold. TN going low means that if the Neighbor Enable is active on the chip being studied, then channel 1 of that chip is tagged for read out.

After 60 counts on the Gray Code counter, any digital latch which has not been previously been set is set to the maximum programmed value of 60. If the threshold for the chip is set to less than 60 counts, then the channels which were set to 60 are over threshold and they are also tagged for readout. The counter clock may continue to run but it has no further effect on the chip. Information (address and digital data) for all of the tagged channels is held on latches in the readout FIFO for further processing.

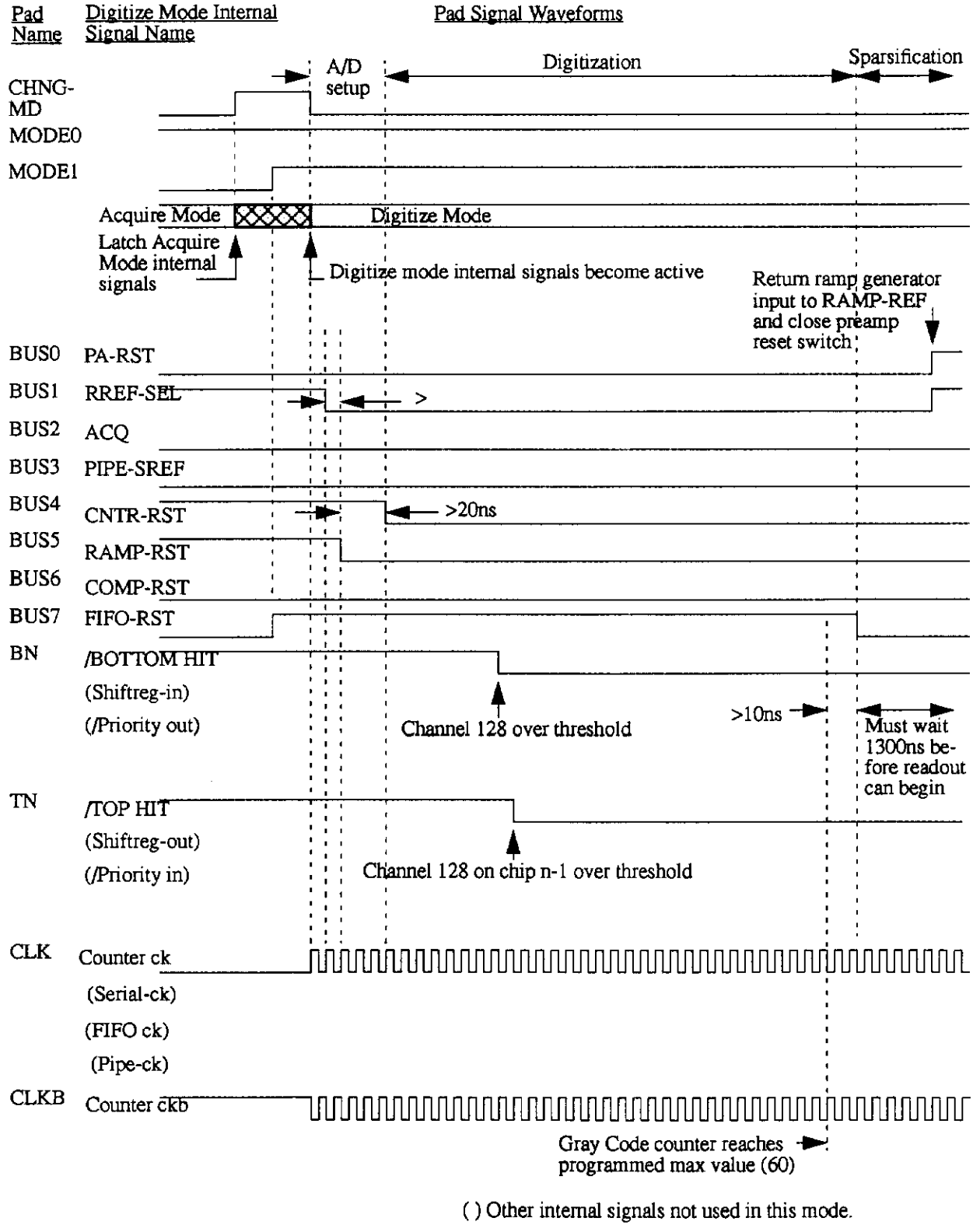


Figure 14 - Digitization Mode Timing Diagram

The time when the counter maximum value has been reached is known in SVXII only from the clock speed and the maximum count programmed into the clock. After it is known that the counter has "maxed-out", FIFO-RST is lowered. (Note in SVXII, FIFO-RST is brought out for added control flexibility. In future submissions, FIFO-RST may be lowered automatically when the counter reaches its programmed level. External control of FIFO-RST then would not be required.) Releasing the reset on the FIFO starts compressing the tagged data (sparsifying the address and digital data) stored on the latches in the FIFO. In a daisy chain configuration, information in all chips will collapse simultaneously. The time for the information to completely collapse is expected to range from 800 to 1300 nsec in the present device. This time is expected to be reduced in future submissions. The clock is no longer needed while information is being compressed. However, the clock may continue to run as shown in Figure 14. While the information is collapsing, RREF-SEL is raised to reconnect RAMP-REF to the ramp generator input before leaving the Digitize Mode. Also PA-RST should be raised to reset the preamplifier in preparation for the next data acquisition cycle which normally occurs after readout.

Readout

After waiting long enough for the FIFOs to collapse, operation of the chip can be changed to the Readout Mode. The mode control lines are used to switch the SVXII into a data readout mode. First, Change Mode is raised which latches the Digitize Mode internal signals (PA-RST, RREF-SEL, ACQ, PIPE-SREF, CNTR-RST, RAMP-RST, COMP-RST, FIFO-RST) with the last levels on the BUS0-7 lines. While Change Mode is high, MODE0 is set equal to 0 and MODE1 is set equal to 1. At the same time, the data acquisition system connected to BUS0-7 should be changed from a data transmit to a data receive condition in preparation for receiving digitized data from the SVXII. When Change Mode is lowered, the internal SVXII data lines are connected to the bus lines provided the chip has received a Priority Input signal. The TN line low indicates that the chip has received a priority input for control of the bus, and that data may be read out on alternate half cycles of a 50% duty cycle clock.

In the Readout Mode, the TN pad is pulled low internally by a 15K resistor and the BN pad is pulled high internally before readout of the chip occurs. After readout, BN goes low.

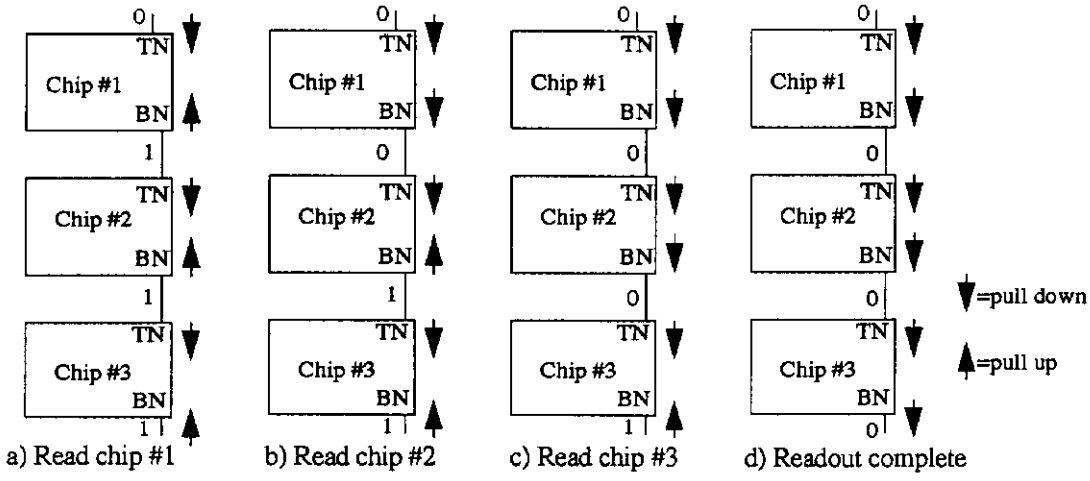
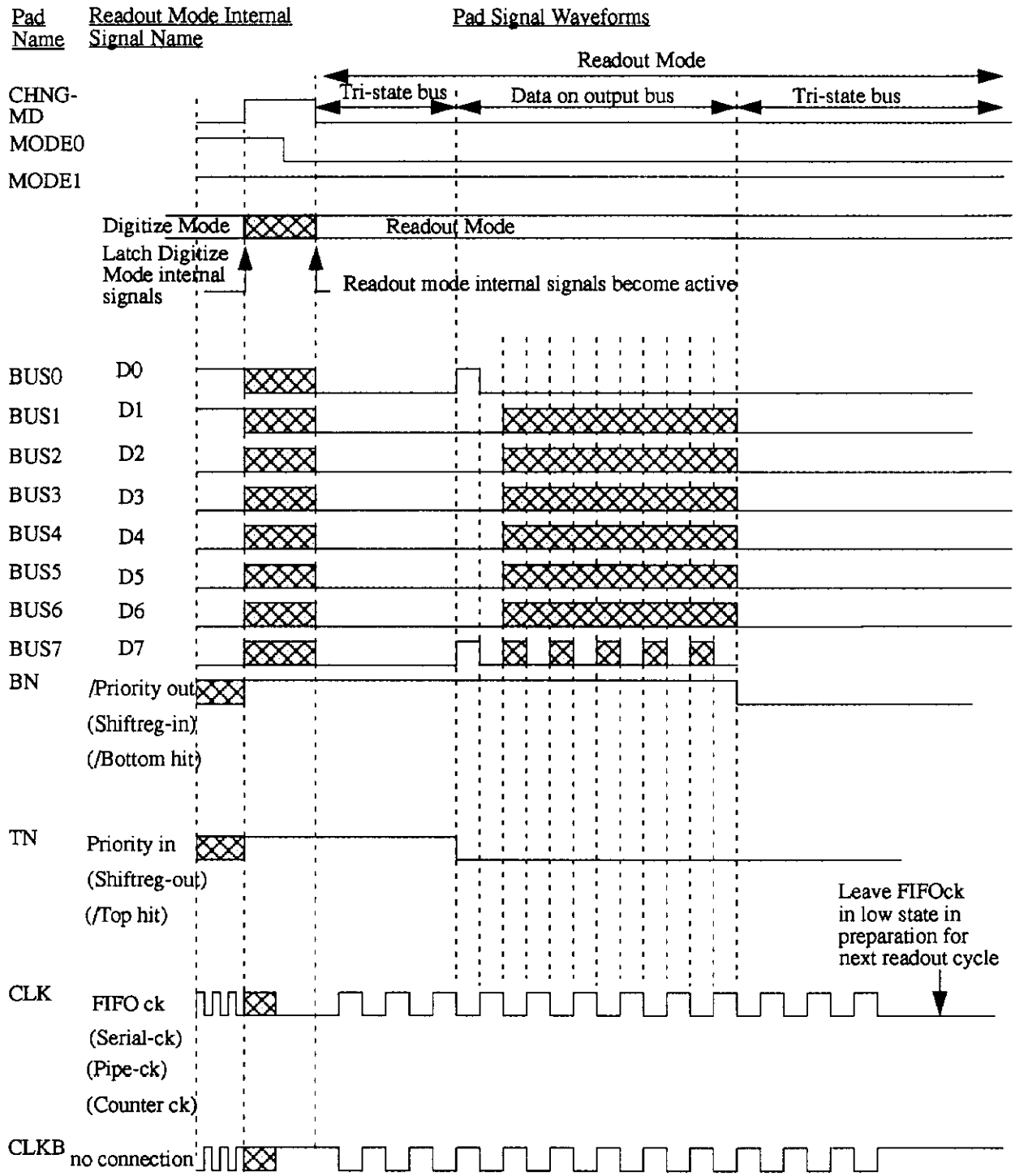


Figure 15 - Passage of priority bit during readout



( ) Other internal signals not used in this mode.

Figure 16 - Readout Mode Timing Diagram for a Single Chip

When a high BN is connected to a low TN as occurs with daisy chained chips, the TN pad is pulled high (wired-or). Figure 15 shows how the priority bit is passed in a three chip daisy chain readout. Passing the priority between chips requires 1-2 nsec.

Figure 16 shows a timing diagram for readout of a single chip. Since TN is pulled low internally, readout of a single chip could begin as soon as TN falls (TC=15k x Cext) after entering the Readout Mode. However in Figure 16, TN is externally held high to inhibit readout for a few clock cycles. (TN high holds the data bus in a tri-state condition.) TN must be lowered on a falling clock edge (FIFO ck) to read out chip information in the proper sequence. (If readout commences immediately after entering the readout mode, the Change Mode line must go low on a falling edge of FIFO ck.) In Figure 16, chip ID (0000001) is read out first followed by a status word (00000000) and then digitized data and address. When all of the desired information is readout from the chip, the Priority Out signal on BN goes low. If the clock continues to run after all data is readout, the output data bus once again enters a tri-state condition.

In the Readout mode the FIFO clock line must be low for a few nsecs before a chip receives its priority input. If it is not, the Chip ID number for that chip may be skipped during readout. The only way to insure that FIFO clock is low prior to entering the readout mode is to leave the Readout Mode with FIFO clock low as shown in Figure 16. Since FIFO clock is set in a random state (high or low) during chip power up, the chip ID could be missed on the first readout cycle. On subsequent chip designs, the FIFO clock should be set low during initialization to insure proper chip ID readout on the first readout cycle. Also note that to avoid any possible glitches upon entering the Readout Mode, the CLK line is brought low prior to entering the Readout Mode as shown in Figure 16.

In the SVXII chip, information is read out using both the high and low levels of the differential clock. When a chip receives a priority input signal and the clock is running, the 7 bit chip ID # is placed on the BUS0-6 pads during the first clock low level. (The BUS7 pad will always be high when the chip ID# is read out.) On the following high half cycle of the clock, an 8 bit status word for that chip (currently 00000000 for all chips) is read out. After the chip ID and status

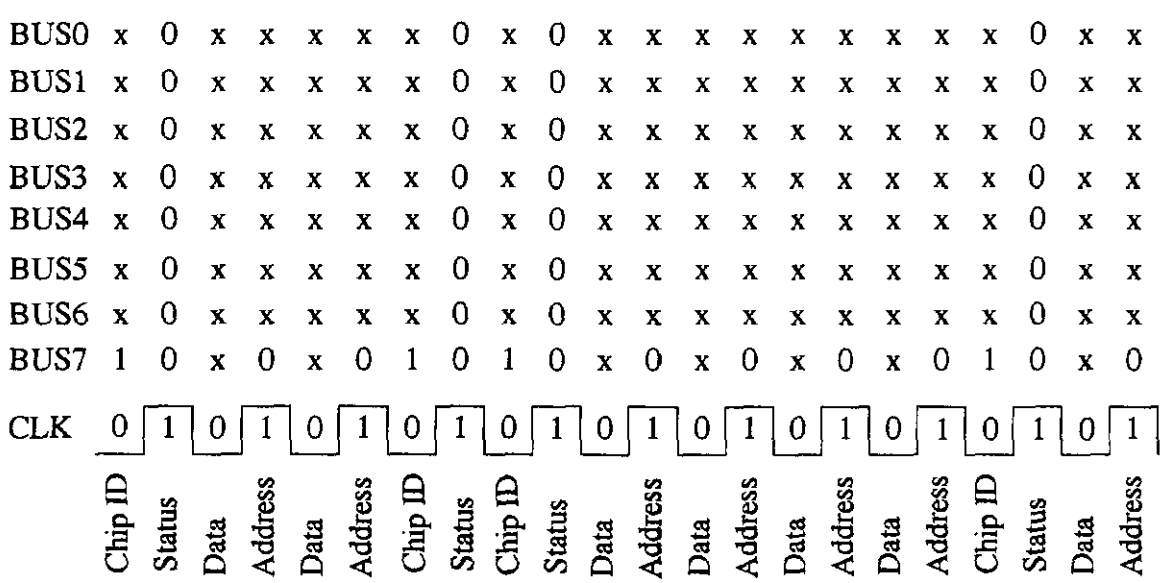


Figure 17 - Typical output bus data for several chips

have been read out, digitized data and address follow on the subsequent low and high clock levels until that chip has been completely readout and the priority is passed to the next chip. (Since there are only 128 different addresses on a chip, the address MSB bit will always be 0.) If a chip receives a priority input and there is no digital data in that chip for readout, the 16 bits for chip ID and status are read out in one low/high cycle of the clock and then priority is passed to the following chip. For clarification, a typical output bus data pattern for daisy chained chips is shown in Figure 17. It is expected that in future designs the order of the digital data and address readout will be reversed. Thus, when the output clock is low and the output bus MSB is high, the chip ID will be read out. And when the clock output is low and the output bus MSB is low, a channel address for that chip will be read out.

Miscellaneous Considerations

Chip initialization is expected to occur infrequently. The parameters for the chip setup are held in static latches which are not expected to change until the next initialization. One of the parameters set in the latches is the analog time delay which is an offset between the read and write pointers in the analog storage section. Once the chip leaves initialization, these two shift registers on all of the chips in a system could be clocked at a 7.6 MHz rate for an indefinite period of time. This amounts to 1xE13 to 1xE14 clocks per hour in a relatively large system. If a glitch (ringing, infrequent coincident noise sources) occurs on a clock line somewhere in the system, the electrical delay for one or more of the chips could be incorrect leading to scrambled data. Although this should be unlikely, the results could be messy. One way to check the integrity of the data is to use the test input feature and readout all chips. The input test mask should be loaded for one hit channel per chip and pulsed during an acquisition mode beam gap. After the appropriate delay time, all the chips should be read out. If channel 1 was pulsed and the Neighbor Enable is active, three channels per chip (1, 2, 128) would be read out and the neighbor hit feature would also be checked. If any chip does not read out hit information, the time delay may be incorrectly set, and previous data from that chip should be suspect. A test of this nature may be warranted either once an hour or once a minute depending on experimental results in the actual installation to provide confidence in the data integrity.

If the Counter CK and Counter CKB in the Digitize Mode are ever high at the same time, the counter clock oscillates creating noise on the chip. Under normal operating conditions Counter CK and Counter CKB should never be high at the same time. However upon power up, the internal latches for these clock signals are set in random states and even initialization does not clear them. Only after going through the digitization mode for the first time and leaving the digitize mode with the clock lines in the correct states can the latched Counter CK and Counter CKB states be guaranteed to be correct. Thus any data from the first digitization cycle should be suspect. This condition can be corrected in later versions of the chip by setting all of the internal clock latches to acceptable levels during power up or initialization.

SUMMARY OF MAJOR FEATURES

The SVXII has several unique features. These features have been described in detail in this document. Those features along with other significant features that have been mentioned are listed below for reference purposes.

1) 128 channels per chip
2) Maximum interaction rate equal to 132 nsecs
3) Separate acquisition and readout cycles
4) Double correlated sampling
5) Large dynamic range
6) Programmable depth analog pipeline (32 cell maximum depth per channel)
7) Digitization of analog signals to 8 bits of resolution
8) Data sparsification (zero suppression)
9) Neighbor channel readout selection
10) Low noise (S/N=10 to 20:1)
11) Low power (approximately 3 mw/channel)
12) Operation compatible with doubled sided AC coupled detectors
13) Separate test input for each channel
14) Daisy chain operation capability
15) Parallel bus data readout
16) Numerous programmable internal registers (chip ID, preamp risetime, threshold level, etc.)

Actual performance of the SVXII will be described in a separate document after testing of the device has been completed.

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