Fermi National Accelerator Laboratory

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Fermilab Physics Department TVC Chip

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Abstract

The Electronics Group in the Physics Department at Fermilab has designed and has had produced 20 prototypes of a full custom four channel time to voltage converter using the ES2 direct write 2 μm CMOS process. The actual implementation of the design was performed under contract by ASIC designs Inc. of Naperville, Illinois. Each channel has two hit capability and one level of input buffering; that is, up to four voltages representing time intervals can be stored from each input for later ADC conversion. The chip produces an edited list of hits and presents the appropriate analog value on its output for each digital value on its hit address lines. The next hit address and analog voltage in the event is presented in response to an external strobe. One current sum proportional to the number of inputs hit for each input buffer is also provided. The chip has been designed to be used on a fastbus TDC card developed here, but it is our belief that it could be adapted to many TDC applications.

Design Goals

The Physics Department TDC was designed for data aquisition systems operating at tens of thousands of events per second. To achieve these rates, the bandwidth of the available data channels must be used efficiently. The first way to increase effective bandwidth is to zero suppress the data at as early a stage in the acquisition heirarchy as possible; the second is to absorb event rate fluctuations to reduce peak bandwidth. To that end, the TDC does zero suppression on card and is outfitted with one level of analog input buffering (which is implemented on chip) and a four event output data buffer memory attached to the bus interface. Secondary design goals were to minimize board complexity and reduce power consumption. The TVC is fabricated in CMOS. As a result, 64 channels of TVCs dissipate approximately one watt. All the analog circuitry on the TDC board is contained in 16 of these chips which as a group are the equivalent of 250 SSI analog and digital chips.

Operation

The chip can be divided into six sections: input flip flops and steering logic, 16 precision switched current sources with integrating capacitors, 16 simple current switches for multiplicity sums, hit map latches, hit editing logic, and output addressing logic.

Inputs

The TVC is designed to be common stop only. Each input is connected to the clock pin of two D flip flops. The Q output of the first flip flop is "and"ed with the 2HIT (two hit enable) line then attached to the D input of the next. One flip flop toggles on the first hit, the other on the second. The common stop line is attached to the direct clear line of both flip flops. A second pair of flip flops identical to the first is provided for the second

event. IBSel (Input buffer select) is attached to the D input of flip flop one of event one, while $\overline{\text{IBSel}}$ is attached to flip flop one of event two. Changing the level of the IBSel line then performs the input buffer swap. By duplicating the entire input circuit, swapping between sections can be done very quickly. The Q outputs of each flip flop goes to both hit map latches and the precision switched current sources. A detail of one channel of input is shown in Fig. 1.

Precision Current Switches

The principle of operation of a TVC circuit is that of a constant current injected onto a capacitor with a linear V(q) characteristic for the time interval to be measured. Assuming a constant charge current, the voltage V developed across the capacitor can be measured and the unknown time interval can be taken from the expression:

$$T = (C/I) \bullet V \tag{1}$$

In this version of the TVC circuit (Fig. 2), the gate of a large geometry (6000 μm x 10 μm) transistor (U10) has been used as the integrating capacitor. The ratios in Fig. 2 next to each transistor are its gate width to gate length ratio. Simulation results predict a value of approximately 70pF for U10's gate capacitance with minimal dependence of capacitance upon gate voltage in the range of 1.2 to 4 volts. To provide a constant current independent of the voltage developing across the charging capacitor, a triple cascode configuration has been employed.

The expression for the drain current ID of a MOSFET working in the saturation region shows a dependence on the drain to source voltage VDS:

$$I_D = K \bullet W/L \bullet (V_{GS} - V_t)^2 \bullet (1 + \lambda V_{DS}). \tag{2}$$

where K is a process dependent constant empirically determined, W is the gate width, L is the gate length, V_t is the minimum gate to source voltage required for channel current flow (threshold), V_{DS} is drain to source voltage V_{GS} is gate to source voltage and λ is the channel length modulation factor. In the small signal equivalent circuit this dependence is accounted for by a resistor of value r_{ds}, connected across the drain and the source terminals. A SPICE simulation for transistor U4, for instance, shows that $r_{ds}4$ is about 10 KOhms. U4 has too low an output impedance to be used to charge U10's gate directly, because $r_{ds}4$, effectively in parallel with the integrating capacitor, would shunt an excessive amount of current past the capacitor as the output voltage increased. In the cascode arrangement used here, the output impedance of U4 is amplified by U5 and U6. A circuit analysis based on simplified transistor models shows that the output impedance at the drain of U6 should be:

$$r_{ds}4 \bullet (g_m5 \bullet r_{ds}5) \bullet (g_m6 \bullet r_{ds}6): \tag{3}$$

where the transconductance parameter, g_m, defined as:

$$g_m = dI_D/dV_{GS}: \tag{4}$$

is in turn given by the expression:

$$g_m = 2 \cdot K \cdot (W/L) \cdot (V_{GS} - V_T) \cdot (1 + \lambda V_{DS}): \quad (5)$$

or

$$g_m = 2\sqrt{K(W/L)I_D}. \quad (6)$$

The expression for g_m shows how the transconductance of a MOS device depends on its geometry. Minimum geometry (2 μm for the process used) transistors were chosen to minimize leakage currents and switching times. The resulting low values for g_m however, necessitate the adoption of a three stage cascode to produce the desired output impedance. The operating points of U4 and U5 are adjusted to achieve maximum output voltage range.

Since the magnitude of the operating current is unknown to approximately 20% due to process variations, the drain current of U4 is obtained by mirroring I_{D1}, which in turn is set by an externally adjustable input current (I_{ADJ}). The V_{GS} of a MOS transistor working in the saturation region, is somewhat larger than V_t. Using expression 2 for I_D, that difference can be expressed as:

$$\Delta V = V_{GS} - V_t = \sqrt{L/W} \cdot \sqrt{ID/K(1 + \lambda V_{DS})}. \quad (7)$$

The geometry of a MOS transistor is a factor in determining its ΔV and this property has been exploited in the biasing of the current source. In the interest of simplicity, the following operating point analysis neglects the effect of V_{DS} on ΔV. I_D for U1, U2, U3, U4, U5, U6, and U13 have approximately the same value. Since V_t is closely matched for adjacent transistors on the same substrate, they (the above transistors) have matched ΔV's. For optimal biasing, the drain to source voltages of U4 and U5 should be kept close to ΔV_4 and ΔV_5 which as a result of our approximations we consider equal to ΔV_1. Because of the square root relation between W/L and ΔV, $(W/L)_{U1}$ is 100/2, about 9 times larger than $(W/L)_{U11}$ which is 22/4. ΔV_{11} is then $\sqrt{100/11}$ or approximately 3 x ΔV_1. The difference in W/L for U12 and U1 is 4:1 which means ΔV_{12} is twice ΔV_1. It follows then that the bias for U4 is:

$$V_{DS4} = \Delta V_4. \quad (8)$$

which is the minimum value required to maintain U4 in the saturated operation region. U5 is working at minimum V_{DS}:$V_{DS5} = \Delta V_5$. This biasing scheme allows the output voltage to swing as high as:

$$V_{OUT\ MAX} = + V_{DD} - 3 \cdot \Delta V_1. \quad (9)$$

Simulation results show that $\Delta V_1 = 170$ mV, V_{DS4} is 255 mV and V_{DS5} is 205 mV for $I_{ADJ} = 70\ \mu A$ and that the integrating voltage can rise to within 0.7 volts of V_{dd} before the current source loses a significant fraction of its output impedance.

Current has to flow on the integrating capacitor only for the time interval to be measured, so transistors U7 and U8 are used to steer the current from U4 to an alternate path between events. Normally the digital signal VCNTRL is low and the transistor U8 is turned ON. The current from U4 flows through U7 and U8 to the VCLAMP node (defined by an on-chip bandgap voltage reference). VCLAMP is also used as the input reference voltage for the single supply amplifier buffering the integrator's output. The bias of U7 is chosen to be positive enough not to drain away any current from U5 when the voltage is ramping up on the capacitor, and negative enough to insure that all the current of U4 goes through U7 when the switch is off. U5 and U7 form a differential pair and the unbalance of the gate voltages amounts to:

$$V_{G5} - V_{G7} = V_t + 2\ \Delta V_1. \qquad (10)$$

During the measuring interval VCNTRL is low and I_{D4} is directed to the integrating capacitor. The voltage on U10's gate is held until the external DUMP signal is asserted high, turning U9 on and resetting VG10 to the initial value VCLAMP. Because the circuitry of the input node of the buffer amplifier is entirely inside the chip, no static discharge protection circuitry is required. The leakage currents from that node are accordingly very small, which in turn means that droop rate for voltages stored on the capacitor are very slow. The measured droop rate from the chip is less than 1V/sec. A transient analysis of the circuit produces the following results:

I_{DS} rise time (T_r):	5 nsec
VCNTRL to I_{DS} 50% on propagation delay (T_{pd}):	10 nsec
0.01% settling of V_{G10} to VCLAMP after a DUMP low to high transition (T_{rst}):	50 nsec

The testing of the chip which contains 16 of these TVC cells produced results in good agreement with the data obtained by the simulation. Figure 3 shows the slope of transfer function for half of the 16 TVC cells in the chip. An integral non-linearity of 3 nsec over a 2 μsec full scale and a differential non-linearity of 0.6 nsec has been measured using a small number of the channels for a data sample. The measurement consists of recording the output voltage across the full scale time range in 50 nsec increments. DV/DT is discretely approximated then by $\Delta V/\Delta T$. The differential non-linearity is measured by histogramming the ΔT values. The integral non-linearity is defined as the largest deviation from a straight line fit to the transfer function. The integral non-linearity tracks very closely channel to channel, so that if higher resolution was needed, a fit done to the transfer function would yield sub nanosecond resolution. However, these chips are for the present intended for use with proportional drift chambers, whose resolution is generally limited by ion diffusion effects to 8 bits of precision or less. As an example, the D0 muon proportional tubes have a drift distance of 5 cm. The best resolution so far obtained is 100 μm σ very near the wire (< 3 mm) and 300 μm σ in the region farthest from the wire.

Multiplicity Sums

A set of simple current switches are used to form hit multiplicity sums. The sums for hits of a given event from four channels are "or"ed together with open drains. This common point is brought to a pin on the chip. There is then one sum out for each event. The multiplicity switches are formed with only one transistor as a current source and two others behaving as analog switches. The magnitude of the current is set by the control current ISET. The ratio of W/L between U1 and U2 is 15 to 1. Thus the ratio ISET to the output current is $\sqrt{15}$ or 4. The output impedance of the switch is on the order of 10K Ohms, the assumption being that these outputs will need to be buffered off chip. Figure 4 shows the multiplicity switch circuit. Since the inputs to the sums come from the hit latches, the sums stay valid until a new event is triggered for a particular input section. Implementing independent sums for each input buffer allows any trigger processor using the sums to be double buffered also.

Hit Latches

The input flip flops contain a map of the hit channels, however they are cleared at the end of the time measuring interval. In order to preserve the hit map for use by the multiplicity sums and the hit editor, one 8 bit latch for each event is implemented. The latches are transparent and use TSTOP delayed by the hold time of the latches as the latch enable signal. The outputs of the latches go to an octal 2 in 1 out selector. The output of the selector is routed to the hit editor. The signal OBSel (Output buffer select) directs one of the two latched events to the input of the hit editor. A diagram of the latch section is shown in Fig 5.

Hit Editor and Output Logic

The hit editor consists of 8 flip flops with a common clock called NXTHit (Next Hit) whose outputs are connected to an 8 line to 3 line priority encoder. The logic for this section is shown in Fig. 6. Data from the hit map latches is asynchronously loaded into the flip flops with the PLoad (Parallel Load) signal. The encoded address is routed to 3 tri-state buffers, the low order 3 bits of a 4 line to 16 line analog selector and a 3 line to 8 line decoder. Each of the 8 ouputs of the decoder is fed back to the corresponding synchronous reset of the 8 flip flops. With this arrangement, the highest priority address is cleared and the next highest priority address appears at the encoder outputs after each clock. The integrating capacitor voltages after going through a unity gain buffer are presented to the input of the analog selector. The OBSel line is the high order address bit for the selector, so that the same event loaded into the hit editor is routed through the analog selector; the result being that the analog voltage present on the output of the selector corresponds to the hit address coming out the address lines.

A carry in and carry out line are used to synchronize multiple chips whose output address lines are bussed. The carry outs of the chips can be priority encoded externally to form higher order address bits. The carry out bit is asserted (conditional on carry in) when there are zero hits or 1 hit remaining. This allows the internal enable for chips on a carry-in/carry-out chain to to travel from chip to chip synchronously with NXTHit common to all the chips. After an initial settling time of 2 μsec for the integrating capacitor buffers, readout proceeds at 1.4 μsec for each hit. A timing diagram of a read out operation is shown in Fig 7. The upper portion of the figure is a record of the digital signals, while the lower is the analog output. Two events are shown, the first with hits on all channels, and the second with hits on hit one of channels zero, one, and two. To illustrate the double buffering, the second event occurs while the first event's read-out is in progress.

Test Features

The chip has 4 pins reserved for test functions. Pin TST0 is test enable. When this pin is pulled low, pins TST1, TST2, and TST3 are routed to the select lines ouput analog multiplexer in place of the hit editor logic. This allows each of the integrator voltages to be examined regardless of the state of the internal control logic.

Mechanical

The prototype chips are packaged in a 40 pin dual in line ceramic package. ES 2 has a number of packaging options, including leaded and leadless chip carriers. We chose the D.I.P. package because it was cheapest, and since the chips already saved so much board area as opposed to the discrete prototype, we felt no need to minimize package size. A pinout diagram of the chip is shown in Fig. 8.

Cost

The quoted piece price for volume quantities of chips as of June 1990 are $21 for quantity 2000 and $15 for quantity 5000. Delivery is five to six weeks after receipt of order.

Conclusion

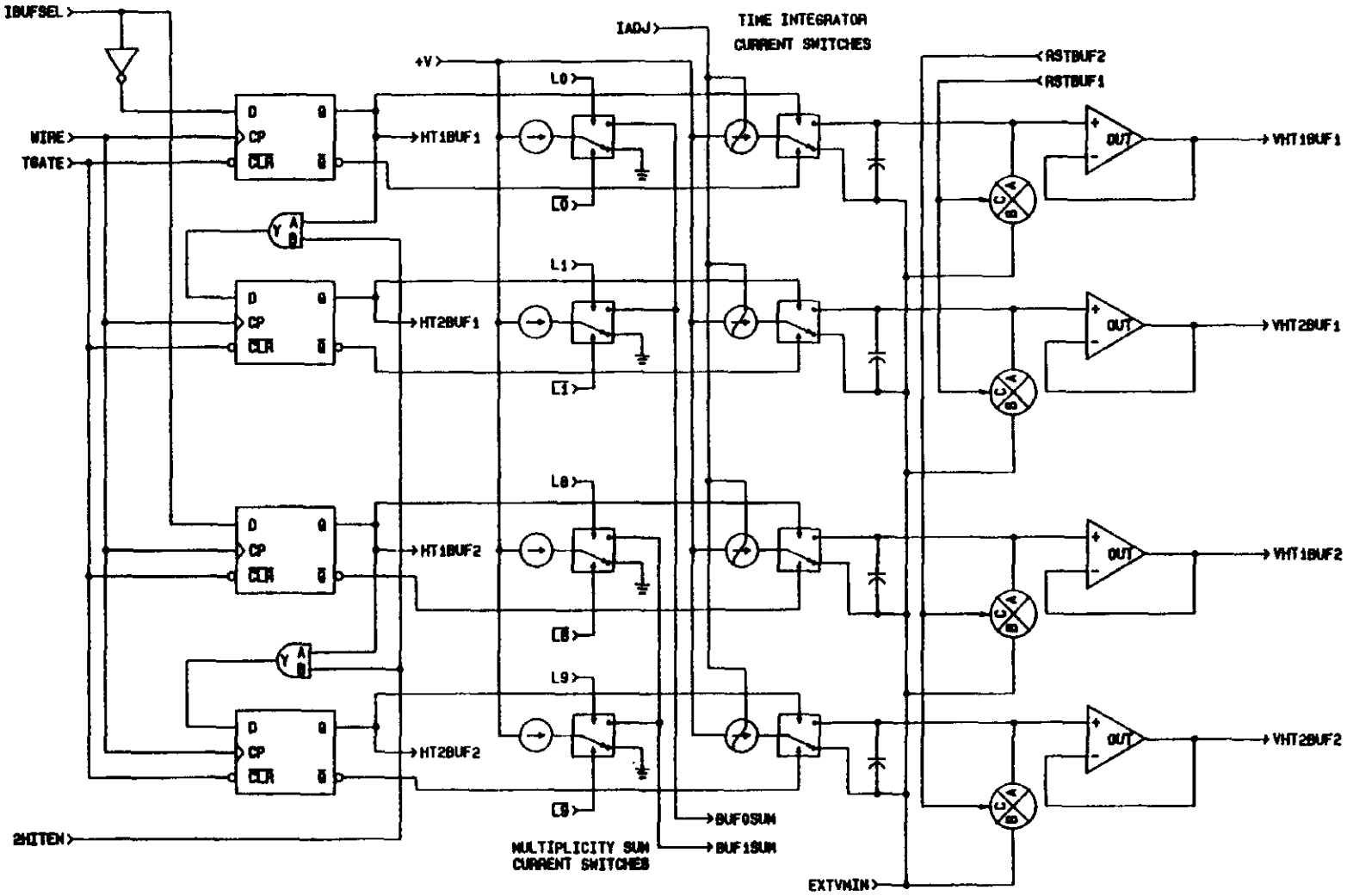
In fixed-target experiments at Fermilab, wire chamber systems have an occupancy of 10% or less. This translates to an average mulitplicity of 7 hits per 64 channels on average. If we can assume that the buffers on the card are capable of averaging the event to event multiplicity fluctuations, then the hits can be read out in about 10 μsec. There are in fact 2 ADCs on the board, but we assume here that in the worst case all the hits occur in the channels attached to one of the ADCs. If a fastbus crate is filled with TDCs, and each hit generates a 16 bit data word, this translates to a sustained bandwidth of close to 20 Mbytes/sec. With this kind of available bandwidth, it should be some time before these modules become the system bottleneck.

References

[1]Analysis and design of analog integrated circuits. 2nd Ed. Paul R. Gray, Robert G. Meyer. John Wiley and Sons.

[2]Physics of semiconductor devices. S.M. Sze. John Wiley & Sons.

FIG. 1



FUNCTIONAL SCHEMATIC OF 1 INPUT CHANNEL

FIG. 2

MINIMUM GEOMETRY TRIPLE CASCODE CURRENT SWITCH

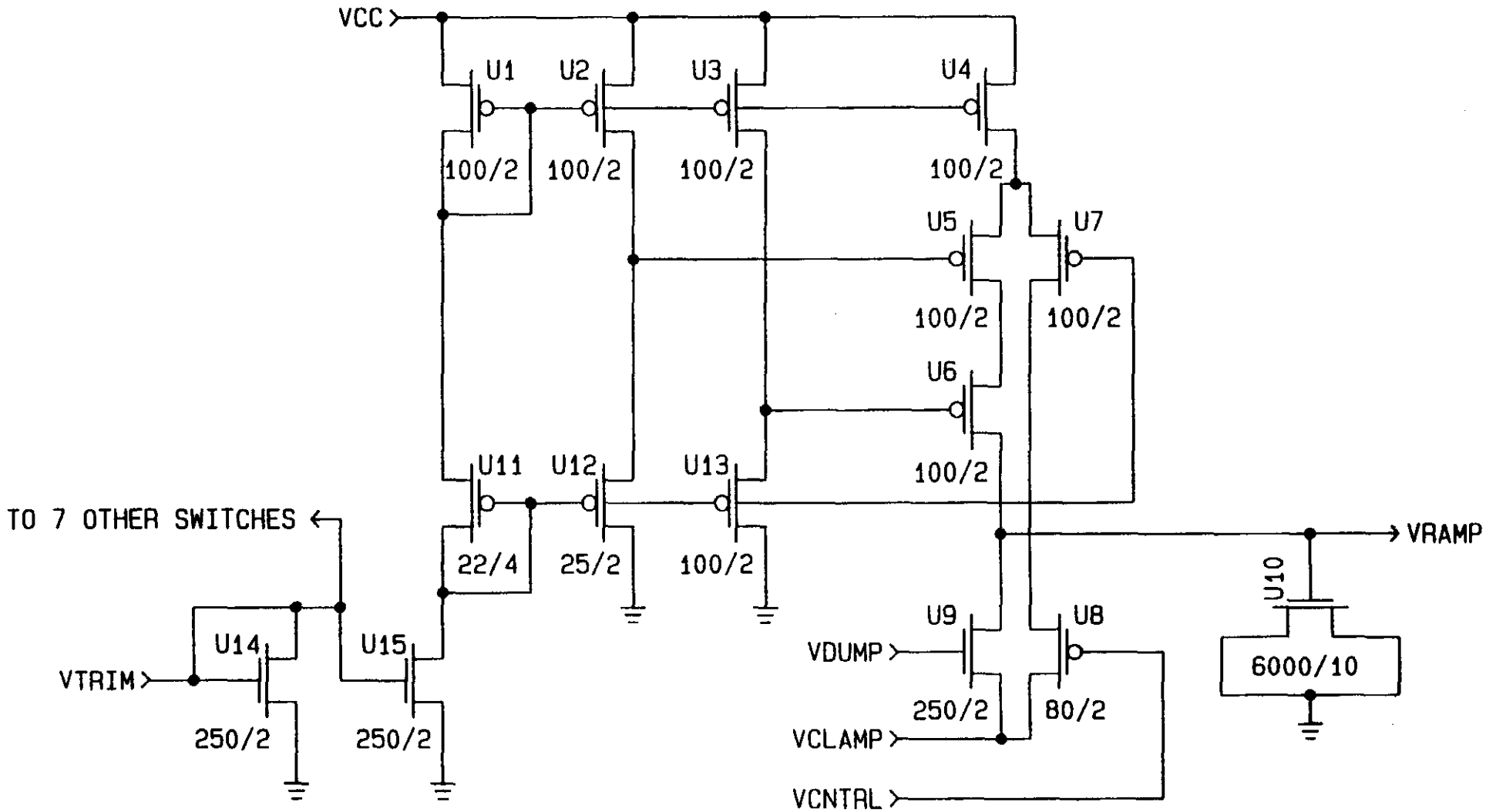


FIG. 3

volts/uSec vs uS for 8 integrators on 1 chip

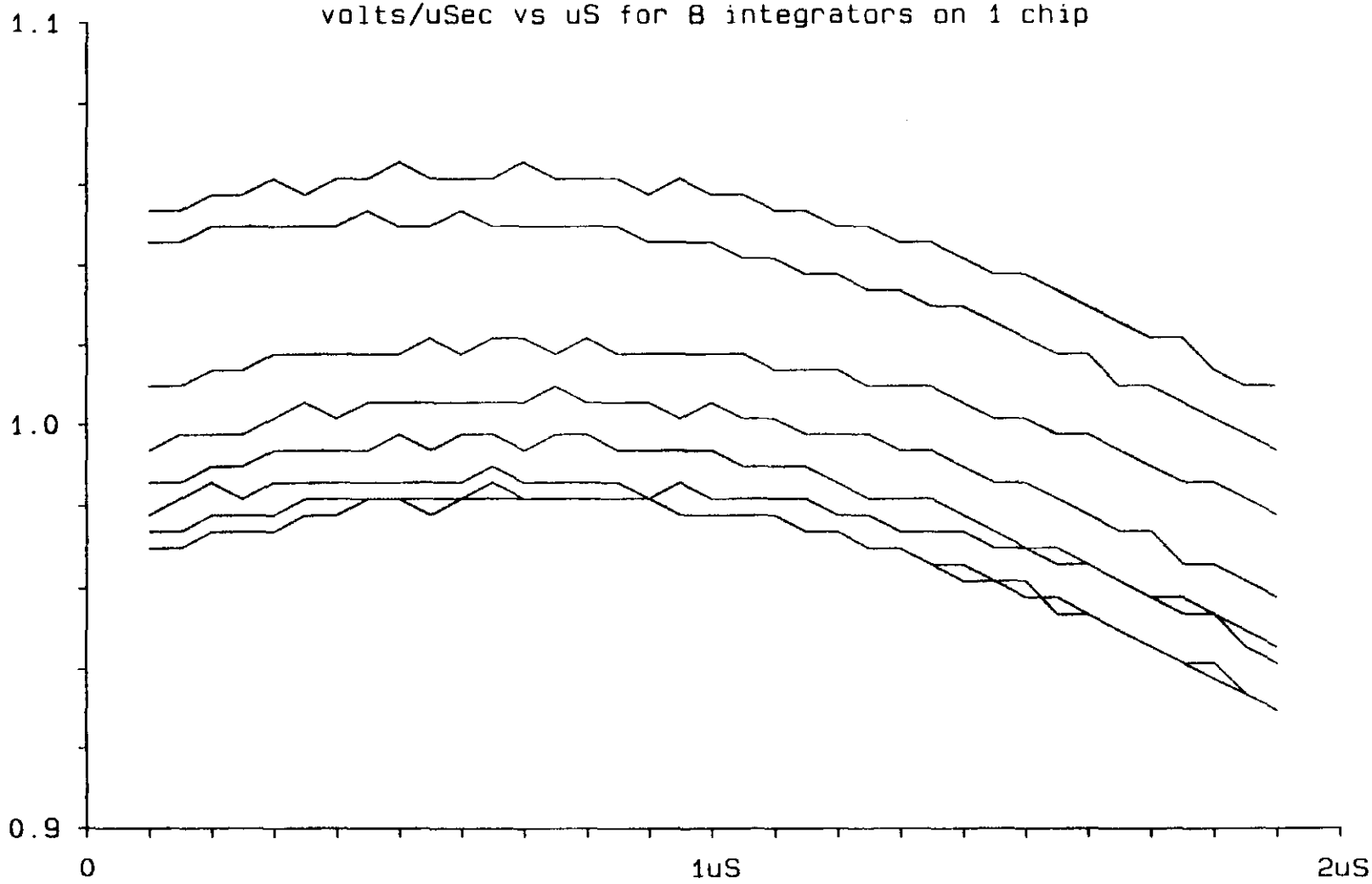
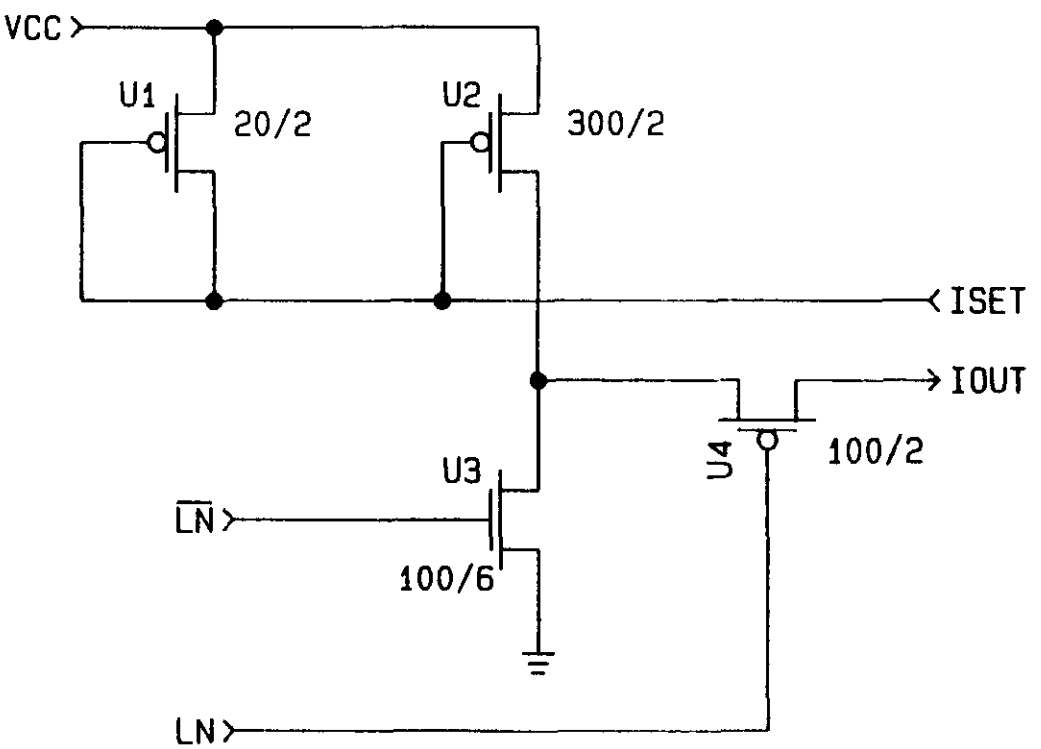


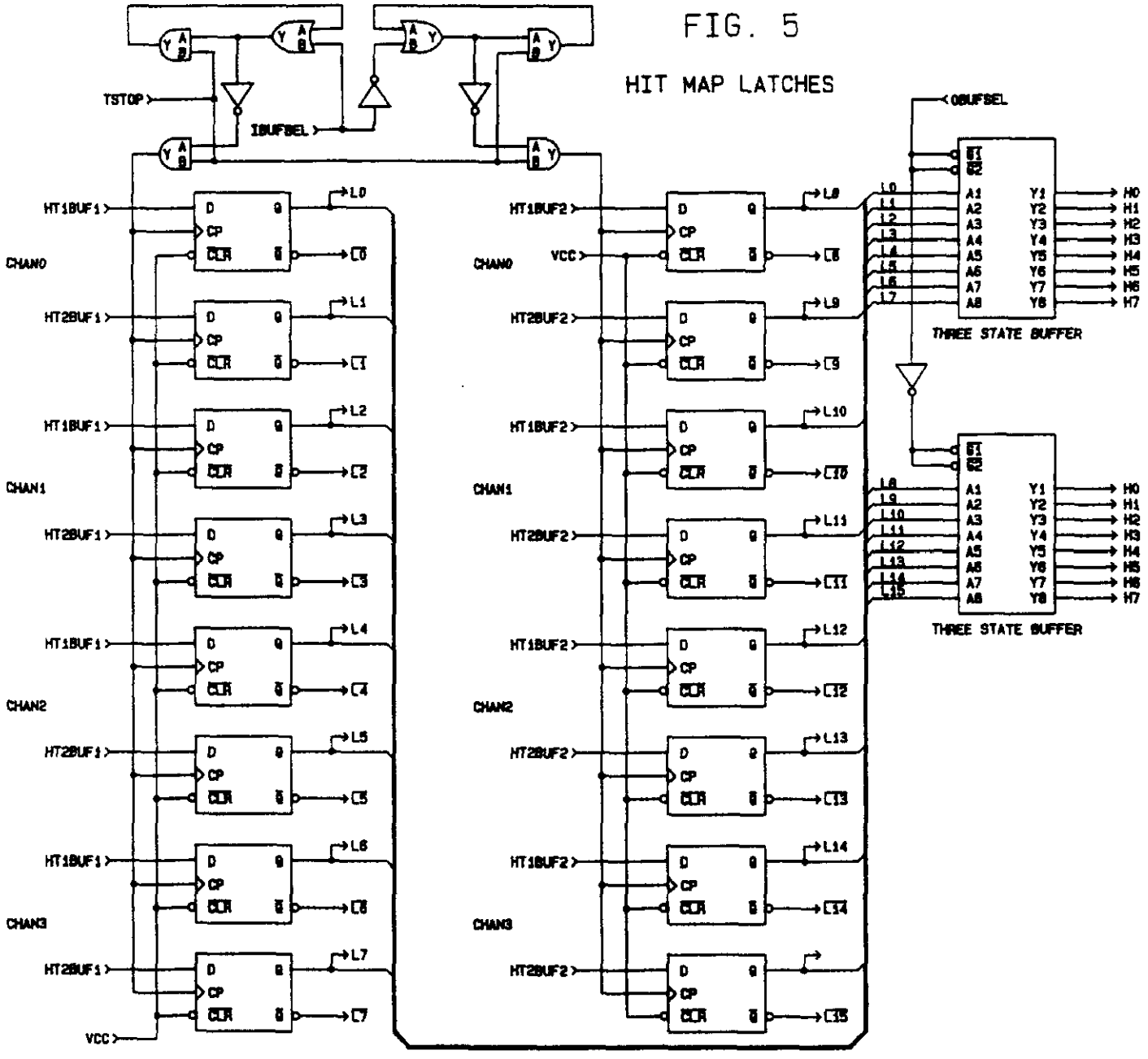
FIG. 4



SIMPLE CURRENT SWITCH
FOR MULTIPLICITY SUMS

FIG. 5

HIT MAP LATCHES



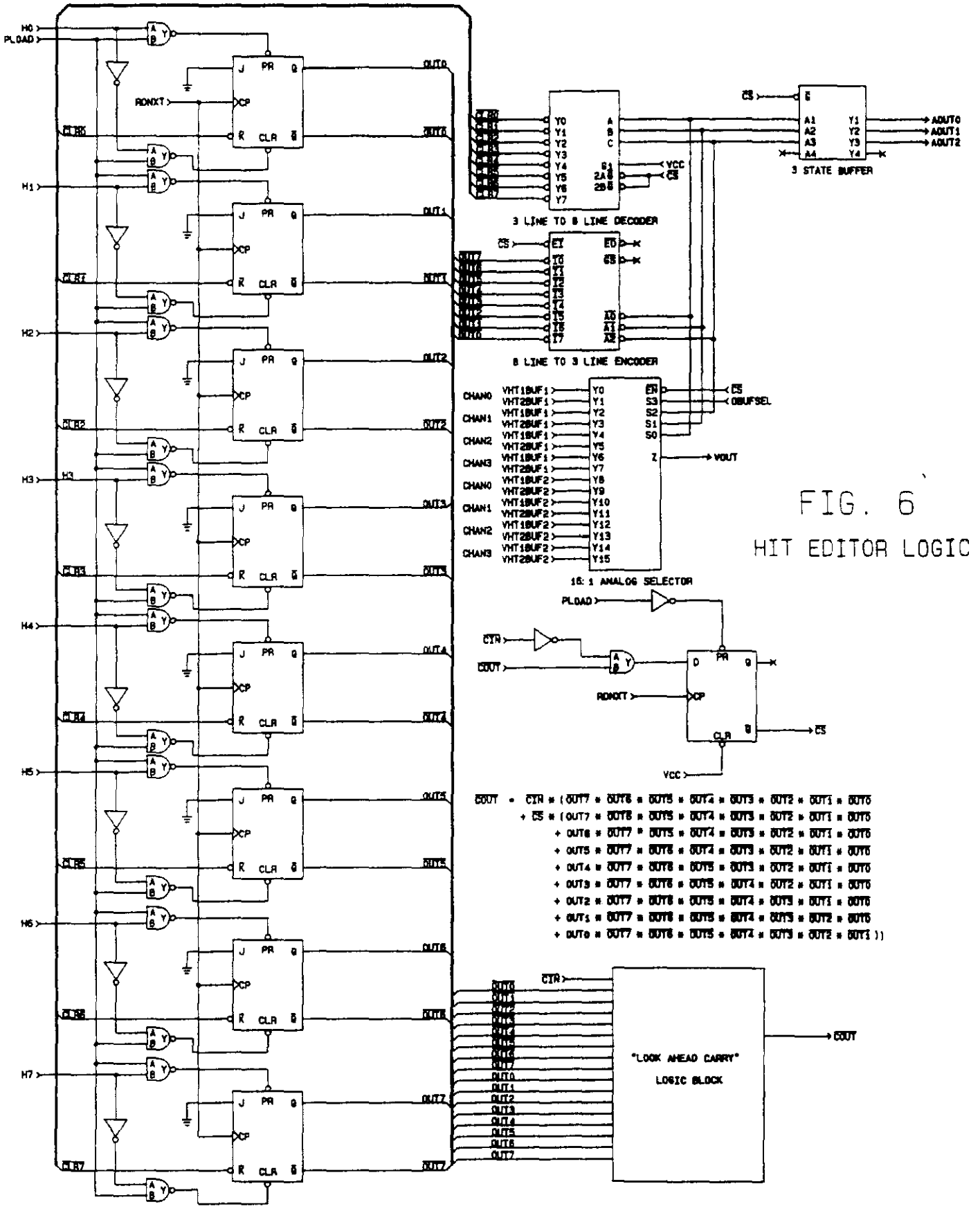
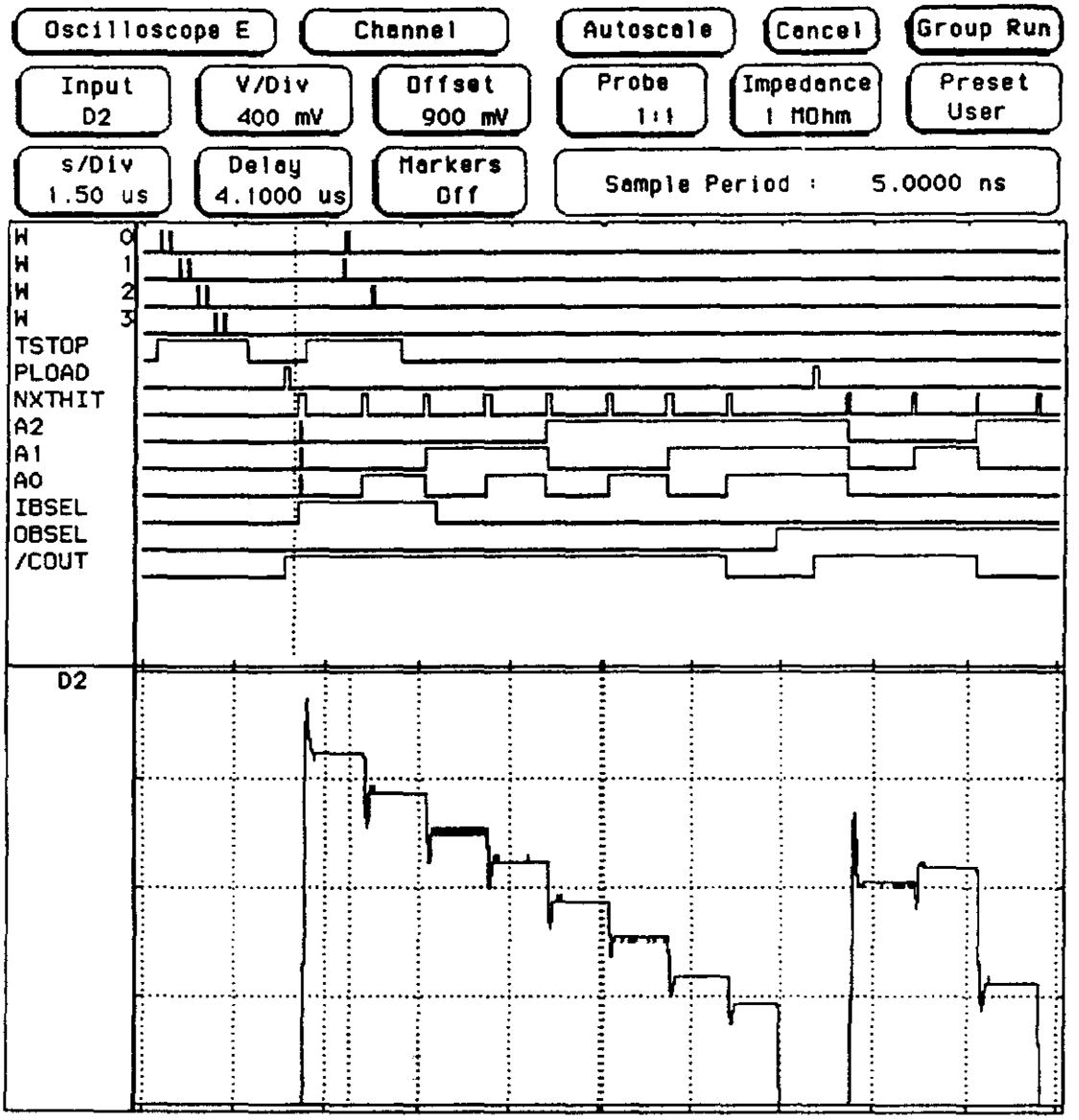


FIG. 6

HIT EDITOR LOGIC

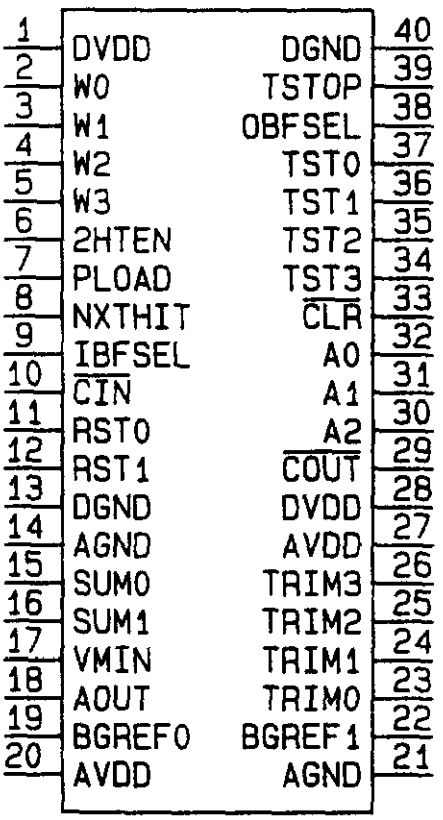
COUT = CIR * (OUT7 * OUT6 * OUT5 * OUT4 * OUT3 * OUT2 * OUT1 * OUT0
+ CS * (OUT7 * OUT6 * OUT5 * OUT4 * OUT3 * OUT2 * OUT1 * OUT0
+ OUT8 * OUT7 * OUT5 * OUT4 * OUT3 * OUT2 * OUT1 * OUT0
+ OUT5 * OUT7 * OUT6 * OUT4 * OUT3 * OUT2 * OUT1 * OUT0
+ OUT4 * OUT7 * OUT6 * OUT5 * OUT3 * OUT2 * OUT1 * OUT0
+ OUT3 * OUT7 * OUT6 * OUT5 * OUT4 * OUT2 * OUT1 * OUT0
+ OUT2 * OUT7 * OUT6 * OUT5 * OUT4 * OUT3 * OUT1 * OUT0
+ OUT1 * OUT7 * OUT6 * OUT5 * OUT4 * OUT3 * OUT2 * OUT0
+ OUT0 * OUT7 * OUT6 * OUT5 * OUT4 * OUT3 * OUT2 * OUT1))

FIG. 7



TIMING DIAGRAM OF TWO EVENTS

FIG. 8



PINOUT DIAGRAM