



**Fermilab**

TM-757  
0892.000

NIM POWER SUPPLY MONITOR MODULE

K. Seino

Fermi National Accelerator Laboratory

P. O. Box 500

Batavia, Illinois 60510

December, 1977

TABLE OF CONTENTS

I.	<u>INTRODUCTION</u>
II.	<u>CIRCUIT DESCRIPTION</u>
2.1	Block Diagram
2.2	Voltage Channel Input Circuit
2.3	Detection, Indication and Control
2.4	Protection Circuits
III.	<u>PERFORMANCE</u>
3.1	Temperature Behaviors
3.2	Common Mode Voltage Rejection
3.3	Transient Response
3.4	Noise Field Tests
3.5	Specifications
3.6	Accuracies when One of Six Power Supply Voltages Ceases Functioning
IV.	<u>DISCUSSIONS AND REMARKS</u>
V.	<u>ACKNOWLEDGEMENTS</u>
VI.	<u>REFERENCES</u>
<u>APPENDIX A</u>	Common Mode Voltage Compensation for Multiplexed Input Amplifiers

FIGURE CAPTIONS

Figure 1. NIM P.S. Monitor Module Block Diagram

Figure 2. NIM P.D. Monitor Module +6V Voltage Channel Input Circuit

Figure A1. Multiplexed Quasi-Differential Input Amplifier

Figure A2. Equivalent Circuit of System in Figure A1 for Common Mode Voltage Error Analysis

Figure A3. Common Mode Voltage Compensation Methods for Amplifier

Figure A4. New Multiplexed Input Amplifiers with Common Mode Voltage Compensation Circuit

DRAWING #: -0892.000-EE-46457-NIM Power Supply Monitor Unit Mother Board Schematic

DRAWING #: 0892.000-EE-46458-NIM Power Supply Monitor Unit Daughter Board Schematic

## I.

INTRODUCTION

A CAMAC power supply monitor module had been designed and constructed to monitor the output voltages of the CAMAC crate power supply unit. The module provided facilities to detect and correct failures and overloading on power supplies before significant amount of data would have been affected. <sup>1</sup>

The same desire was brought up with the NIM bin system. For the NIM bin system, a multiplexed circuit concept was proposed from the beginning in order to sacrifice a minimal number of slots for monitoring. The author encountered some difficulties which were unique to a multiplexed system. One of the difficulties was a problem with potential differences between grounds of different bins, which was a common mode voltage problem to the module. The author discusses the common mode voltage problem and its compensation method.

The system and circuits are described in Section II. The performance of the module is described in Section III. In Section IV, the author discusses why a multiplexed system was conceived and makes remarks on some difficulties of the multiplexed system. And, at the end, he does a cost comparison between a multiplexed system and a single system.

## II.

CIRCUIT DESCRIPTION2.1 Block Diagram

The block diagram of the module is shown in Figure 1. If one follows the direction of signal flows, one notices that inputs are on the left and outputs are on the right. There are six voltages channels and one return channel. Each of these voltage channels is multiplexed to accommodate eight inputs. One return channel is shared among six voltage channels. Each voltage channel consists of an input multiplexer, an amplifier and a pair of comparators. The input multiplexer selects one of eight inputs, and the amplifier properly processes the input for detection. The paired comparators have upper and lower reference levels (+600mV) to determine whether the input is in range or out of range.

On the right half of Figure 1, there are demultiplexing gates, an address counter, a timing circuit, two groups of indicators and power supplies. The demultiplexing gates along with the address counter and timing circuit properly select a bin at a time, sort out the data from the paired comparators and send them out for indication. There are two groups of indicators - one for voltages and the other for bins. The power supplies convert the voltages from the master bin to +11V and +5V to power the module.

## 2.2 Voltage Channel Input Circuit

One of the important parts of the module is the voltage channel input circuit, and it is very important to understand the principle of the circuit in order to operate the module in a proper way.

There are six different voltage channels, and there are some differences from one channel to another. However, for an illustration, +6V voltage channel is shown in Figure 2. The principle of the other channels is the same, and therefore it is not repeatedly explained here. The heart of the input circuit is the upper amplifier shown in Figure 2. The (-) input of the amplifier has two extra branches excluding the input and feedback branches. One of them is a reference branch, which offsets the +6V input so that the output is zero when the input is exactly +6.0000V. The values of the resistors around the amplifier are determined so that the output is  $\pm 600\text{mV}$  when  $\pm 1\%$  error exists on the +6V input. The other branch is for a common mode voltage compensation. This part of the input circuit is quite different from the conventional differential amplifier, which is formed with an operational amplifier and four principle resistors. Because of the commonly shared return circuit impedance, the conventional differential amplifier suffers from larger errors when potential differences exist between grounds of bins as common mode voltages. When the common mode voltage is zero, no current flows through the return circuit. Because currents from plus voltages are cancelled by currents from minus voltages.

However, when the common mode voltage is not zero, currents flow and produce voltage drops through the return circuit. In order to eliminate this phenomenon, the fourth resistor around the conventional differential amplifier was removed. By removing the fourth resistor from all the channels, the currents through the common return circuit becomes zero, and thus the undesirable voltage drops do not exist there, even when the common mode voltage is not zero.

Instead, another amplifier shown in the lower part of Figure 2 was added. This amplifier has a gain of 2, and, if a common mode voltage of  $E_{cm}$  exists in the system, it amplifies it to  $2E_{cm}$ . Then, this voltage is connected to the (-) input of the upper amplifier through a resistor that has a value close to the feedback resistor. The circuit has CMRR of 74db at DC and 66db at 60Hz. The amplifier is shared among the six voltage channels, therefore the additional circuit occupies relatively small space.

Please refer to Appendix A for a detailed description of this new common mode voltage compensation method.

When one thinks of detecting  $\pm 60\text{mV}$  error on  $+6\text{V}$ , one realizes that one needs an accuracy of around 0.01% on resistors and reference voltages. All of the resistors and the reference devices in the circuit are precision components.

### 2.3 Detection, Indication and Control

The outputs from all of the six different voltage channels are standardized.  $\pm 1\%$  errors on any of the six voltage channel inputs produce  $\pm 600\text{mV}$  at the outputs of the input amplifiers.

-7-

These outputs are compared with +600mV voltage references at the paired comparator stage. These comparators produce a TTL high or low level depending upon whether the input is in range or out of range. The TTL level signal is processed through two demultiplexers and gates. One of the demultiplexers (#74LS138), two eight position DIP switches (VOLTAGE SELECT) and six OR gates (#7432) activate or deactivate the six voltage channels for monitoring. If +6V, for example, is out of range and if its channel is activated for monitoring, a low true output from one of the OR gates triggers the monostable multivibrator for the +6V voltage indication. The other demultiplexer (#74LS138) along with a 8-input NAND gate (#7430) combines the outputs from the six OR gates above and demultiplexes them. If +12V on Bin 3, for example, is out of range, one of the outputs from the demultiplexer triggers the monostable multivibrator for the Bin 3 bin indication. For the latter example above, +12V voltage and Bin 3 bin indications are lighted.

The control circuit consists of a clock oscillator, and address counter, one-shots and gates. The clock oscillator provides 10KHz pulses for timing. A counter (#74161) and a 8-line to 3-line encoder (#74148) provide necessary addresses to CMOS multiplexers (#AD7501) and demultiplexers (#74LS138) mentioned above. In the scan mode, the counter clocked by the 10KHz pulses counts 0 through 7, and it is reset back to 0 as soon as it reaches 8, with the help of a one-shot (2.2 $\mu$ s) and gates. In the manual mode, Bins 1 through 8 are selected, and the address of a selected bin is generated by the 8-line to 3-line encoder with the help of a rotary switch.



The selected address is loaded into the counter with the 10KHz clock pulses. The duration of the measuring cycle is 100 $\mu$ s per bin. However, the first 60 $\mu$ s of the duration is the settling time for the CMOS switches and the input amplifiers, and the rest of the time is for actual detection of the signals interested. A one-shot triggered by the 10KHz pulse delays the timing by 60 $\mu$ s and then opens the gates and enables the demultiplexers.

#### 2.4 Protection Circuits

There are seven CMOS multiplexers used in the module. Six of them are used in the voltage channels, and one is used in the common return circuit. The ones in the voltage channels are protected by a high value resistor which exists between the input of the module and the multiplexer. On the inputs of +24 and +12V voltage channels, each of the input lines is clamped to either one of +5 or -5V with a diode to reduce leakage currents which flow from open switches to a closed switch. For the reason mentioned above, input lines do not have to be clamped in both directions. However, they have to be clamped in the same direction as the polarity of the input voltage.

The multiplexer in the common return circuit is protected by paired diodes and series resistors. There are two possible causes for damaging the multiplexer. One possibility is that, if one of the eight return lines is accidentally connected to either one of +24 or -24V, the multiplexer will be damaged.

## III

PERFORMANCE\*

A temperature deterioration upon the detection accuracy was observed to be less than  $0.01\%/^{\circ}\text{C}$  on the pre-prototype unit in a temperature range of  $25^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ .

When a potential difference exists between the ground of the master bin and that of the slave bin as a common mode voltage, the module rejects it. Common mode voltage rejection ratios were measured to be 74db at DC and 66db at 60Hz.

The module can detect pulses whose width is greater than  $5\mu\text{s}$  and whose height is 2% of the nominal voltage.

To investigate noise problems, the pre-prototype unit was tested at several places in the Laboratory. A maximum error of 0.003% was introduced by noises coming from the outside of the module through four of 25 foot cables.

Based upon the data taken on the pre-prototype unit, the following tentative specifications were made.

SPECIFICATIONS (TENTATIVE)INPUT CHARACTERISTICS

Input Voltages:	$\pm 24\text{V}$ , $\pm 12\text{V}$ , $\pm 6\text{V}$
Input Resistance:	400 Kilohms ( $\pm 24\text{V}$ ) 200 Kilohms ( $\pm 12\text{V}$ ) 100 Kilohms ( $\pm 6\text{V}$ )
Common Mode Rejection Ratio:	74db at DC 66db at 60Hz

MEASUREMENT CHARACTERISTICS

Measuring Speed:	100 $\mu\text{s}$ per bin 800 $\mu\text{s}$ per cycle
Alarm Trip Setting:	$\pm 1.0\%$ of input voltages

Detection Accuracy:

$\pm(1.00 \pm 0.20)\%$  of input voltages at  $25^{\circ}\text{C}$ , plus temperature coefficient of  $\pm 0.01\%$  per  $^{\circ}\text{C}$ .

#### MEASUREMENT METHODS

Bin Selection SCAN:

Module scans all of eight bins.

MANUAL:

Module monitors a bin selected.

Bin Voltage Selection:

$+6\text{V}$  can be selected for monitoring bin by bin.  $+12\text{V}$  together with  $+24\text{V}$  can be selected bin by bin.

Test:

Internal test circuit generates  $\pm 1.7\%$  error signal to test out the module.

#### ALARM OUTPUT

Open collector output handles load with voltage of  $30\text{V}$  maximum and current of  $150\text{mA}$  maximum.

Output Response:

$10\mu\text{s}$  delayed with respect to leading edge of  $\pm 2\%$  pulse change on input voltage.

\* Note:.

For further details on performances, see PREP Engineering Specification #ES-7136, "NIM Power Supply Monitor Module", December, 1977.

### 3.6 Accuracies When One of Six Power Supply Voltages Ceases Functioning

Six power supply voltages from a bin are connected to the monitor module at a time either manually or by auto-scanning. If one of these six voltages ceases functioning completely (the voltage becomes zero), it will introduce some inaccuracy on detection of other voltages. As described in Section 2.2, currents from plus voltages are cancelled by currents from minus voltages, and therefore no voltage drop is developed through the return circuit of the voltage channel input circuit. However, if, for example, +6V becomes zero, -6V voltage channel suffers from an additional inaccuracy of 0.30% because of an unbalanced current through the return circuit, which has a series resistance of about 300 ohms. The following table shows detection accuracies on the voltages of a bin where one of the six voltages is failing.

Failing Voltage						Detection Accuracy in Voltages of Failing Bin at 25°C (%)		
24	12	6	-24	-12	-6	+24	+12	+6
						1.00±0.20	1.00±0.20	1.00±0.20
X						1.00±0.28	1.00±0.35	1.00±0.50
	X					"	"	"
		X				"	"	"
			X			"	"	"
				X		"	"	"
					X	"	"	"

X: Failing (Voltage is zero).

## IV.

DISCUSSIONS AND REMARKS

One requirement was that the minimal number of slots in a NIM bin system should be used for the monitoring purpose. There are twelve slots in a NIM bin. Therefore, if a single module monitors one NIM bin, 8.3% is used for the monitoring purpose. Whereas, if a multiplexed module monitors eight NIM bins, only 1.0% is used for the purpose. In the CAMAC crate, where twenty-three stations are open for a variety of modules, the occupancy ratio is 4.3%, which is a half of the one for the NIM bin. Generally speaking, if the number is smaller than four, one should go with a single system and if the number is larger than five, one should go with a multiplexed system. Another factor is that most of key components such as multiplexers, resistor networks and diode networks come in multiple of four, i.e., 4, 8, 16, etc. Taking these factors into account and considering the amount of space in the single wid NIM module, we decided to go with eight.

If one decides to go with a multiplexed system, one has to realize that he has to tackle some difficult problems which exist in multiple systems. How much noise comes through cables? Is there any potential difference on grounds of different bins? The noise problem turned out not to be serious after testing the pre-prototype unit in several experimental areas. However, the problem of potential differences or a common mode voltage problem to the module was really serious. At the beginning of the project pursuit, a clever idea of having a common return for six different voltage channels was proposed.

This common return later turned out not to work well with the conventional compensation method for common mode voltages. It took a few weeks of concentration and thinking. In any development work, this kind of happening is not unusual. Some problem which had not been anticipated at the beginning would come along. Solving the problem is a part of the development work.

Besides the problems mentioned above, laying out pc board artwork, packaging and constructing with a multiplexed module is not easy. How difficult is the work? It is six times more difficult than the single CAMAC module, said the technician who worked on both of the modules. No one has time to compare the two cases with some numbers. However, one realizes it is much more difficult than a single module. When it comes to check-out the module, one deals with forty-eight inputs. One has to conduct tests, which are related to multiple system problems, in addition to type of tests which are normally done on a single system.

What about the construction cost? Excluding development cost, the author listed the parts and labor costs for the multiplexed NIM module along with single NIM and single CAMAC modules for a comparison.

-14-

Type of Module	Cost				Remarks
	Parts	Labor	Total	Per Bin	
Multiplexed NIM (x8)	\$840.00	\$360.00	\$1200.00	\$150.00	Including Cables
Single NIM (x1)	\$210.00	\$ 65.00	\$275.00	\$275.00	
Single CAMAC (x1)	\$200.00	\$ 50.00	\$250.00	\$250.00	

V. ACKNOWLEDGEMENT

The author would like to acknowledge the work of David Von Ohlen on the prototype construction. He did an elaborate work in making two pieces of artwork in order to accomodate so many components on pc boards. He patiently put things together for three prototype modules which had many hard wires inside. The author would like to acknowledge Ray Yarema for his continuous support and suggestions.

VI. REFERENCES

1. R. E. Shafer and R. J. Yarema, "CAMAC Power Supply Monitor Module", Fermilab TM-705-0810.00, December, 1976.
2. "Guide to Analog CMOS Switches and Multiplexers", Analog Devices Inc., Norwood, MA., September, 1975.
3. E. A. Torrero, "Focus on IC Analog Switches and Multiplexers", Electronic Design 18, September 1, 1975.



APPENDIX A

The module monitors 48 different variables - six different voltages from each of eight different NIM bins. There are six voltage channels in the module, and each of these voltage channels is multiplexed in eight folds.

Figure A1 shows a multiplexed system which has four voltage channels. This system will be used for investigating (1) a problem in a multiplexed quasi-differential input amplifiers, (2) a new method for compensating common mode voltage around an operational amplifier and (3) implementing a new multiplexed input amplifiers with a common mode voltage compensation circuit.

In the system shown in Figure A1, an input multiplexer (AD7501KN) selects one of its eight inputs at a time, and connects it to an amplifier. Whereas the return multiplexer connects the selected return line to four amplifiers. One return multiplexer is shared among four amplifiers for cost and space considerations.

If the +6V on Bin 3, for example, has a value of exactly +6.0000, the -6V reference cancels the input, and the output is 0.0000V when Bin 3 is selected. However, if there is a 1% error on the +6V input, the output becomes 600mV. The other voltage channels work in the same way as the +6V channel, and produce a standardized output of 600mV per 1% error on the input.

When there is a potential difference between the master bin and a slave bin as a common mode voltage, currents flow out of the amplifiers. These currents add up one another and create a voltage drop through the return circuit, and the voltage drop produces an error on the output of the amplifier. An Equivalent circuit for such a system can be drawn as shown in Figure A2. The amplifier on the right is for +6V and the one on the left is for +12V. The amplifier for -6V is identical to the one for +6V, and the same relation holds between +12V and -12V. For simplicity, the resistance through the return circuit,  $r$ , was multiplied by two rather than adding two more amplifiers for -6V and -12V. When the common mode voltage  $E_{cm}$  is equal to 1V, and when  $R_1=50K$ ,  $R_2=500K$ ,  $r=300$  ohms, the error on the output for +6V is estimated to be 64mV, which is more than 10% on the 600mV output. In actual measurements, a 80mV error was observed.

How can you eliminate this? The author went back to basics of the operational amplifier. In Figure A3 (a), the author reviewed the basics of the conventional differential amplifier. When a common mode voltage  $E_{cm}$  exists, the output is given by

$$e_0 = \left( \frac{R_2}{R_1 + R_2} \times \frac{R_1 + R_2}{R_1} - \frac{R_2}{R_1} \right) \times E_{cm} = 0$$

Now if the basic circuit (a) is modified to be the one in (b), what will happen? The output is expressed as follows.

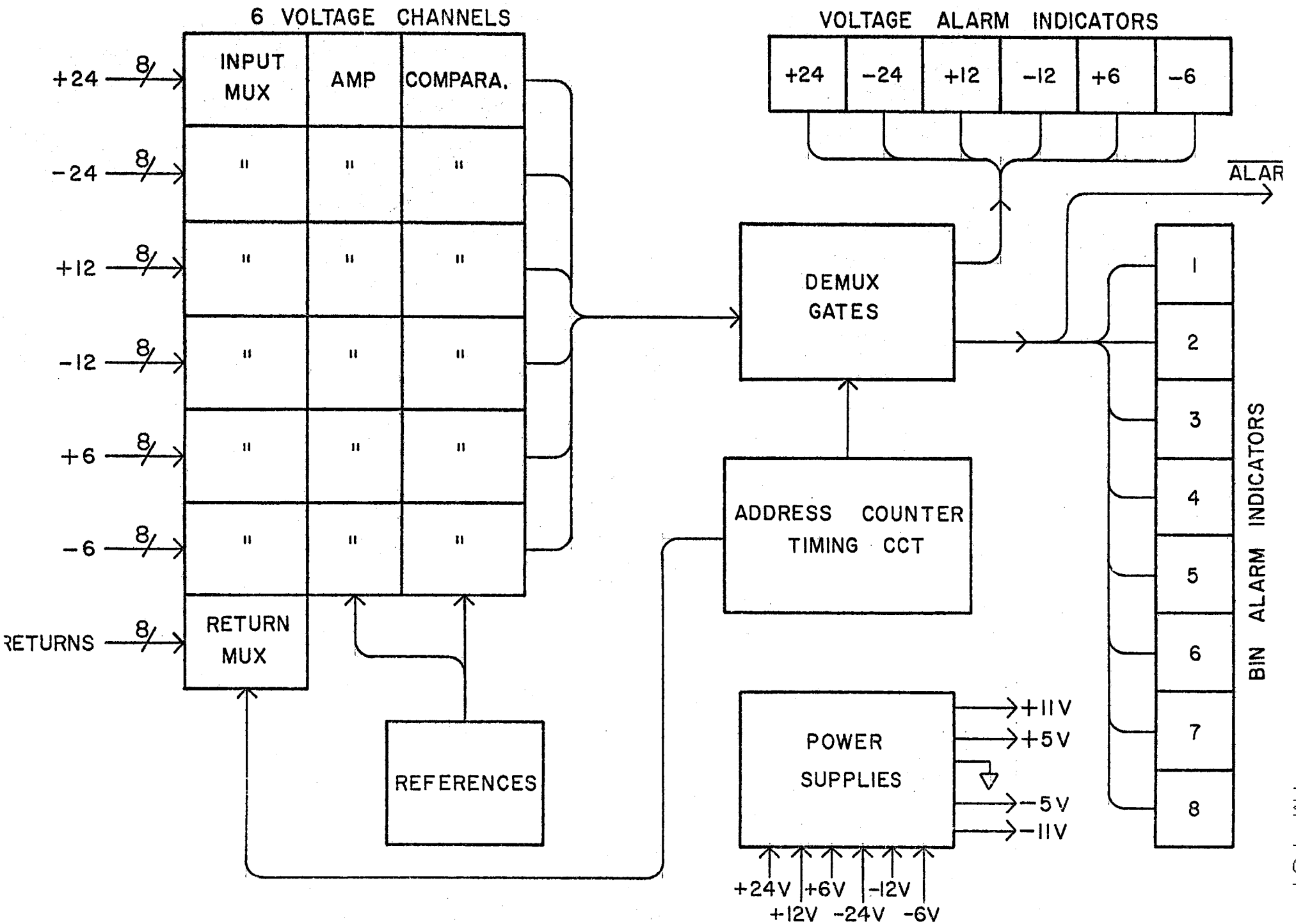
-18-

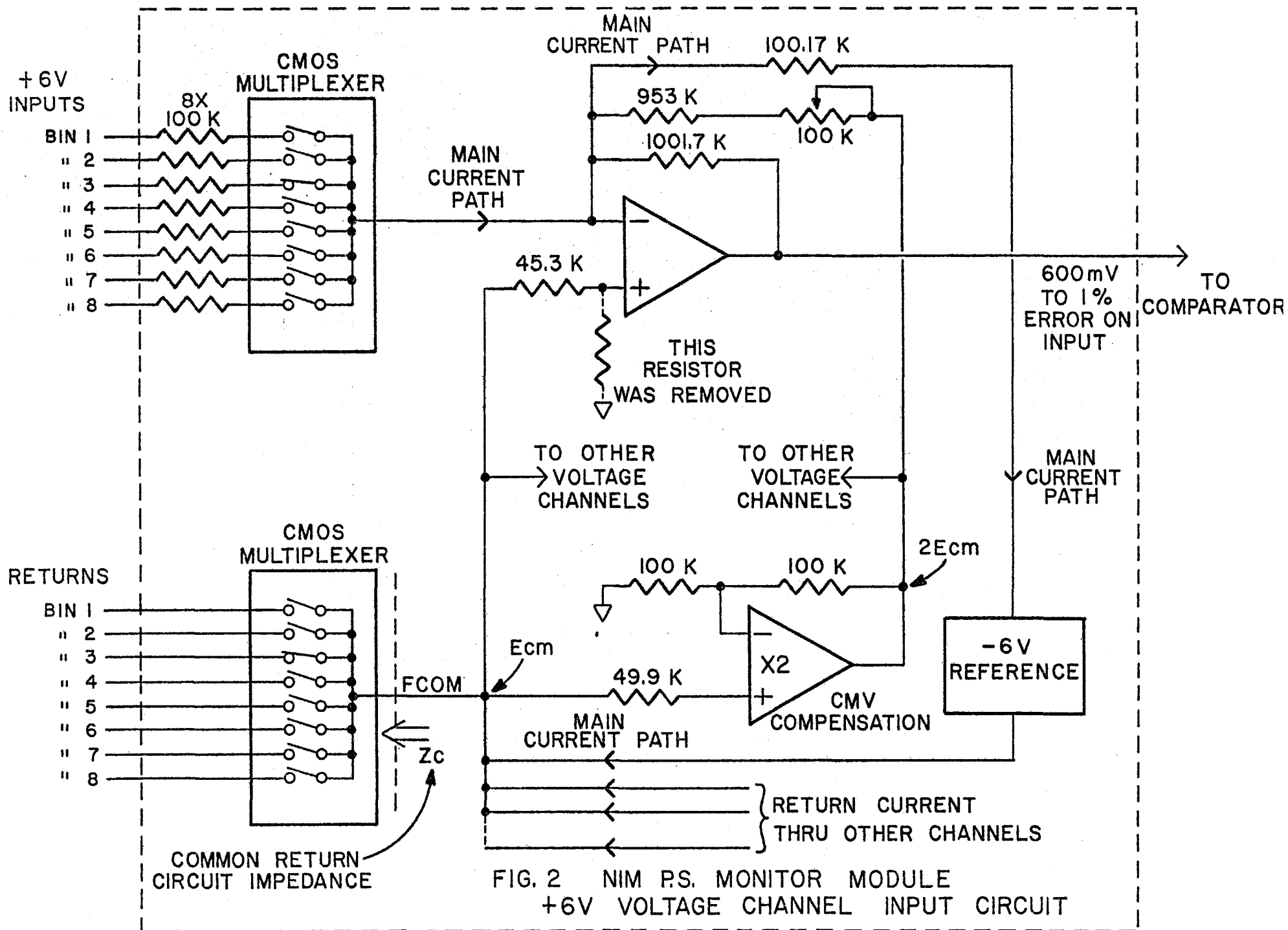
$$e_0 = E_{cm} - R_2 \times \frac{E_{cm}}{R_2} = 0$$

This shows that the common mode voltage was compensated and no error was produced at the output. Does the (b) circuit have any advantage over the (a) circuit? Yes, there is one - no appreciable current except leakage flows via the (+) input of the amplifier. This is a great advantage in the system under study. An actual implementation of the (b) circuit would be the one shown in (c). The lower amplifier in Figure A3 (c) amplifies the common mode voltage from  $E_{cm}$  to  $E_{cm}$  and feeds it through the resistor  $R_2$ .

The new system with the common mode voltage compensation is shown in Figure A4. One amplifier which has a gain of 2 is shared among four input amplifiers. The output is fed into the (-) input of each amplifier through a fixed resistor and a potentiometer combination for the best compensation. Tests on the new system revealed less than 2mV errors per 1V of the common mode voltage. The new system was more than one magnitude better than the old system which had had 80mV errors per 1V.

FIG. 1 NIM P.S. MONITOR MODULE  
BLOCK DIAGRAM





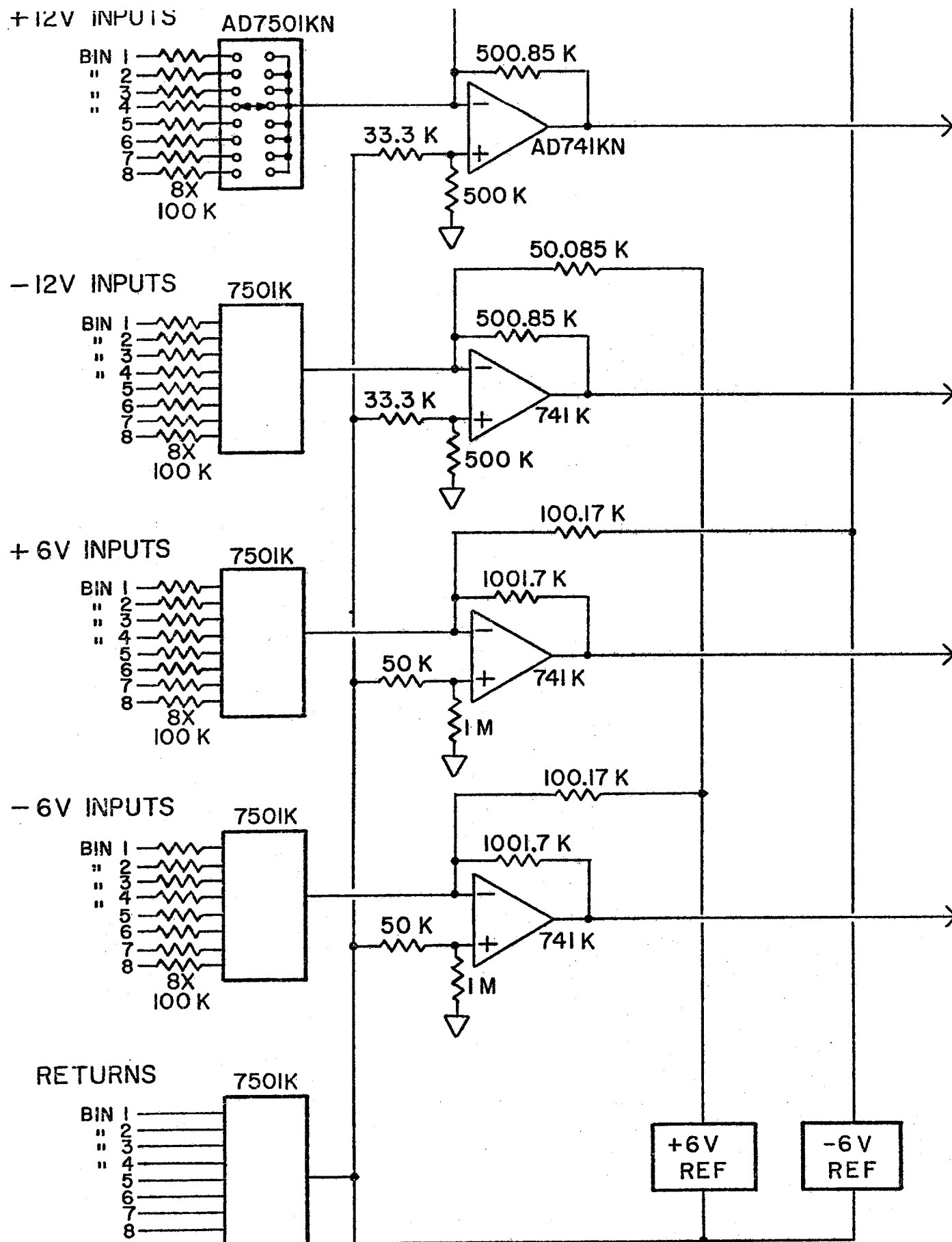
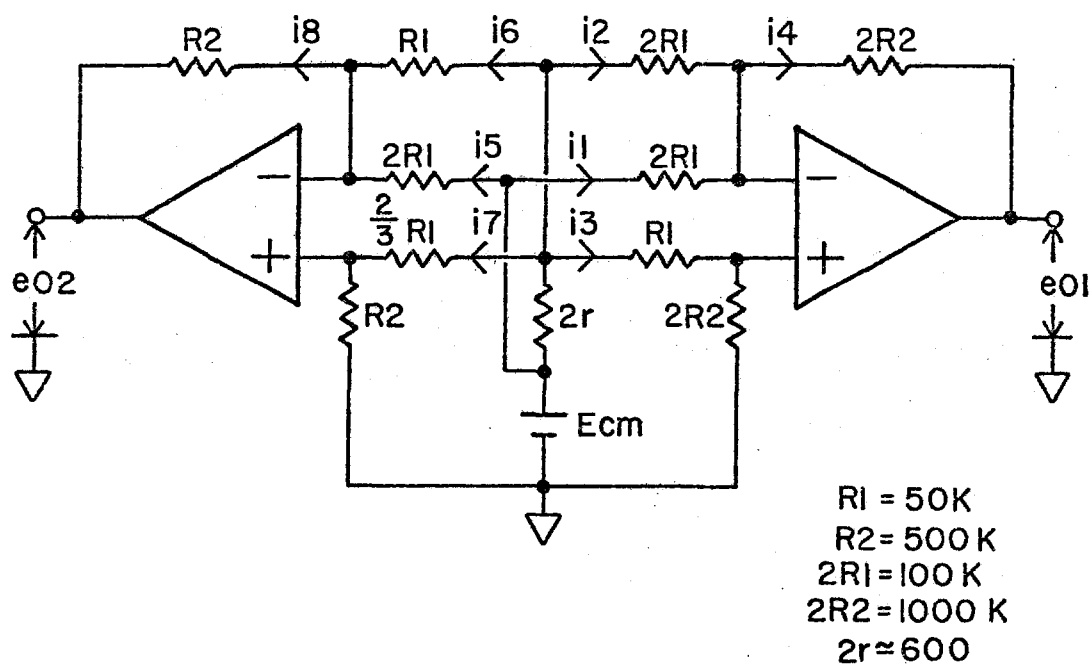


FIG. A1 MULTIPLEXED QUASI-DIFFERENTIAL INPUT AMPLIFIERS

-22-



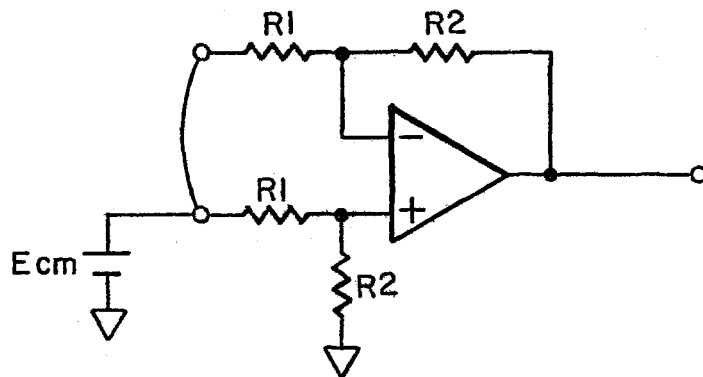
$$e_{01} = i_3 \cdot 2R_2 \left(1 + \frac{R_1}{R_2}\right) - \frac{E R_2}{R_1} - i_2 \cdot 2R_2$$

$$i_2 = \frac{E}{2(3r + R_1 + 2R_2) + \frac{10r(R_1 + 2R_2)}{R_1 + \frac{3}{2}R_2}}$$

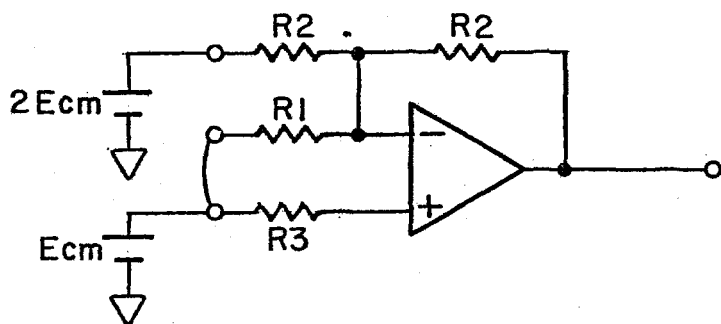
$$i_3 = 2i_2$$

FIG. A2 EQUIVALENT CIRCUIT OF SYSTEM IN FIG. A1  
FOR COMMON MODE VOLTAGE ERROR ANALYSIS

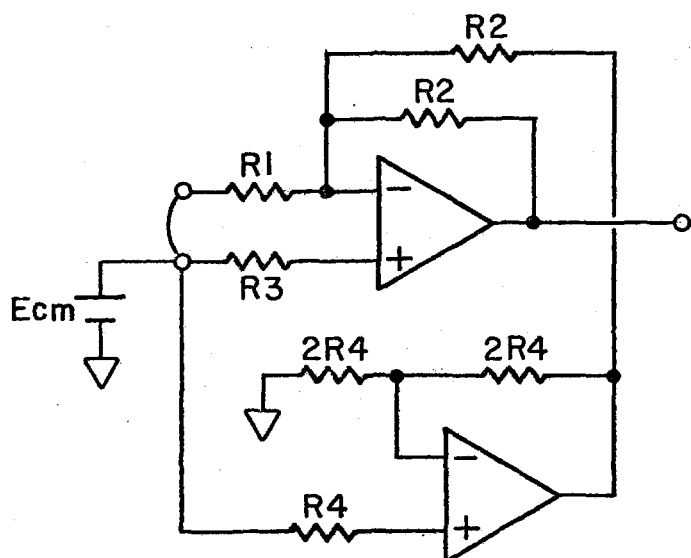
FIG.A3 COMMON MODE VOLTAGE COMPENSATION  
METHODS FOR AMPLIFIER



CONVENTIONAL  
(a) DIFFERENTIAL  
AMPLIFIER



(b) BASIC IDEA FOR  
AMPLIFIER IN (c)



(c) NEW AMPLIFIER WITH  
COMMON MODE VOLTAGE  
COMPENSATION CIRCUIT



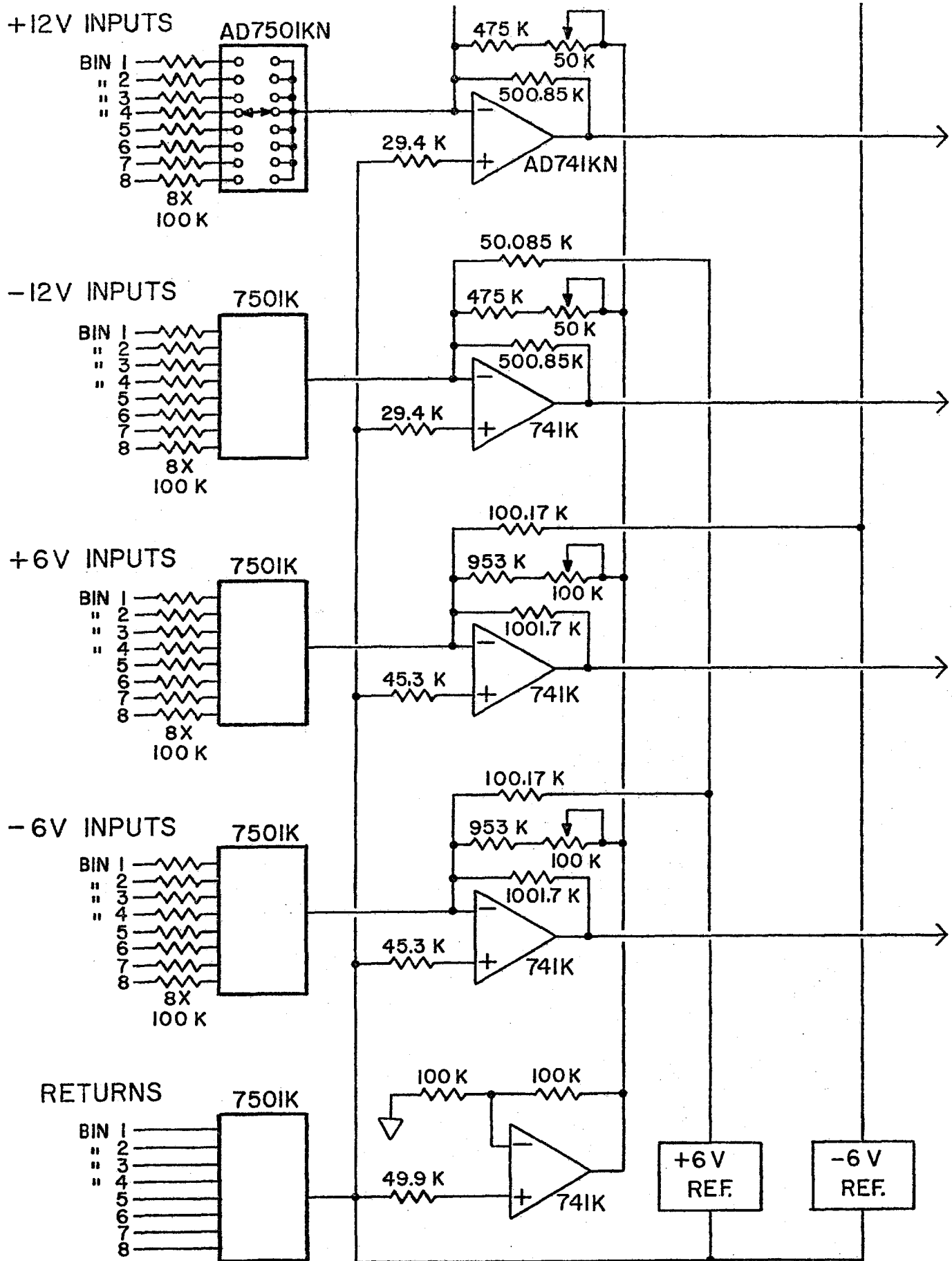


FIG. A4 NEW MULTIPLEXED INPUT AMPLIFIERS WITH  
COMMON MODE VOLTAGE COMPENSATION CIRCUIT

