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PRELIMINARY DESIGN OF A DRIFT CHAMBER TIME DIGITIZER

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INTRODUCTION

This note is being prepared to outline the system design while it is still possible to make major changes. At this time, design has progressed to the point that some data has been taken on a two channel bread board.

Several meetings, the last on February 12, 1975, were held at Fermilab with the objective of defining the parameters of a Drift Chamber Time Digitizer System. The notes of this meeting (TM-553) outline a number of systems that have been built or are in various stages of construction. A questionaire passed out at this meeting had a rather low rate of return so we did not achieve a documented concensus.

As a result of this meeting, and with the knowledge that a fairly promising commercial system (LeCroy 2770) was under development, it was decided to go ahead with the development of a Drift Chamber System within Research Services. (Memo Miguel Awschalom to R. Shafer of May 1, 1973).

DESIRED SPECIFICATIONS

The format of TM-553 lists most of the parameters desired in drift chamber electronics. A number of items are discussed in detail in TM-553 and these discussions will not be repeated here.

INPUT

Opinion seems about equally divided between NIM standard and ECL input. ECL advocates mostly propose differential twisted pair inputs while the NIM proponents are thinking of coax. The twisted pair approach is potentially less expensive due to lower cost connectors (connectors will account for approximately 10% of parts costs) and the saving of two level translators since most systems will use ECL preamplifiers. In practice, several patches may take place between the Drift Chambers and the electronics. Further, ECL levels cannot be used with standard NIM and CAMAC modules so that testing and

monitoring is more difficult with ECL levels. We rate this choice a toss up.

DIGITIZER

There are four schemes that we can identify:

1) Straight counting of a fast clock.
2) Time stretching and counting of a slow clock.
3) Combination of 1) with the storage in a fast register of the phase of the clock, extending effective clock rate by one or two bits.
4) Combination of 1) with time stretching to resolve time between major clock pulses.

The first is by far the easiest scheme. Unfortunately, the present plans for drift chambers at Fermilab seem to require the ultimate in drift chamber resolution which means time resolution of 2-4ns or 250MHz to 500MHz clocks. This requires high power and high cost components. We know of no proponents to use direct counting above 100MHz in spite of the availability of ECL scalers to above 1GHz.

The second is the most used system to date. Early experiments with Drift Chambers used commercial TDC's, most of which have resolutions to 100ps and are more than adequate in resolution if not in cost per channel or conversion time. Conversion time is not a big problem if abort time is small. Thus, the LeCroy scheme of resetting the time stretcher with each incomming pulse produces an acceptable scheme even though the conversion time is 15us since the conversion time overlaps the computer interrupt time which is hard to keep below that level. This scheme also requires the least power, LeCroy advertising less than 0.2W per wire. (We would like to know how he does it.)

Stretcher schemes are analog and can suffer from a variety of problems so that it is necessary to make careful measurements of the design. Many designs have been completed to an order of magnitude greater accuracy than required by drift chambers so this is not a major problem but it is one that cannot be ignored. One likely problem, integral linarity, is of no particular significance since the drift time is not linear and two corrections are as easy to make as one. A second potential problem, especially with the LeCroy fast reset scheme, is the stretcher capacitor "memory" (dielectric adsorption) of previous events. It will be necessary to look carefully for this effect in any stretcher design.

The third scheme is under development by groups at CERN and Columbia. These implementations tend to require high power and parts cost. There may be some problems in trimming the delay line latches so that the read out is not ambiguous.

The power used by these schemes is formidable. The Sippach (Columbia) scheme is reported to require 5W per wire with 8 wires in a single width CAMAC module - or 200 amps per CAMAC crate. The Verweig (CERN) scheme uses somewhat less power per wire (3W) and half the wires per module but will still require special crates and cooling.

In spite of the required power, the Sippach solution is an elegant one if the multiple track requirement is real. More on this later.

The fourth scheme is represented by the UCSD (W. Vernon) design in TM-553 and by our design. By combining a few bits of stretcher with a slow clock it is possible to operate almost all the logic at slow (low power Schottky) rates while maintaining good time resolution. Since analog techniques are used for only a few bits (4 in our case) accuracy requirements are not high and circuits can be designed (we hope) without trimming provisions for each channel. Again, since the accuracy required of the capacitor memory is low, dielectric adsorption problems should be reduced making the desirable fast abort scheme easier to implement.

TRIGGER

We consider common stop triggering to be highly desirable. In the most attractive schemes, each incomming pulse resets the clock and starts the timing operation. At some later time the decision is made to accept the event, further inputs are blocked and all times are stored.

With common stop triggering the decision logic time required to determine a possible event overlaps the drift time of the event. In general, this will require only one short delay cable per system to match the expected maximum drift time plus propagation time to the electronics to the event decision time.

Common start triggering requires a delay cable equal to the event decision time in every signal cable.

Common stop triggering is easy to implement with an all digital

scheme, with analog time stretchers it is necessary to check that the storage capacitor does not remember an earlier charge.

TIME RESOLUTION

Time resolutions of known systems range from 0.5ns to 10ns. In TM-553 we conclude that 4ns is adequate to match the potential accuracy of the drift chamber process. An extra improvement of $\sqrt{2}$ is possible if the stop time is measured to high accuracy. (In practice 1 or 2 additional bits in enough.) We are designing for 3ns resolution since this is within the capability of our X16 stretch and low power Schottky scalers.

DOUBLE TRACK RESOLUTION

A number of systems are being designed for multiple hits on a single wire. This is because it is desirable experimentally to resolve two closely spaced tracks. The Sippach design is particularly elegant in the electronic solution of the multi track problem.

From our observation we have concluded that multiple track detection will not be particularly successful, even though multi track resolutions of 2 to 3mm have been reported in the literature.

In drift chamber operation, a particle track leaves behind a number of isolated electrons which drift to the sense wire in slightly different times where the multiplication process results in a burst of charge for each electron arrival. With two tracks it is necessary to make the chambers very thin if all the electrons from the first track are to arrive before those from the second track since those near the chamber faces must travel slightly farther to the sense wire. This reduces the efficiency so it is now necessary to increase the amplifier gain, possibly even to the point of detection of single electron arrivals. If the signal is now differentiated to resolve two tracks it is likely to also resolve single electron arrivals.

Further, the multiplication process tends to produce after pulses which can arrive some time after the initial pulse.

Thus, while it is possible to electronically detect multiple tracks, we believe it will be most difficult for track spacings below 5mm (100ns) since the electronics is likely to record mostly junk, i.e., the arrival times of individual electrons, if high gain differentiating amplifiers are used.

Since it is necessary to use two staggered chambers to resolve the left-right ambiguity, this configuation also allows resolution of two tracks per drift cell. This is the configuration we support and are designing single track per wire electronics.

RUNDOWN TIME

For present applications, rundown time is not particularly important, provided it is kept below computer interrupt time (which can be as much as 250us). We are anticipating event selection by fast digital pre-processors. In this case, fast analysis of events by digital pre-processors which might operate at 100ns cycle times and which might make an accept or reject decision in 100-200 instruction times could greatly increase the fraction of good events recorded on tape and thus the effective event rate since most experiments will be tape limited for the near future.

The rundown time of 1us for our system would allow such pre-processing.

ABORT TIME

As mentioned earlier, common stop systems require fast abort times. They should not be too fast, however, otherwise the system will be more likely to measure after pulses than the primary track. This system is thus being designed with a 100ns dead time for multiple inputs on the same wire. With simple circuits this allows stretching the input pulse to 50ns which is enough time to discharge the storage capacitor.

Since events must be spaced by at least the maximum drift time this will not result in loss of data for drift spaces of 1/2cm or more.

SYSTEM OBJECTIVES

Much of our design has been "given away" in the previous discussion comparing our system with the design points in TM-553. We give special emphasis here to our primary design goal:

1) To design a drift chamber system which could be distributed through PREP to provide a cost effective solution to most drift chamber applications.

PREP is called upon to supply a variety of configurations.

Maintenance of special crates, special cables etc., is a major problem. For this reason packaging in other than NIM or CAMAC was discarded. Packaging in NIM with CAMAC read out was given serious consideration. CAMAC packaging was adopted since it would reduce the required number of module types to 2, would require no special cables, would enable early test runs to be quickly implemented (with as few as 2 CAMAC modules) and would still appear to be competitive in cost.

This decision prompted a number of secondary design goals:

1) To operate within standard CAMAC crate power.
2) In anticipation of future pre-processing, the system should have minimum rundown time.
3) The system should operate with common stop triggering.
4) The read out system should read only the non-zero channels to minimize read out time.
5) Construction cost should be 50% or less of the advertised LeCroy price of $50.00/channel.
6) The system should be designed to allow access by a processor module other than the crate controller.
7) No special crate wiring.
8) All CAMAC rules are to be obeyed (well almost).
9) Time resolution to be 4ns or better.
10) Systems should be available to Fermilab experimenters ahead of LeCroy commercial units.

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