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HIGH-SPEED BEAM POSITION ELECTRONICS FOR ACCELERATOR CONTROL AND DIAGNOSTICS

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GENERAL

Fast beam position electronic processing devices have become an integral part of the on-line and diagnostic components of the Fermilab accelerator. These devices process signals derived from a variety of differential pick-up electrode assemblies mounted internal to the beam vacuum chamber. In some instances the position detectors are only a few feet away from the point where beam signal samples are available while in others coaxial cable runs of about 1000 feet may be required to transfer the beam pulse data to the detection equpment. The relatively large losses associated with long cables and signal intensity variations greater than 5 orders of magnitude create a requirement for electronic devices with good signal-to-noise discrimination, high sensitivity, and large dynamic range. Such position detectors have uses related to the con trol of the beam in active closed-loop feedback systems and in diagnostic control schemes in which position data are observed and machine parameters adjusted accordingly. In the Fermilab accelerator, several feedback loops with complex interrelated feedback paths use, as their primary source of data, the beam position information derived by the systems described herein. Among these are: (1) the main accelerator synchronous phase angle control loop, (2) the horizontal and vertical main accelerator beam damping system, and (3) the injection tuning monitor loop.

The guidelines for a position system to serve these needs as well as those of a diagnostic nature are that the system have 50 dB minimum dynamic range, ± 1 mm resolution, 5 MHz minimum bandwidth operability in a variety of modes such as sample and hold, CW, triggered etc., and an output which is normalized relative to intensity. To accommodate these requirements together with others such as adjustable scale factors, specialized filtering, data holding ease, packaging standardization, etc., two types of position systems have been developed.

In one type of system, the amplitude difference information obtained from the pick-up electrodes is converted to phase difference information at the beam signals fundamental frequency by a grouping of interconnected quadrature hybrid junctions and RF transformers. These components are configured as an RF amplitude-to-phase converter. Post converter signal processing is accomplished by a dual channel RF limiter/cosine processor/wide bandwidth pulse amplifier chain. The resultant output is proportional only to beam position, independent of intensity due to the processing of angle information which uniquely contains the ratio of the input signals.

In the other beam position system an amplitude SUM and DIFFERENCE processor develops the position signal by forming signals proportional to the sums and differences of the pick-up electrode potentials. A passive hybrid junction operating at the beam signals fundamental Fourier frequency (close to 53 MHz) functions as a signal level comparator and performs the summing and differencing operations. Post comparator processing in this system includes a fast AGC system to permit normalization of the data and cosine phase detector which provides the required difference-to-sum signal $\left(\frac{d}{\Sigma}\right)$ ratio with its correct sign. This ratio, after scale factor adjustment is the measure of beam position, independent of intensity variations. An important feature of the devices to be discussed is that they do not depend on repetitive beam signals for their operation. A single pass of a series of sixty beam bunches spaced approximately 20 ns is sufficient to activate the position detector circuits. In some cases position data developed in 1.6 μsec is held for as long as 10 seconds. The devices therefore become useful for both analysis of repetitive (or circulating beams) and single beam passage (as in beam injection, transfer, or extraction) investigations. This paper will give a capsule description of each type of position device together with their relevant parameters.

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PHASE PROCESSING POSITION SYSTEM

The phase processing position detector is shown in Figure 1. The detector consists of four major circuits as follows: (1) the Amplitude-to-Phase Converter, (2) Limiter Phase Detector, (3) Logic Generator/Track and Hold, and (4) Output and Scale Factor Circuit. The voltages developed by beam passing through the electrode assembly is transmitted to the Quad Hybrid/Transformer grouping by way of impedance matching devices (⊠) and by splitters (A and B). The splitters and transformers provide the Quadrature Hybrids with three in-phase and one anti-phase beam signal. Since each Quadrature Hybrid output port (ports 2 and 3, Figure 1) contains the sum of an in-phase and quadrature-phase component of the input voltage, the phasors at ports 2 and 3 exhibit amplitude and phase variations as $\left(\frac{V_b}{V_a}\right)$ changes above and below 1. The angular difference in these phasors ($\Delta\Psi$), can be shown to be simply related to the ratio of the input signals $\left(\frac{V_b}{V_a}\right)$. For the case where the input signal phases are matched, the phase angle is:

$$(\Delta\Psi) = \tan^{-1}\left(\frac{V_b}{V_a}\right) - \tan^{-1}\left(\frac{V_b}{V_a}\right) \text{ rad.} \quad (1.$$

By determining ($\Delta\Psi$), the ratio of the inputs and thus the position of the beam is determined. The angle information developed by the amplitude ratio-to-phase conversion process indicated by equation (1. and contained in signals V_a and V_b, is transmitted to the limiters and phase detector circuits for removal of amplitude variations and demodulation. The limiters shown in Figure 1, are designed to limit from thermal noise levels to signals of about 1.5 V P-P input level. The primary purpose in limiting prior to the demodulation by a phase sensitive detector is to prevent amplitude cross product terms from appearing at the demodulators output, i.e., the phase detector is sensitive to the amplitudes of the inputs as well as the phase angle between the input signals. Since the slope of equation (1., the AM-to-PM conversion sensitivity, is relatively small, 6.5 electrical degrees/12% change in the $\left(\frac{V_b}{V_a}\right)$ ratio the limiters must be of the "constant phase" type and exhibit an extremely stable phase versus signal-level characteristic. The limiter pairs used for the phase processor circuitry have a dynamic operating range of 70 dB, over which phase tracking is maintained to within 3 electrical degrees throughout the frequency range, 48-to-58 MHz. Note that when $\left(\frac{V_b}{V_a}\right) = 1$ in

equation (1., $(\Delta\Psi) = \frac{\Pi}{2}$ rad. This is the desired result since the cosine-law phase detector produces a zero output when the beam is aligned to the axis of the aperture. The correct sign of the displacment is contained in the phase detectors output since the developed phase difference angle ($\Delta\Psi$) operates in either the 1st or 2nd quadrant. The polarity of the detectors output, being related to Cos ($\Delta\Psi$), will reflect the necessary in-out, up-down, relationship of the beam relative to the on-axis condition.

The matched bandpass filters shown in the LIMITER PHASE DETECTOR circuit aid in recovering the beam fundamental component (53 MHz) and reducing spurious harmonic frequencies from the output of the limiters. The filters have full bandwidths of 20 MHz and skirt selectivity approaching 36 dB/decade.

The phase detectors output signal is transmitted to the LOGIC GENERATION TRACK and HOLD circuit which controls the flow of position data to amplifier circuits which are designed to supply load currents of as much as 120 ma and scale the amplitudes to useful values.

The track and hold circuits are activated by a signal limiter which converts the SUM signal, developed by the third quadrature hybrid (Σ), of the converter circuitry, to TTL level logic. The logic circuit has a dynamic range of 60 dB min and consists of six "long-tail pair" limiter stages and associated detectors and broadband pulse amplifiers. The risetime of the TTL output is 4 ns. The logic circuit is configured as an updating amplitude discriminator so as to allow gaps of several beam bunches to control tracking and holding functions. Discrimination against missing bunches and large bunch amplitude variations is achieved by circuits in the TTL LOGIC block; this measure reduces false triggering or multiple triggers.

Two signal output channels are provided by the Output and Scale Factor circuitry. One circuit contains a dc-5 MHz bandwidth power amplifier with adjustable gain (2-6), for driving 50 Ω loads to ± 6 V peak. This channel designated FAST OUTPUT has a sensitivity range of 1-3 V/cm when the detector is connected to either split-plate differential electrodes, or stripline electrodes. The FAST OUTPUT path provides position data for beam damping devices and diagnostic monitors. The FILTERED OUTPUT channel derives its signal from the held samples of the batch data appearing at the output of the TRACK & HOLD circuit. The tracking and holding process is utilized in place of passive or operational integrators to permit control loop circuits, which use the slow channel data, to have larger gain and phase margins as well as allowing improvement of amplitude stability under conditions where only part of the ring is filled with protons. Gain adjustments of the NARROW BAND AMP permit an output sensitivity range of from 1-to-3 V/cm when either split-plate differential or stripline electrodes are used. The maximum output is 6 V/50 Ω and typical bandwidths set between 1 and 10 kHz by (R, C) Figure 1. The overall properties of the phase processor are summarized below:

PHASE PROCESSOR CHARACTERISTICS

Operational Modes: RF, CW, Pulse; no switching
Position Range: ± 2 cm min; depends on electrodes used
Resolution: < 0.5 mm
Operating Frequency: -40-65 MHz
RF Input Z: 50 Ω Nominal
Input Phase Matching: ± 20°; not critical
Max RF Input: 2V P-P Nominal
Dynamic Range: > 60 dB; normalized
Fast Output: 1-to-3 V/cm, adjustable/50 Ω
Fast Output Bandwidth: 5 MHz min; RT < 50 ns
Filtered Output: 1-to-3 V/cm, adjustable/50 Ω
Filtered Output Bandwidth: 10 KC typical
Linearity: < 5% B.S.L. to $\left(\frac{V_b}{V_a}\right)$ ± 30%
Packaging: NIM Module; 4 wide

Circuit Description SUM and DIFFERENCE System

Figure 2 contains the block diagram of the SUM and DIFFERENCE processor. There are 5 major functional areas represented: (1) Input Signal Processing, (2) Hybrid Signal Comparator, (3) AGC and Logic channel, (4) SUM and DIFFERENCE channel, and (5) Output and Scale Factor amplifier section.

The beam pick-up signals are coupled to the hybrid comparator by coaxial cables. When split-plate differential electrodes are used source impedance matching devices may be required. These devices (⊠), Figure 2, are designed to transform the reactive component of the pick-up plates (≈ 0-j50 Ω) to a real impedance (50+j0Ω) so as to reduce the effects of standing waves on the cables and eliminate "echos". For stripline electrodes, broadband real impedances are inherent in the design and the matching devices are not necessary. The SIGNAL INPUT PROCESSING block of the SUM and DIFFERENCE also contains a set of gain and phase matched filters to aid in selecting the fundamental Fourier component of the beam. These filters are tuned to 53 MHz, have a -3 dB bandwidth of 9.5 MHz, nominal impedance of 50 Ω and are constructed of "constant impedance" bridge "T"-type sections.

If the ratio of the input quantities, Figure 2, is formed, i.e., $\left(\frac{V_a - V_b}{V_a + V_b}\right)$ the dependency upon the intensity factor is cancelled leaving the displacement (S), a function only of a proportionality constant and the ratio, thus:

$$S = K \left(\frac{V_a - V_b}{V_a + V_b}\right) = K \left(\frac{d}{\Sigma}\right) \text{ Length Measure} \quad (2.$$

The actual beam displacement then is uniquely contained in the difference-to-sum ratio. Formation of the ratio to secure independence from beam intensity variations is the function of the AGC and Logic Channel and the Sum and Difference channel of Figure 2. A fast division process of the RF sum and difference signals is carried out in these channels in a two-step process. The magnitude of the quotient (S), is developed first, followed by affixing the correct sign to the result.

In Figure 2, note that the same Automatic Gain Control (AGC) voltage is applied to both the sum (Σ) and difference (d) channels; hence the gains G_1, G_2, are made to track each other. The circuits of the blocks shown in the AGC and LOGIC area of Figure 2, forces the AGC voltage to become whatever value is necessary (within the dynamic range bounds) to establish a constant RF output voltage (E_Σ) at the sum channel output port. For these conditions, and referring to Figure 2:

$$G_1 = G_2, \text{ because of gain tracking through AGC action;} \quad (3.$$

$$\text{thus, } \Sigma G_2 = E_\Sigma = K_1, \text{ constant due to AGC action;} \quad (4.$$

$$\text{and, } d\ G_2 = E_d, \quad (5.$$

$$\text{and, } E_d = K \left(\frac{d}{\Sigma}\right) \text{ Volts.} \quad (6.$$

Equation (6. is an important relation, it shows that the division process can be carried out through a dual channel gain-slaved amplifier chain in which an AGC system acts to keep a reference voltage (sum signal) constant. Equation (6. points out that the difference

channel's output voltage E_d, contains the required measure of off-axis position (S), since it is directly proportional to the $\left(\frac{d}{\Sigma}\right)$, ratio. Note that processing the difference output signal by an amplitude detector alone would not result in the necessary position data because directional, in-out, up-down, information is missing. However, the proper sign is applied to the difference signal by transmitting of the sum and difference signals to a phase sensitive demodulator (Figure 2) having a transfer function of the form:

$$E_{det} = G\, E_d \cos\left(\theta_{E_\Sigma} - \theta_{E_d}\right) \text{ Volts} \qquad (6.$$

where G = constant, a gain parameter.

The circuit shown in Figure 2 makes E_{det} dependent only on the difference voltage and the cosine of the phase difference angle. Since the hybrid comparator produces a difference signal ($V_a - V_b$) which is in phase with/or 180° out of phase with the sum ($V_a + V_b$) depending on whether the beam is on one side or the other of the beam axis, the Cos $\left(\theta_{E_\Sigma} - \theta_{E_d}\right)$ term of (6. is positive or negative and thus the correct sign and amplitude of the displacement is contained in the demodulators output.

The Figure 2 signals EHV SLOW, EHV HELD, and EHV FAST, as obtained by amplification and/or holding the amplified values of the detectors output E_{DET} are the devices outputs. The sensitivity factors for each of these outputs are listed in the SUM and DIFFERENCE parameters below.

A series of beam bunches lasting < 1 μsec, is sufficient to actuate the TRACK and HOLD circuits. The position information obtained on a single passage of the beam can be retained with little droop for 10 sec.

The voltage proportional to the sum signal is derived from the amplitude of the AGC voltage. The AGC voltage is developed by a gain ramping circuit which is activated by a start trigger, Figure 2, top, obtained by detecting the spaces between batches (≥ 60 nsec.) and converting the spaces to a TTL logic level trigger. As the ramp proceeds, the gain is driven upward until a threshold is reached whereupon a command STOP is developed. Stopping the ramp holds the gain constant until the next cycle, approximately 82 bunches later, where the process repeats. The time of arrival at the fixed threshold is dependent on the size of the RF signal and thus the ramp voltage level acquired at the STOP command is a measure of the intensity. The intensity signal, E_{SUM}, is obtained by sampling and is linearized in terms of dB, the value is:

$$E_{SUM} = (7 - 0.14\ dB)\ \text{Volts} \qquad (7.$$

where dB = number of decibels the input is below 1V P-P.

To account for the fact that the gain of the RF amplifiers continues to increase for several nanoseconds following the generation of a STOP command, delay correction circuits are used in the AGC and LOGIC control processes. The delays cause the RF gain to be larger than is actually required for perfect normalization. A corrective circuit, Delay Offset and the Sample Gate, Figure 2, combine to: (1) depress the AGC voltage level following a stop command by an amount to account for the delay in stopping the ramping action, and (2) to allow the RF signals E_Σ and E_d to be transmitted only after the correct gain level has been reached. The delay correction circuits permit normalization over a 45 dB range with less than ± 2 dB error.

Several operational modes have been designed into the position system to accommodate various usages.

The mode of operation either CW, triggered, or internal logic is selectable from a front panel switch. In the CW mode, the device accommodates continuous wave signals, with an internal clock providing samples every 1.2 μsec. For the triggered mode, an external TTL trigger starts the gain ramp and samples are taken each time a trigger is applied. Maximum trigger rate is 1 MHz. For the internal logic mode, triggers are developed automatically about every 82 beam bunches.

The overall parameters of the SUM and DIFFERENCE system are listed below.

SUM AND DIFFERENCE POSITION SYSTEM PARAMETERS

General

Operational Modes; Switch Selectable: CW
Internal Logic, Triggered
Displacement Range: ± 2 cm Min.
Operating Frequency: 45-58 MHz.
Resolution: < 0.5 mm.
Maximum RF Input: 1 V P-P
Dynamic Range: 50 dB Normalized
Input Impedance: 50 Ω Nominal
Phase Matching of RF Inputs: ± 3°

Normalized Difference Outputs

E_H, V HELD (Sensitivity): 1-2.5 V/cm/1000 Ω
E_H, V HOLD TIME: 10 Sec Max.
E_H, V HELD DROOP: 30 mV Max.
E_H, V FAST (Sensitivity): 1-3 V/cm/50 Ω
E_H, V FAST BANDWIDTH: 4.5 KC, @ -3 dB
E_H, V SLOW (Sensitivity): 1-3 V/cm/1000 Ω
E_H, V SLOW BANDWIDTH: 10 KC, @ -3 dB
SUM OUTPUT VOLTAGE: E_{SUM} = (7-0.14 dB) Volts
SUM HOLD TIME: 10 Sec Max.
E_{SUM} DROOP: 20 MV Max.

Dynamic Performance

Trigger Rate: 1 MHz Max.
AGC Slewing Rate: 70 dB/μsec.
Fast Output Rise Time: < 80 nsec.
Packaging: NIM Std, 4-Wide Module

SYSTEM TRADEOFFS

The choice of which type of position detector is used depends on a number of factors and on the specific application. For applications requiring the largest dynamic range, fastest normalization performance, and the minimum amount of attention to phase equalization of the input signals the phase processor has the advantage. However, in applications where a microsecond is available for signal processing and where dynamic range is restricted to say 50 dB, the amplitude SUM and DIFFERENCE system has advantages, particularly in terms of control and sampling, derivation of an intensity related signal, and from the standpoint of thermal noise (KTBF) minimization. Careful phase equalization of the input signals are required, however. The circuit arrangements of both position detectors allow data acquisition on single passage of beam. In those applications where the properties of injection, beam transfer, and extraction are to be studied the described devices become very useful aids. Other system factors also guide in the tradeoff analysis, among these the most significant are frequency range, allowable normalization error, minimum/maximum available signal levels, impedance matching to the electrode assembly, and system interface requirements such as loading, power availability, and packaging considerations.

The two devices described have been developed to fulfill almost all of the operational and diagnostic

needs of a large accelerator where fast data processing is mandatory. The design concepts outlined for the phase and amplitude processors also permit expansion in capability to other frequencies, bandwidths, and ranges and data holding options with state-of-the-art components.

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FIGURE-1
PHASE PROCESSOR POSITION SYSTEM

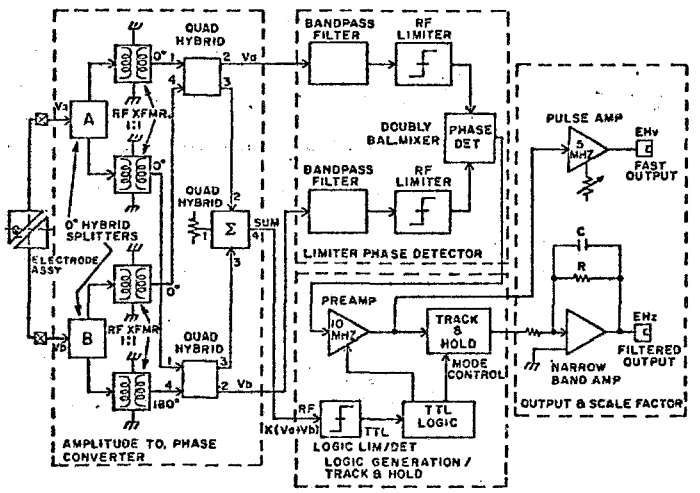

FIGURE-2
SUM AND DIFFERENCE POSITION SYSTEM