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A SYNCHRONIZATION METHOD FOR HIGH-SPEED START-STOP SCALERS AND DIGITAL DEVICES HAVING ASYNCHRONOUS TRIGGERS

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SUMMARY

A synchronization method and an associated circuit which is applicable to start-stop digital circuits particularly high-speed scalers/counters and devices requiring the application of control pulses for presetting, loading, clearing, etc., is discussed. The method developed for synchronization is especially useful when the control pulse must be timed to a particular region within a cycle of the input clocking waveform even though the synchronism between the start trigger and clocking signal is arbitrary. The technique used to generate the timed control pulse is through frequency multiplication with subsequent gated division of the clock signal, together with manipulation of the start triggering process by standard integrated circuit logic gates, flip-flops, and delays.

When the control pulse is applied to scalers requiring the use of preset control pulses to initiate the counting process in a sequential manner, errors associated with the start-up counting processes are eliminated, while jitter in terminal count data relative to the start triggering markedly reduced. A random triggered, recycling, predetermined start-stop scaler optimized for the 40-60 MHz range and using the outlined triggering method is discribed. The scaler has a range from 2-to-9999 counts, sensitivity of 40 mV rms and provides both NIM and TTL standard logic outputs.

The scaler is composed mainly of standard ECL integrated circuits including universal counters, configured in a "synchronous parallel carry" connection, and ordinary logic gates and flip-flops. Following a start trigger, the scaler is designed to cycle until disabled, delivering an output pulse each time the predetermined count is reached. The time jitter of the output pulses with respect to the periodic input signal is less than 0.1 ns.

High resolution examination of the behavior of individual charge bunches within the Fermilab Main Synchrotron is made possible when the scaler is set to count the machine's harmonic number. If the scaler is set one digit away from the harmonic number, the output pulses advance one bunch for each turn around the machine, allowing a sequential display of the contents of each bucket in the machine.

INTRODUCTION

Oftentimes there is a requirement to develop control pulses for application to start-stop digital circuits. These control pulses may be utilized as presets, resets, enables, clears, etc., for on-line or diagnostic digital devices The control pulses are required to be applied to control terminals of these devices at a particular time during a clock cycle for proper circuit operation. The dynamic timing properties[1] (set-up time, (T_{SU}), hold time (T_H), and transition time (T_T) of specific circuits pinpoint the exact nature of the timing requirements, but in general, the timespan between the set-up and hold-time boundaries must be bridged by the applied control pulse. When the digital circuit is to be triggered in a start-stop sequence, wherein the start-stop triggers are synchronous with the transitions of the clocking signal, the circuits timing dynamics can be established in a straightforward way. One simple way is to utilize fixed delays in the triggering and/or clock lines to force the trigger initiated control pulses to bridge the required clock transition for each cycle of start-stop operation.

For the asynchronous situation the relative timing between the start triggers and clocking transitions is a random variable, and therefore to force the position of the applied control pulses to always bridge the correct region adaptive processing of both clock and trigger signals is necessary. Of particular interest in this writing is the development of an adaptive synchronization method to permit error-free[2] control of a class[3] of "universal counter" integrated circuits which constitute the primary building blocks of high-speed start-stop scalers.

This memorandum will discuss the relevant aspects of synchronous and asynchronous triggering of these digital devices first, to establish the parameters of interest, and secondly a discussion of a particular method to synchronize the starting and stopping processes will be given together with a block diagram description of a typical scaler used for synchrotron control and diagnostics.

SYNCHRONOUS TRIGGERING

An example of the synchronous triggering is shown in Figure 1. The top sequence in the figure shows the counter start-up timing diagrams where a start trigger is applied during the positive transition of the clock; the trigger being synchronous with the clock. The preset control pulse, a required function to standardize loading conditions upon a "start count" command, is positioned about the set-up and hold boundaries by simple delaying the clock signal by the set-up time, (T_{SU}) seconds. This fixed delay allows the first and subsequent presets to be positioned at the correct time relative to the control region within a clock cycle. Stopping the counter, following the last possible terminal count, is accomplished by another delay as illustrated in the lower part of Figure 1. Here the stopping signal is synchronous with the clocks' positive-going edge but the last terminal count beginning on the negative edge of the delayed clock is already in progress. Since the stop trigger will always be in synchronism with the non-delayed clock for this case, it is only necessary to delay the stop trigger for a period (T_C), one clock period. This delay which may be developed by passive means or active gate circuits, allows the terminal count to be completed before the counters final stopped state is reached and thus spurious transitions or glitches caused by mode shifting while outputting are prevented. The timing shown in Figure 1 for the synchronous trigger case shows that a preset can always be made to bridge the required set-up and hold conditions. In fact, the preset can be extended in width somewhat beyond that shown without fear of overlapping the next set-up interval, see Figure 1.

The synchronous timing sequence shown in the Figure would allow a counter to function throughout a wide range of clock frequencies and starting could be achieved without error because of the synchronous relationships. It is important to note, however, that operation of a circuit with the timing situation shown, would ultimately be dependent on how wide the preset control is relative to the clock period and also on the stability of both delays and presets. Forming the ratio β, of clock period (T_C) to the sum of set-up and hold time value ($T_{SU} + T_H$), and limiting it to values ≥ 1, i.e., letting:

$$\beta = \frac{T_C}{T_{SU} + T_H} \geq 1, \qquad (1.$$

some insight as to the clocking performance bound can be obtained. From Figure 1 and the condition given for β in (1. it is seen that the ($T_{SU} + T_H$) sum could never be allowed to grow beyond the value of T_C without causing more than one set-up time interval to come under the influence of the preset. More that one set-up region under preset influence must be disallowed if counting errors are to be avoided. For $\beta \to 1$, the requirements for accurate jitter-free positioning of the preset function relative to the clocks transition, become exceedingly critical if the maximum capability of the circuit is to be realized. Jitter in either delay or preset width (width modulation) could cause an insufficient amount of time to meet the required values of set-up and hold time. When $\beta = 1$, the dynamic characteristics of the circuit would almost certainly be exceeded by delay and preset width jitter, even if these parameters are very small. The condition $\beta = 1$, consequently, sets the upper boundary for normal clocking; and from (1. this happens when:

$$T_C = T_{SU} + T_H \text{ sec.} \qquad (2.$$

and the upper frequency of normal clocking (f_{max}) is then:

$$f_{max} = \frac{1}{T_{SU} + T_H} \text{ Hz.} \qquad (3.$$

As an example, a high-speed counter, ECL series 10,000, with $T_{SU} + T_H$ = 7 nsec and a terminal count delay of 2 nsec [4] would have a clocking limit of 111 MHz. In practice, single counters of this series operate at about this clocking frequency.[5] When more than one counter is connected in tandem to increase the program counting range, other factors such as carry propagation and decoding delays act to lower the maximum clocking frequency somewhat.

Knowing that β is for a given counting device is helpful in evaluating whether it can perform at a specified clock frequency. For $\beta < 1$, normal preset control would not be expected, while if $\beta > 1$, normal preset control would be expected, because of the non-overlapping nature of the preset pulse width and clock period parameters.

ASYNCHRONOUS TRIGGERING

The synchronous triggering mode outlined above and shown in the counter timing sequences of Figure 1 has limited utility because synchronous triggers are not always available. A means to secure start-stop operation for arbitrary synchronism between triggers and the clock, together with high-speed clocking rates, (say 10 to 100 MHz) and for circumstances where β is small (say between 1 and 2) is a frequently encountered condition in accelerator related systems.

One example occurs when it is desired to provide scope triggering so that the beam bunch structure of a synchrotron can be observed in relationship to the rf cavity gap voltages for discrete bunches. Counting the rf cycles, by use of a start-stop counter started and stopped by system triggers and set to count the machine's harmonic number, allows the necessary stationarity between the functions so that scope viewing is made possible.

An important consideration for the asynchronous start-stop operation which the above example points out, is that the starting and stopping processes must be free of counting error upon start-up so that the exact harmonic number of cycles can be counted and be free of spurious terminal counts and glitches upon stopping so that extra triggers won't be produced. The most significant error upon start-up is "first terminal count error". The first terminal count is defined as the counters initial output pulse, the one which immeidately follows the first preset control pulse. The first terminal count must appear

only at the designated number of clock counts programmed via the data input terminals. More or less than the programmed number constitutes 1st terminal count error. Terminal counts after the first one (follow-on counts) are generally developed in a synchronous manner by ORING the counters output with the first preset control pulse. A single error in counting the number of clock cycles to the first terminal count is a serious error. Large errors over many start-stop cycles may be generated and corrective measures may be impossible to implement due to the random nature of the processes. First terminal count errors may be generated in a number of ways, the more significant being:

(1) The start preset control pulse may have insufficient width to bridge the SET-UP and HOLD time limits of the counter circuit.

(2) The start trigger may be improperly phased with the clock signal, or uncorrelated and excessive jitter may exist between these functions randomly causing an insufficient SET-UP or HOLD time.

(3) The start preset pulse may have a width so large with respect to a clock cycle, i.e., $\beta \ll 1$, that more than one clock cycle passes before the counter is allowed to load the desired modulus.

(4) Noise or voltage transients on the start input may cause multiple starts or intercycle noise.

Depending on the particular situation and the relative statistics of the start trigger and clocking functions, the counting error may be an appreciable number of clock cycles. For the situation (1) above the counter may not start counting at all. For the conditions of (2) above, the counter may function part of the time, skipping some clock cycles. For condition (3) the counters SET-UP and HOLD time requirements will be met upon each start command because more than one cycle is bridged, however, there will always be at least a one-cycle count error associated with the first terminal output pulse. For counting circuits which use the terminal counts in a feedback control operation to activate cycle-by-cycle presetting and loading lines, these errors affect operation deleteriously.

Extra terminal counts and spurious outputs upon stopping are equally serious errors and may be the result of:

(1) The stop trigger being coincident with a terminal count, preventing the counter from reaching a stable state during its final transition, i.e., mode shifting while outputting.

(2) Noise on the stop trigger input.

(3) Too short an interval between starting and stopping, i.e., stopping following a start but prior to the time a stable condition is reached.

This rapid mode shift causes glitches (multiple outputs) which may be interpreted as true terminal counts when these signals are actually false outputs.

Figure 2 shows several timing sequences associated with a typical start-stop scaler operating near its upper frequency limit. The figure illustrates how counting errors are developed as a result of asynchronism between start triggering and input signal. The applied start triggers are shown at different times within the timespan of a single input cycle, sequence (A), to illustrate the range over which typical triggers may exist. The set-up and hold time intervals are identified together with the extent of the control regions ($T_{SU} + T_H$ sec.), throughout which the preset pulse must be present for proper start-up counting operations. The preset control pulse sequences (B, C, D) of Figure 1, are based on: (1) all preset control pulses start at the leading edge of the applied start triggers, (2) the input signal being delayed for T_{SU} seconds to force at least one preset control pulse to meet the SET-UP and HOLD requirements, and (3) the sequences (B, C, D) are shown for preset control widths of 1, 3/4, and 1/2 period of the input respectively to aid in examination of the overall timing relationships.

By inspection of sequences (B, C, D) relative to the control regions, it is observed that not every illustrated, preset pulse in the sequences satisfy the necessary timing for correct start-up, i.e., only some (those marked +) of the preset control pulses bridge a control region. In the majority of the cases shown, either insufficient set-up or hold time is available for normal control gate functioning or the preset control pulse falls entirely outside the region when normal presetting/loading could be initiated. All of these conditions produce single or multi-count errors or a missed cycle resulting in no terminal count. A similar error generating condition exists for other

trigger positions, signal delays, and preset control pulse width values. In about only half of the situations shown would a successful first terminal count be achieved and outputted at the correct time.

At first glance, a gated clock activated by processing the start trigger would appear useful since the first clock cycle could be made to commence a fixed delay increment equal to the counters set-up time after the start trigger. The preset control pulse initiated by the start trigger would always be in synchronism with the outputted (gated) clock. At high frequencies, however, the technique fails under asynchronous triggering, because a fractionated first cycle is developed - the gate catches the clock at various points along its cycle and the resultant clock signal has a foreshortened first cycle. Set-up and hold parameter requirements can not be met under all the short-cycle conditions and the counter is subject to the aforementioned errors. Still other methods, using width modulation, delay modulation, etc., do not appear applicable because they do not reduce the timing uncertainty between clock signal and start triggers which is the basic problem.

Obviously another method is required if the stated drawbacks are to be removed and the timing uncertainty reduced.

Suppose the applied clock signal frequency is multiplied by an integer $N > 1$ to form a signal which is thereupon immediately divided by N. The resultant function (a pseudo clock) will have the same frequency as the applied clock but the division process can be made to operate on transitions occurring at T_c/N sec. rather than those at T_c sec. An edge triggered "D" flip-flop used as a simple divider ($\div 2$) can operate in this manner, while other correspondingly simple circuits can provide other division ratios. As a result of the dividers action the timing uncertainty between the pseudo clock signal and a start trigger can be reduced from T_c to T_c/N sec. A preset control pulse having a specific width can then be formed which can be forced to bridge the set-up and hold regions required for asynchronous operation. To accomplish this it is only necessary to make the preset width (T_P) equal to:

$$T_P = T_{SU} + T_H + \frac{T_c}{N} \text{ sec.,} \qquad (4.$$

at the highest clocking frequency of interest and to fix the position of the preset relative to the clock by introducing a delay in the pseudo clock signal of T_{SU} sec.

A detailed synchronization method based on the above concept and which removes the counting and error generating problems outlined earlier has been used by the author. The method prevents first terminal count error by developing a preset control function which always is in the correct position to meet the set-up and hold dynamics of a given circuit. The method is very useful, but not restricted to clocking frequencies in the decade from 10 to 100 MHz and consists of the following 5-step process. Refer to Block Diagram Figure 3.

Step 1 - The circuit or scalers preset control pulse, and clock lines are normally maintained at a logic level corresponding to $\overline{\text{LOAD}}$; waiting for the pulse and transition which will start the triggering/loading and counting process.

Step 2 - A pseudo clock signal, delayed by an amount of time corresponding to (T_{SU}), is developed by first, multiplying the applied input signal frequency by an integer N, N>1, (2 for the case shown) and secondly, immediately dividing the resulting product signal by N through the use of a suitable high-speed edge triggered, gated, flip-flop (CLOCKING F-F) which is controlled by a second R-S flip-flop (START F-F) interconnected to the start trigger and the ENABLE terminal of the (CLOCKING F-F), as in Figure 3.

Step 3 - The applied start trigger, occurring at any time during the applied clock signal, forces a transition in the state of the (START F-F) which in turn permits the (CLOCKING F-F) to commence toggling only after the recept of a positive clock input edge, i.e., the first positive-going signal edge following the start trigger establishes the start of a pseudo clocking train whose period equals that of the input signal but without a fractionated first cycle as would

result from simple gating processes of the applied signal. The start-up phase of the pseudo clock is, therefore, always in synchronism with the start trigger and the timing uncertainty has been reduced from (T_c sec.) to ($\frac{T_c}{N}$) sec.

Step 4 - The counters first preset control trigger, as required in Step 1 above, is developed directly from the start triggers leading edge through the use of a ONE-SHOT whose duration (T_P) is adjusted for; $T_P = T_{SU} + T_H + \frac{T_c}{N}$ sec. Follow-on presets, utilized to continue the counting process after the first preset are derived from terminal counts, always T_c in width, fed-back to the preset line through fast gates; see Figure 4. The counter will cycle after starting until a stop trigger is applied to initiate the stop processes.

Step 5 - Stopping the counting process is achieved by: (1) reestablishing the pre-start state of the (CLOCKING F-F) gate control terminal thereby ending the pseudo clock signal. This process is delayed, however, until a terminal count has been completed, i.e., stopping is delayed if a terminal count appears coincident with a stop trigger, and (2) an inter-START/STOP inhibit gate, generated by application of the start and stop triggers to their respective (START F-F) and (STOP F-F), is applied to the decoding gate/s to prevent noise or spurious signals from appearing at the output lines within the time interval between the stop trigger + T_c and the next start trigger transition times.

The timing sequence applicable to the outlined synchronization method is shown in Figure 4. As before, the start triggers represent possible start times and sequence (B) indicates the pseudo signal resulting from the multiplication and division processes. Sequence (C) compares the pseudo signal and preset control region for the applied trigger positions. Note that in contrast with corresponding sequences (B, C, D, and delayed signal) in Figure 2, that the sequence (C) of Figure 4 contains a preset control pulse at the correct time (bridging the control region) for all positions of the start

triggers. It can be shown, further, that for any other possible position of the start trigger, interior to a clock cycle, this favorable relationship is maintained.

The above synchronizing method has been applied to the design of high-speed scalers configured in the "synchronous parallel carry" connections of Figure 3. This configuration is used to obtain a large range in divide modulo while at the same time maximizing counting speed and minimizing the possibility of counting error due to variations in input signal period. As in Figure 3, the signal to be scaled is applied to the clocking terminals of all stages within the scaler simultaneously. The carry advance data instead of slowly rippling from one stage to the next, are developed by high-speed external decoder gates and propagated via minimum-delay paths to appropriate carry-in terminals. The scalers cyclic terminal count pulses not only constitute the required scaled output but have the required synchronism and the correct logic levels to meet the presetting/loading control requirements for cyclic operation. The terminal counts are, therefore, fed-back directly to the preset/load control terminals of each counter stage in the scaler to establish the cycle-by-cycle preset/loading operations. With the described feedback connection, the scaler can follow variations of the input frequency adaptively while maintaining programmability even for cycle-to-cycle modifications in the divide modulo. By selecting the appropriate control mode connections, upcount, down count, and preset control or hold count operation and by application of the necessary data to set the divide modulus, the counter begins to cycle upon simultaneous application of the input signal and preset control pulse. The output is obtained either by decoding four output data lines or by utilization of the carry advance information.

CLOCKING FREQUENCY LIMITATIONS

The bound for clocking frequency under start-stop triggering for the asynchronous case has a limit just as in the synchronous case discussed earlier. For the asynchronous case, however, the maximum start-trigger clocking rate may be quite difference from the continuous clocking limit. The

start-stop limit depends mainly on the values of the set-up and hold times and on the multiplication/division factor (N). The continuous clocking limit is also dependent on the set-up and hold times and on the total carry advance and decoding delays used to develop a continuous train of presets following the first one, but not on (N). The independance relative to (N) is due to the self-synchronous nature of the feedback presetting process.

The start-up clocking limit is imposed when the preset width (T_P) equals the clock period (T_c). From (4., this happens when:

$$T_c + T_{SU} + T_H + \frac{T_c}{N} \text{ sec.} \qquad (5.$$

$$\text{or} \quad T_{SU} + T_H = T_c \left(1 - \frac{1}{N}\right) \text{ sec.} \qquad (6.$$

$$\text{and} \quad f_{max} = \frac{1}{T_P} = \frac{(1 - \frac{1}{N})}{T_{SU} + T_H} \text{ Hz.} \qquad (7.$$

As an example, a counter circuit with $T_{SU} + T_H = 7$ nsec., N = 2, from (7. would have a maximum start-up clocking frequency of:

$$f_{max} = \frac{0.5}{7 \times 10^{-9}} \approx 72 \text{ MHz.} \qquad (8.$$

Note however, from (4. that the preset pulse width could be made smaller if (N) is increased. For N = 4 say, and for $T_{SU} + T_H$ as above, f_{max} increases to 107 MHz; a significant improvement. Alternatively, if it is desired to determine whether start-up clocking could be achieved at a given frequency, β could be evaluated from:

$$\beta_{max} = \frac{T_c}{T_{SU} + T_H + \frac{T_c}{N}} \qquad (9.$$

For $\beta \geq 1$ start-up clocking and control without terminal count error would be expected. For example, suppose the clock period (T_c) is 20 nsec, (50 MHz clock), N = 2, and $T_{SU} + T_H = 7$ nsec, as before. For this case $\beta = \frac{20}{17} = 1.17$, and the circuit would clock correctly upon the application of the start trigger.

The performance of the starting conditions of course, must be compatible with those of the continuous counting conditions if a given circuit is to operate throughout a start-to-stop cycle. From Figure 4, sequence (C), a terminal count is shown beginning at the negative-going edge of the pseudo clock. A terminal count starting at this time is consistant with terminal count development for self-synchronous counters. Note that for the condition where the terminal count is processed to develop the next preset as in the case for the timing diagram shown, that a total delay of T_D sec. could elapse before the set-up time boundary of the next clock cycle is reached. If delay T_D were larger than $(\frac{T_c}{2} - T_{SU})$ sec., Figure 4, the set-up conditions could not be met and an error would result. The maximum continuous clocking when feedback methods of generating the preset are used is, therefore:

$$f_{max} = \frac{1}{T_{c_{min}}} = \frac{1}{2\,(T_{SU} + T_D)} \text{ Hz.} \qquad (10.$$

For (T_{SU}) = 3 nsec, typical for an ECL device, and T_D = 5 nsec. (to represent the total carry advance and decoding delay), the maximum continuous counting frequency $f_{max} \approx 63$ MHz. Since this value is somewhat below the start-up conditions for the same circuit parameters (72 MHz) as before, the limiting factor in the operation is the long delay in developing and returning presets for use during continuous cycling conditions. A reduction of only one nanosecond in the delay would, however, make the limits equal. Values of N > 2 would, therefore, provide no improvement in counting frequency without reducing T_D more than 1 nanosecond. For very small T_D, say 1-to-2 nsec, increasing N to 4 would increase the counter upper clocking performance.

Operation at 100 MHz, requires $T_{SU} + T_D$ to be 5 nsec maximum, a value which is achievable with high-speed logic circuits such as MECL III[6] or equivalent circuits.

In APPENDIX I, a detailed discussion of the starting and stopping sequences for a typical counter are given together with a brief resume of the intercycle inhibit operation. In APPENDIX II, jitter is discussed and an effective and simple technique to multiply the frequency of the input signals using rf hybrid junction and exclusive OR gates is discussed.

CONCLUSION

Triggering a high-speed counter without start-up or stopping error has been achieved for the condition that the start-stop functions are asynchronous to the applied clocking function.

The method employed to achieve this is through frequency multiplication of the applied signal, subsequent frequency division of the product by a gated, edge triggered, flip-flop, and the development of a preset control pulse timed to always bridge a counters set-up and hold time boundary. Stopping the count action without extra pulses or glitches is achieved by delaying the stop function if the stop command appears coincident with a terminal count.

A high-speed scaler optimized in the 40-to-60 MHz range and having a counting range of 2-to-9999 with 40 mV rms sensitivity has been constructed from the outlined method. Clocking frequency in excess of 100 MHz appear possible under start-stop operation. The counter is presently providing R & D diagnostic data on the Fermilab machine's bunch structure as well as providing a standardized "trigger" for scoping machine related signal functions.

A parameter, β, relating the counters circuit dynamics to clock period and the multiplication/division factor has been developed to provide an insight as to the maximum achievable start triggering clocking speed for a given circuit.

NOTES

1. T_H = The minimum time a signal is retained at a particular point in a digital circuit following a transition, and also, the minimum time following a transition that data must remain unchanged to meet proper dynamic circuit requirements.

   T_T = The time between defined "HI" to "LO" or "LO" to "HI" voltage levels at a specific terminal in a digital circuit.

   T_{SU} = The time interval for which a signal is applied and maintained unchanged at a specific input terminal of a digital circuit before an active transition occurs at another terminal, and also minimum time before a transition that information must be present to ensure meeting proper dynamic operation of a circuit.

2. Error-free, as applied to logic gates: The applied signal does not violate either the set-up or hold time parameters associated with the gate; as applied to a counter, $f_{out} = f_{in}$ divided by the programmed modulus under all control conditions - exactly.
3. Universal counters employing Medium Scale Integration techniques of the MECL 10136/37; Motorola devices, and F95016/10 series; Fairchild Semiconductor, Inc.
4. Assuming terminal counts are used in a feedback arrangement to control the counters cyclic control pulse operation.
5. See Motorola, Inc., Report on Counter Applications, NOTE #584; Motorola Semiconductor Products, Inc. 1972.
6. Motorola Incorporated - Semiconductor integrated circuit having nanosecond gate delays and toggle frequencies to 500 MHz.
7. Motorola series 10,000 or equivalent.
8. See Designing With TTL Integrated Circuits, McGraw Hill Book Company, New York, New York; 1971, Chapter 10.

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APPENDIX I

START SEQUENCE

Referring to Figure 3, the applied clock signal is multiplied by the smallest multiplier N = 2, associated with the outlined technique. By multiplying the applied clock signal by N = 2, at least one positive-going transition is made to exist interior to each clock cycle period (T_c), Figure 3 and 4, top. Application of the multiplied clock signal (2f) Figure 3, and a negative-going enable gate started by the leading edge of the START trigger allows the CLOCK F-F to begin toggling on the first positive transition of the multiplied clock. A sequence of triggers and the associated pseudo clock signals illustrating this action is shown in the upper part of Figure 4. Here the triggers Sequence A are positioned at various time points within the applied clock's cycle and the resulting pseudo clock signals are shown in Sequence B. Note that a shaded region surrounds the pseudo clock signals to show the timespan which must be bridged by the preset to accommodate the counters starting dynamics. The timewidth of this region is defined by the sum; $T_{SU} + T_H$. Note further, that the pseudo clock has the same period as the applied clock - a direct result of the divide-by-2 action of a simple flip-flop. The clocking flip-flop of Figure 2 also contains a connection from the enable input to the reset (R) input so that the pseudo clock output signal will be forced to: (1) always start from a logic "0" reference level upon application of the start trigger, and (2) always end on the logic "0" level upon application of a stop trigger. This reset circuitry standardizes the counter loading process making it the same each and every time a start-stop sequence is commanded. The counters first preset is developed by the PRESET ONE-SHOT, Figure 3, whose trigger input is the leading edge of the START trigger and whose duration (T_P) is adjusted by a simple R-C network to $T_P = T_{SU} + T_H + \frac{T_c}{N}$ = 1 clock cycle as shown in Figure 4, Sequence C. The PRESET ONE-SHOT is protected from spurious start signals by an inhibit gate derived by the START F-F. The first preset developed by this circuitry is shown in the Sequence C of Figure 4, where it is shown together with an associated delayed clock signal. In each case the preset bridges the required region about the clocks positive transition for each and every position of the

START trigger. For other trigger positions the relationship is maintained. The counter is thus forced to start without counting error, skipping, etc., even for asynchronism between the applied clock and START trigger. To be sure that follow-on presets are timed correctly and the scaler made to follow input frequency variations, it is only necessary that the positive-going terminal counts be ORED with the first preset and distributed the counters preset control line through a gate, PRESET GATE, Figure 3.

STOP SEQUENCE

To stop the counting sequence, a delayed stop trigger is introduced to the START F-F causing it to produce a transition which ends the toggling of the CLOCKING F-F, returning the output to a logic "0". This action stops the counter but only after the STOP GATE, Figure 3, passes a final terminal count via a delay line whose transit time is set for the longest clock cycle period (T_c). In this way the counter is allowed to count through a circumstance where the STOP trigger is coincident with a terminal count. The counters are thus allowed to reach a stable stopped state. The outlined stopping sequence is much simplier to augment than the start sequence but some delay in stopping is the penalty for the method. There are nevertheless, other options which may be applied to the stopping process, for example, by the addition of gates connected to the clock and to the terminal count decoder outputs, one may initiate a stop command on the first CLOCK cycle following a STOP trigger in the absence of a terminal count.

INTERCYCLE INHIBIT

The START F-F's $\overline{Q}$ output is connected to the final decoding gate circuit, Figure 3. This circuit connection inhibits the decoding process from the time a delayed stop pulse is developed until the next START trigger is received. The output circuits thus have a forced logic "0" state during the interval. This circuit protects external circuits from noise and spurious signals as well as standardizes the output conditions during the interval.

APPENDIX II

JITTER

Two jitter parameters are relevant, (1) jitter of the output terminal count signal relative to the input signal, and (2) jitter of the output terminal count signal relative to the start trigger pulse. The first type of jitter has been minimized to < 0.1 nsec by using synchronous[8] counting techniques and circuit design features such as: (1) tandem connected logic gates to form a hard limiter at the input signal line. This procedure maintains the maximum slew rate in the logic "1" - "0" aperture range and minimizes the possibility of jitter induced from input amplitude variations. (2) Power supply potentials are highly regulated, 0.05%, so as to minimize bias level variations for all IC gates, and (3) shielding and grounding devices are used to minimize coupling between the clock and control lines and between output and input signal lines.

The second jitter parameter, output jitter relative to trigger pulse, is reduced by the triggering method outlined. Since the applied signal is multiplied by N the CLOCK F-F, Figure 3 operates with a period of $\frac{\text{Applied Clock Period}}{N}$. The jitter in the pseudo clock signal relative to the triggering pulse is thus reduced by the factor N. Becuase the pseudo clock signal is the true input to the counting chain, the output jitter relative to triggering is also reduced by N, an important contributing factor to the stabilization of circuits which utilize the scaled output data.

MULTIPLICATION PROCESS

In Figure 3, note that the method of multiplication is achieved by using a 4-port rf coupler, a quadrature hybrid, in combination with logic IC's. The forward properties of the coupler produces two equal amplitude signals phased in time quadrature at Ports 2 and 3. The reverse properties produce a signal at Port 4 which is proportional to output load reflections. The reverse signal port is terminated in a matched load and is otherwise not used. For a broad

bandwidth multiplier it is only necessary to apply the quadrature output signals to an exclusive OR/NOR gate to obtain a doubling of input frequency. Above 10 MHz the method produces a signal with reduced harmonic content* - no filtering is required, while operation is achieved over a broad bandwidth and implementation is extremely simple in the 10-to-100 MHz range.

The hybrid exclusive OR/NOR method of multiplication has many advantages over mixer, fixed delay, or snap diode/filter array techniques among which are: (1) the hybrid couplers require no dc power, they are passive components, (2) the circuit is directly connectable to standard impedance coaxial lines - 50Ω matching easily achieved, (3) bandwidth approaches 2 decades, (4) ECL logic levels and impedances are directly compatible with the outlined circuit approach, (5) excellent isolation is afforded between input and output > 30 dB by the coupler and IC combined, and (6) mechanical interfaces are easily achieved since the coupler approaches the size of a 14 pin in-line IC package.

*Logic gates begin to act as bandwidth limited linear amplifiers having associated filtering properties.

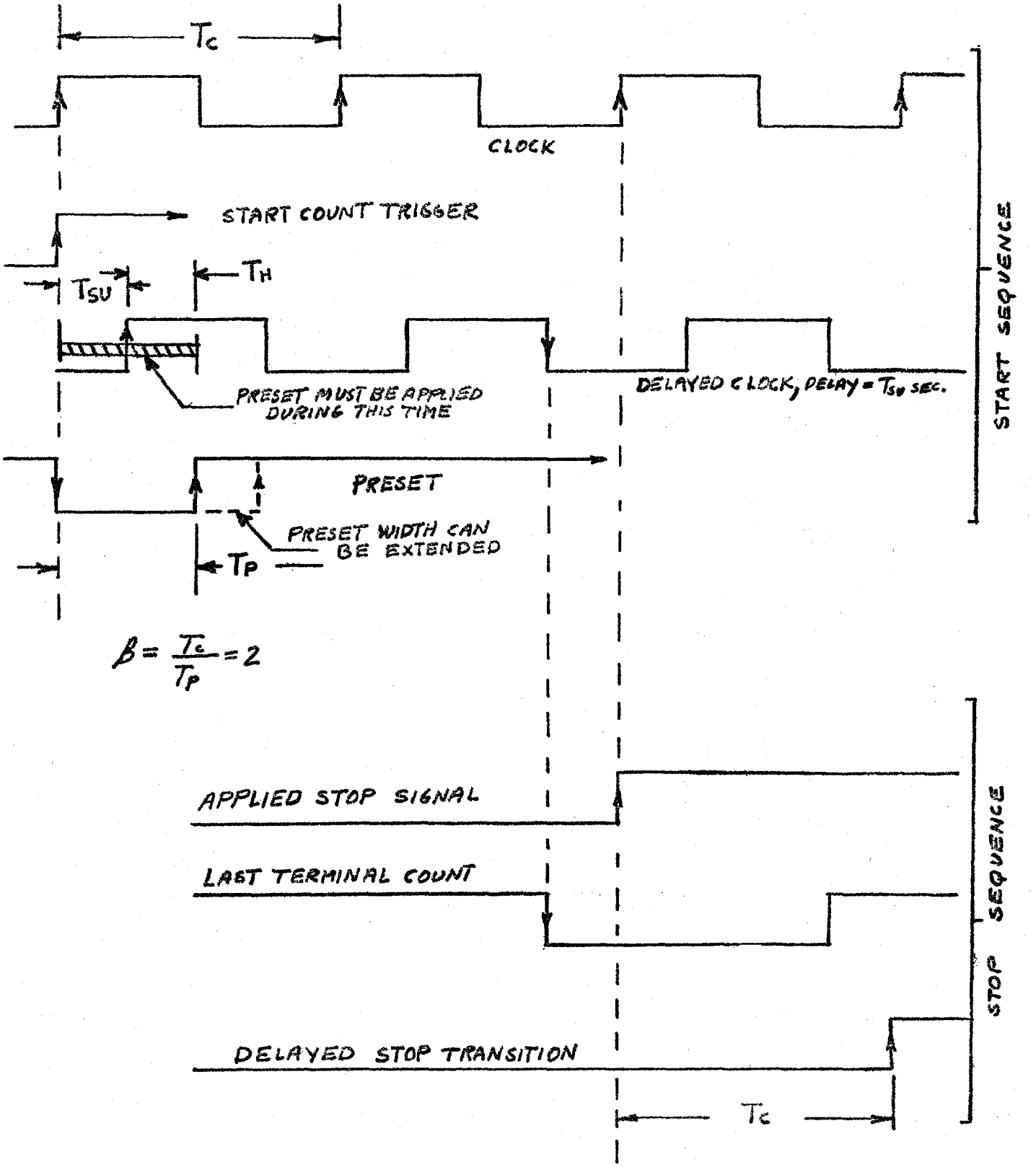

FIGURE-1
COUNTER TIMING SEQUENCE
FOR SYNCHRONOUS START-STOP TRIGGERS

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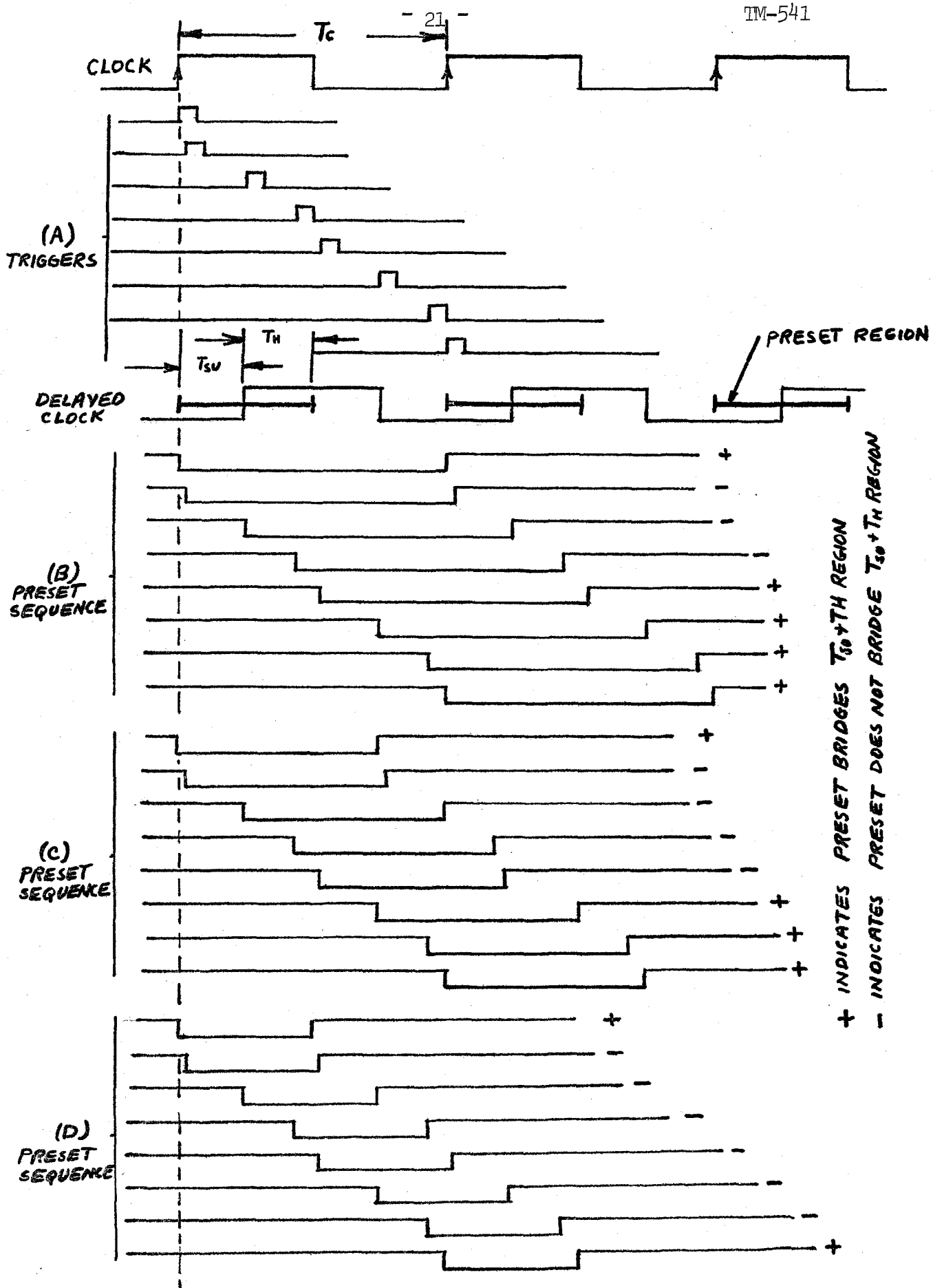

FIGURE-2

COUNTER TIMING SEQUENCE - NO CLOCK MULTIPLICATION, VARIBLE PRESET WIDTH

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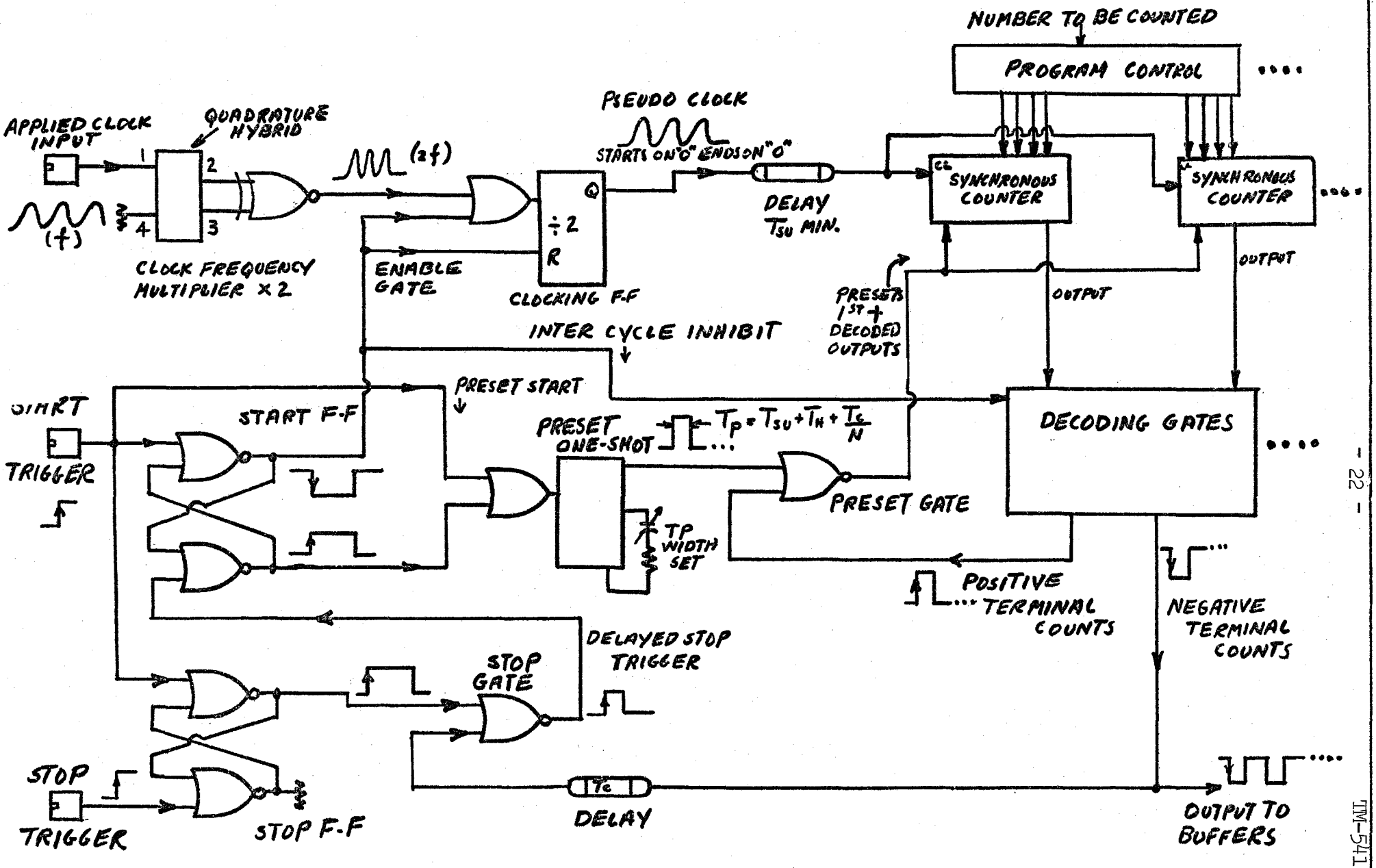

FIGURE - 3

BLOCK DIAGRAM OF SYNCHRONIZATION METHOD

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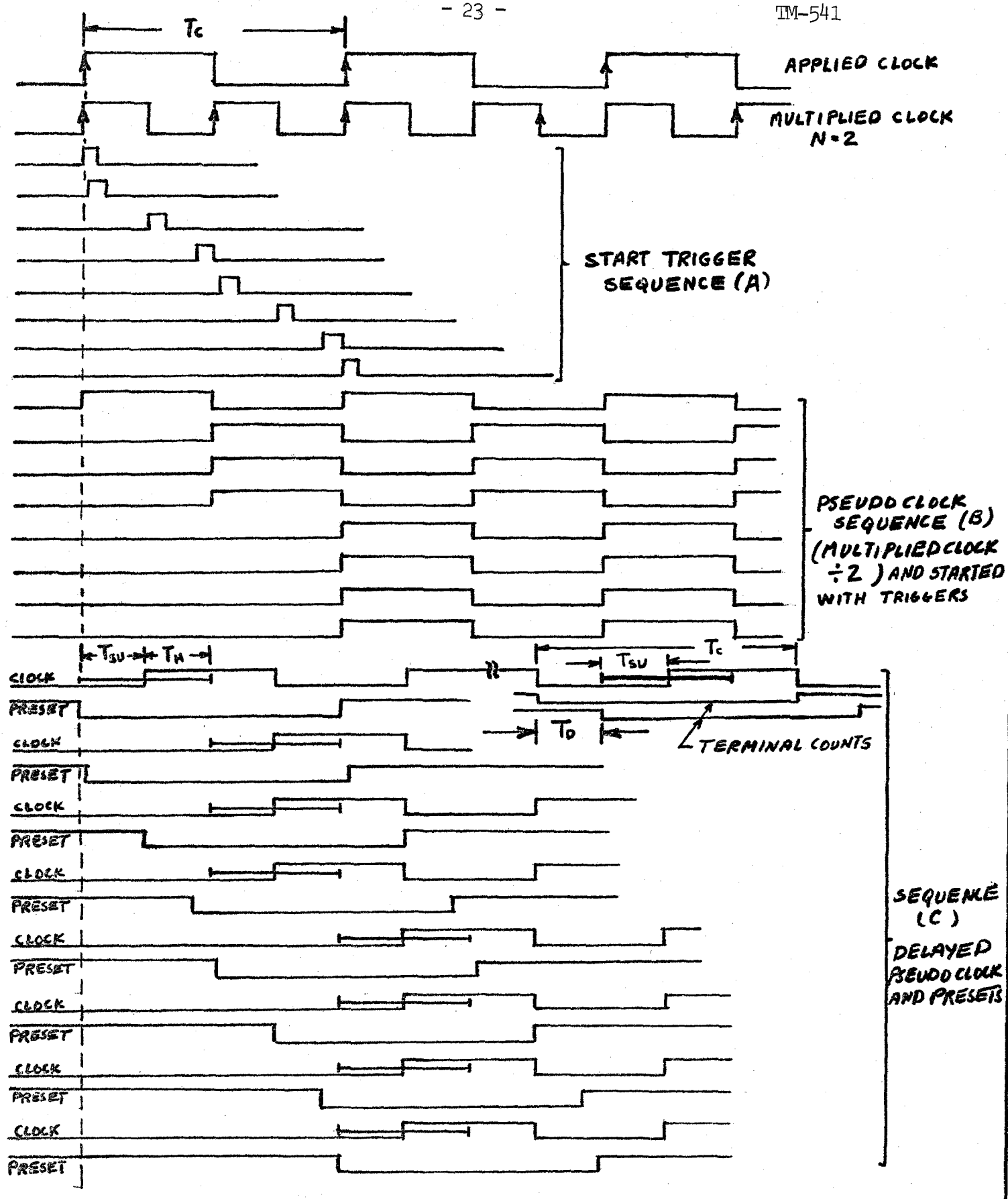

FIGURE-4

TIMING SEQUENCE - ASYNCHRONOUS CLOCK & START TRIGGERS
PRESET BRIDGES ($T_{SU}+T_H$) TIME AFTER PROCESSING CLOCK & TRIGGERS
CLOCK MULTIPLICPTION, N=2, B=1

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