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A MULTIPLEXED CONTROL SYSTEM FOR THE NAL MAIN ACCELERATOR*

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SUMMARY

The control system for the NAL Main Accelerator Ring is based on a distributed multiplex technique which uses serial transmission of digital data to link 24 service buildings to a central computer system. Each service building contains logic for conversion of serial data to parallel format and parallel to serial. Data transmission cables form a large loop that extends around the four mile circumference of the accelerator so that data transmitted from a central communications controller goes to each service building sequentially and then is returned to the central controller. The communications controller is an integral part of the interface electronics for a MAC-16 minicomputer which serves as a real-time controller for ring subsystems. The MAC-16 is connected to control console electronics and to a second minicomputer used for Main Ring power supply fine control. In the near future, the MAC-16 will be linked to an XDS Sigma II computer that serves as a central controller for the entire accelerator complex.

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Control System Organization

The Main Accelerator control system, like the control systems for the Linac, Booster Accelerator, RF and Beam Transfer, will eventually become a satellite to the Xerox Data System Sigma II central control computer.[1] However, in order to avoid complete dependance on the Sigma computer, all control systems are as modular as possible. There are two practical consequences of this philosophy. First, the Sigma II is not required to operate in "real time"; this function is relegated to the satellite control computers. Second, satellite control systems can operate in a stand alone mode, independant of the vicissitudes of the central computer. At present, the Main Ring Control System operates only in the stand alone mode.

The Main Ring control system uses two Lockheed Electronics Corporation MAC-16 computers. One of these, Computer A in Figure 1, is the primary real-time controller for the Main Ring. Computer B is dedicated to software control of the magnet power supply fine control system.[2] Both computers communicate with remote stations via communications controllers which serialize the digital data, transmit the serial information to ring loops and convert serial data returned from the ring loops to parallel format. Both systems use identical though separate electronics. Remote station, electronics, called House Logic Units (HLU), may be inserted anywhere in a transmission loop by simply installing another repeater station in the loop.

Control Computers

Each of the two MAC-16 computers contains 8K words of memory, 16 priority interrupts, a real-time interface and 2 input/output channels. Computer A will be upgraded in the near future to a 16K memory. The interface electronics shown in Figure 1, are connected to the Programmed Data Channel (PDC), which is a standard I/O channel operating under direct program control through the A register. The second I/O channel, the Multiplex Data Channel (MDC), is similar in operation to Direct Memory Access as provided on older computers such as the Varian 620i. The MDC channel is reserved for the MAC-16/Sigma II serial transmission link. Interface electronics contain a special real-time clock operated from the 2k Hz Main Ring master clock. The interfaces include special registers and gates for linking computers A and B, an 8 channel digital output multiplex (A only), an 8 channel digital input multiplex (A only) and special registers and gates for the communications controllers.

The Distributed Multiplex Control System

Since electronics for both the Ring Control System and the Main Magnet Fine Control System are essentially identical, the following discussion will be limited to the Ring System.

Serial Data Format

Data transmissions use a 32 bit serial "word" which contains all information required to control remote station logic. Data is organized in a "packed" format, as shown in Figure 3. The first bit, t_{QO}, is a synchronizing bit. The 5 bits assigned to House Address select a service building or "House". The next three bits, the Device Address, are used for the first level of multiplexing in an HLU. The following four bits are for command control of HLU operation. Then follow three response bits which must be generated by the addressed HLU. The last 16 bits are reserved for data to or from the House. Synchronization of the serial data word is accomplished by a burst Data Clock, TCLK, transmitted on a separate, parallel wire.

Communications Controller

The communications controller supervises all data transmissions to and from the ring loop. This includes forming the packed control word, serializing it, reading back the return word and checking for remote logic and transmission errors. An essential feature of the Communications Controller is that it can operate separately from the computer. Once a serial transmission is begun, the transmission cycle will proceed automatically until the data returning from the ring loop is shifted in and checked. HLU commands generated by the communications controller are based on MAC-16 PDC command bits: The Digital Input (DI)

bit causes data to be returned from an HLU, the command Output (CO) bit sets control information into subunits in an HLU - primarily for selecting I/O channels in HLU multiplexors. The Digital Output (DO) bit causes data sent to the ring to be stored in an addressed HLU register, and the SI, or Status Input bit causes the HLU to send back information about its latest operating mode.

Not all capabilities ascribed to the communications controller are now implemented. In particular, formating of the packed serial words and checking of returned words are done by the control program. This necessitates two output and two input cycles of the 16 bit PDC bus for every ring transmission. The final system will require only one output and one input operation per transmission.

The Data Transmission System

The transmission loop consists of 6 shielded-twisted pair cables bundled in a common jacket. The pairs are similar to Belden type 8227 cable with a differential Z_o of 96 ohms. Line repeaters are located in each service building so that every line driver must drive about 1100 feet of cable. The master transceiver uses electronics identical to service building repeaters except that connections between line receivers and drivers are cut and diverted to the communications controller. Texas Instrument SN75107 balanced line receivers and SN75110 balanced line drivers are used throughout. Two 75110's are always used in parallel to increase the drive currents to 24 mA. In this configuration it

is possible to transmit at a pulse rate in excess of 7MHz, over a 1000 ft. length of cable. The only disadvantage to the 75107 series receivers and drivers is their low common mode voltage limit, ± 3 volts. Since each wire of a pair, at both transmitting and receiving ends, is terminated in 47 ohms to ground, no significant problems with common mode signals in excess of 3 volts have been encountered.

The six pairs carry the following signals: Serial data (at 1 MHz bit rate), burst data clock (at 2 MHz), 2 kHz Main Ring Master Clock, Main Clock reset serial data fault response and Main Ring clock reset response. Since the six pairs are not yet installed beyond the second superperiod, the burst data clock and serial data are looped back on the two response lines whose repeaters transmit in the reverse direction from normal signal flow.

Service Building Logic

Three cables are required to connect service building logic to the serial data transmission system: Serial data in (SDIN), Burst Clock in (TCLK), and serial data out (SDOT). Each of the 24 HLU's must shift in the House Address, Device address and command bits. However, command bits are stored only by one, addressed HLU, except in the aggregate command mode, where all 24 HLU's respond to a CO or DO command. Aggregate addressing is not permitted for DI or SI commands. The addressed house must respond by inserting command response bits in the appropriate time slot of the serial word. The command response bits and data

generated by a DI or SI command must be inserted in the appropriate time slots of the original serial word "on the fly". This is accomplished by connecting the SDOT line to an OR gate integral to the 75110 drivers. All I/O operations are completed within the 32μs length of the serial word.

Multiplexing of parallel data in an HLU occurs on two levels. The first level is direct to Device controllers (see Figure 3) via the device address bits transmitted as part of each serial word. The second level occurs within Device Controllers and requires a CO command. Since channel addresses are stored by each Device Controller, only one CO command is required for a sequence of DO or DI commands - except the Analog to Digital converter which uses the CO command as a "convert" pulse.

Error Checking

Parity checking has been ommitted from the Multiplex System. A combination of HLU generated response bits and bit-for-bit comparison of transmitted and received data words provides a more stringent verification of data transmissions. In all transmissions, the first 13 bits - t_{oo}, House Address, Device Address and command bits - must be returned to the communications controller exactly as sent, and for a DO, CO or DI command, the appropriate command response bit must be returned. There is no SI response bit. Consequently, the pattern of the first 16 bits of the returned serial word is known. For a DI command the returned bits of the data word, which were transmitted as zeros are, with some exceptions, not known a priori. An SI command, will cause the appropriate HLU address, hardwired into each unit, and the transmitted device address bits to be returned in bits

2^8 through 2^{15} of the data word. Bit 2^7 indicates the remote/local operating mode of the HLU, and bits 2^0 through 2^6 will return the contents of the channel address register of the device controller selected.

Acknowledgements

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References

1. Klaisner, L.A., et at. "Central Control System for the NAL Accelerator", Paper F-30, Proceeding of the 1971 National Accelerator Conference.
2. Cassel, R. and Pfeffer, H., "The Power Supply System, Control and Response of the NAL Main Accelerator", Paper K-6, Proceedings of the 1971 National Accelerator Conference.

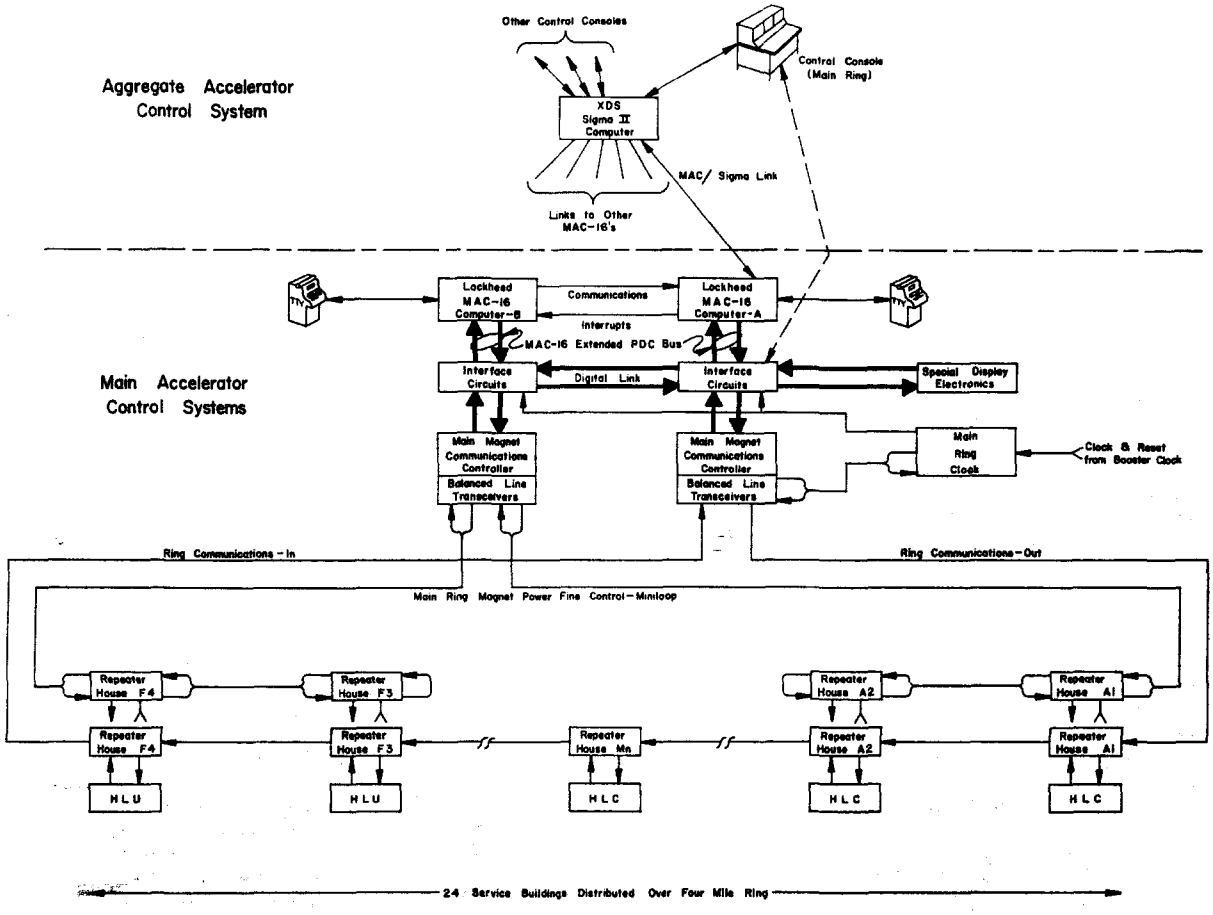

Figure 1. The NAL Main Ring Control System

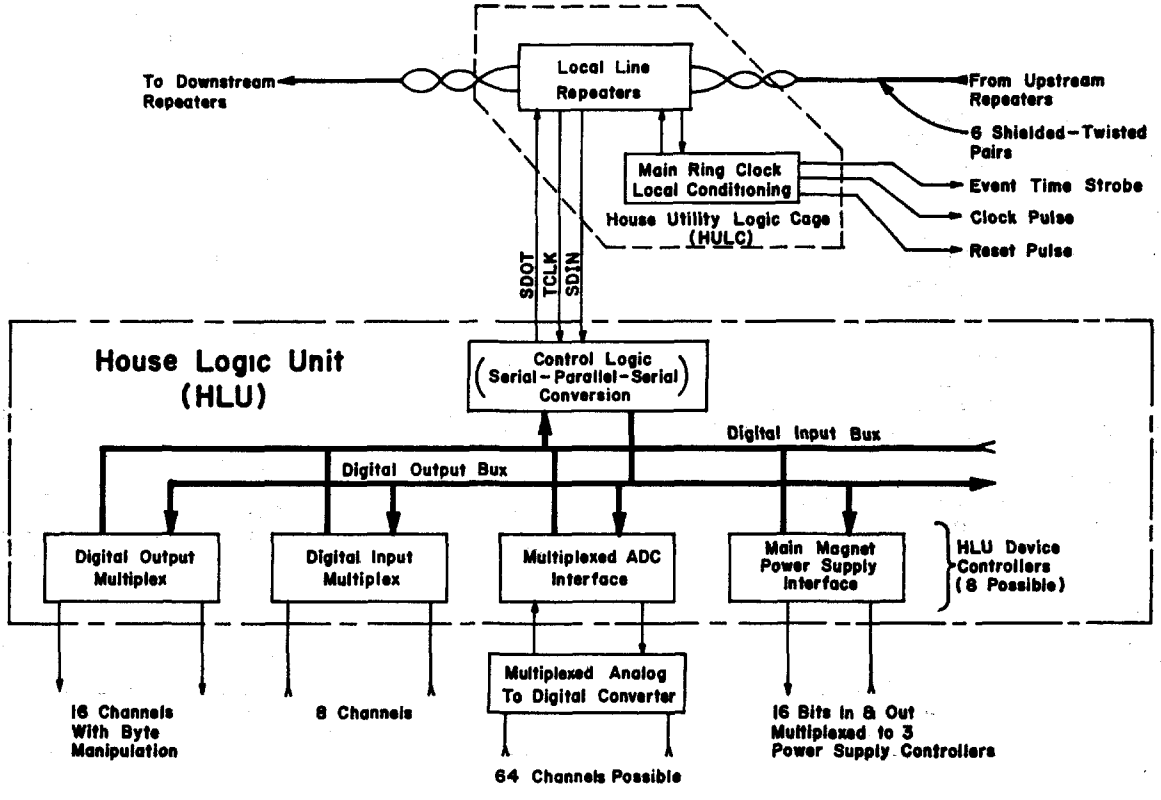

Figure 2. Typical Main Ring Service Building Logic

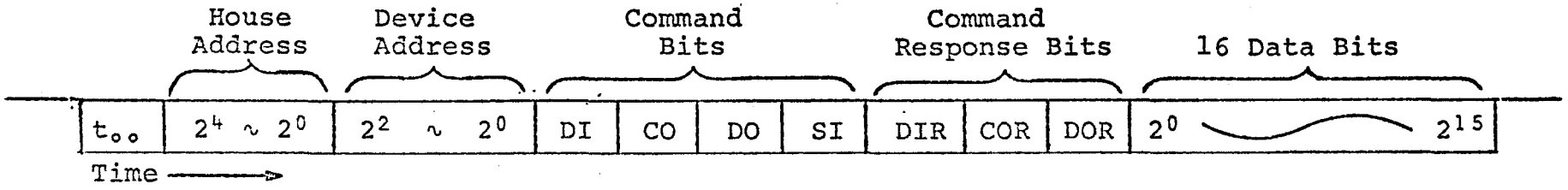

Figure 3. Serial Data Word Format

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