Analysis and Grading of the Test Performance of PS Modules for the CMS Phase-II Outer Tracker Upgrade

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The Outer Tracker detector of the Compact Muon Solenoid (CMS) experiment provides information about the trajectory of charged particles produced in proton-proton collisions at the Large Hadron Collider (LHC). During the High Luminosity LHC upgrade, scheduled for the late 2020s, the Outer Tracker will be replaced with new modules capable of transmitting data to the L1 Trigger. These modules are being assembled at several facilities around the world, including Fermilab, necessitating coordinated standards of module quality. Here I discuss the development of POTATO (Phase-II Outer Tracker Analyzer of Test Outputs), a C++ software which provides a standardized procedure for analyzing and grading test results of the Outer Tracker modules. The particular focus of this paper is on the analysis and grading of the PS (pixel-strip) modules in POTATO.

I. INTRODUCTION

At the CERN Large Hadron Collider (LHC), beams of protons moving at near-relativistic speeds are collided, producing showers of high-energy particles which can be studied to investigate open questions in physics. Over the next few years, the LHC is preparing to be upgraded to increase its instantaneous luminosity by a factor of 10 with respect to the nominal one. The Compact Muon Solenoid (CMS) is one of two general purpose experiments at the LHC, and it will likewise be undergoing an upgrade during this time. In this paper, the upgrade of the CMS Outer Tracker will be discussed, with particular focus on the process of assembling and testing the new tracking modules.

A. Outer Tracker

The Outer Tracker (OT) provides information about the trajectory of charged particles produced in LHC proton-proton (pp) collisions. The OT is made up of several layers of silicon modules arranged in one barrel and two end-caps, as shown in FIG. 1. When a charged particle passes through these sensors, a signal is produced, from which the path of the particle through the detector can be reconstructed. Two types of sensors are used: the PS (pixel-strip), arranged on the interior layers closer to the beam, and the 2S (strip-strip), placed farther from the center. This paper is specifically concerned with the PS modules.

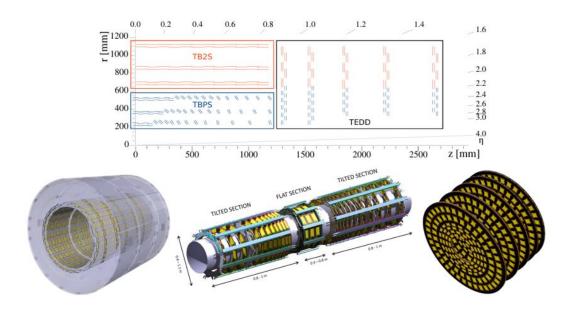


FIG. 1. Layout of the Outer Tracker (top). Model of the TB2S barrel (bottom left). Model of the TBPS (bottom middle). Model of a TEDD unit (bottom right).

Where the new tracking modules differ from those in the current OT is in the use of stubs for triggering. The solenoid magnetic field of CMS allows for discrimination of particles based on transverse momentum (pT). As shown in FIG. 2, high-pT particle hits form stubs which are identified by the front-end electronics and read out to the trigger system. The size window in which two particle hits must lie to identify a stub can be tuned to particular pT thresholds.

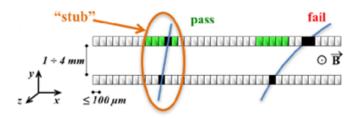


FIG. 2. Stub formation diagram.

B. PS modules

The PS modules, composed of one layer of strip sensors and one layer of pixel sensors sandwiched together, provide higher resolution measurements of particle coordinates parallel to the beam than the 2S, hence their placement closer to the center of the detector. Each module contains two front-end hybrids, hosting 8 SSA (Short Strip ASIC) that read out the hits on the strip sensor. The pixel sensor is read out by 2x8 MPA (Macro Pixel ASIC) chips, which are wire-bonded to the front-end hybrids. This gives a total of 32 read-out chips per module. The structure of the PS module is shown in FIG. 3.

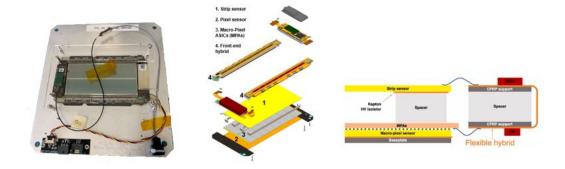


FIG. 3. PS module at Fermilab (left). Exploded view of the PS module (middle). Side-view diagram of the PS module (right).

FIG. 4 illustrates the data flow from the OT to the L1 Trigger, which selects which data to store. Hits from high-pT tracks, which are particularly of interest in physics analysis, are selected and the information is sent to the back-end electronics, enabling tracking at 40 MHz. These tracks, combined with the other sub-detector information, will allow for identifying events interesting enough to be downloaded from the detector for further processing. If this is the case, Level-1 accept signal is sent to the modules and all the hits belonging to that event (triggered data) are downloaded.

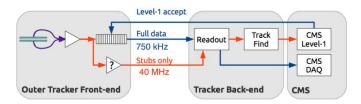


FIG. 4. Outer Tracker data flow.

C. Testing

To ensure each assembled module is functional, a series of tests are carried out to evaluate its performance. Noise, pedestal, and other parameters that ensure effective data communication are measured during burnin tests. Pictures of the burnin system are included in FIG. 5. The test results are stored in ROOT histogram format.



FIG. 5. Burnin box for module testing at Fermilab.

D. POTATO

With the new OT requiring 5,592 PS modules, their assembly and subsequent testing, is distributed over several facilities around the world. To ensure uniform quality control criteria across these facilities, we have developed a software called POTATO, or the Phase-II Outer Tracker Analyzer of Test Outputs, which provides standardized analysis and grading of module test results. As illustrated in FIG. 6, POTATO treats the results in two separate steps: analysis, which extracts relevant information, and grading, which categorizes the module based on its performance. The results of these two steps are stored in XML form and uploaded to a centralized database, along with the test data, to be shared with the collaboration.

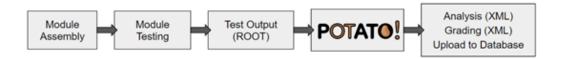


FIG. 6. Flowchart of module assembly and testing process.

The POTATO user interface, shown in FIG. 7, allows the user to select particular test files to analyze and grade. It also provides a method for interfacing with the database, either to upload local files or to download data for modules produced by the collaboration.



FIG. 7. POTATO user interface.

II. ANALYSIS

At the analysis stage, the histograms produced during burnin testing are processed by POTATO to extract relevant quantities. For each variable (e.g., noise), the mean and RMS are computed, and channels with outlying values are identified. These parameters are summarized in the output XML file at the chip, front-end hybrid, and module levels, as in FIG. 8. The current version of POTATO includes completed procedure for analyzing noise, pedestal, and inter-chip communication efficiency histograms.

FIG. 8. Snippet of an example analysis XML (module summary).

A. Noise

A fundamental property of the detector is the noise, which affects the threshold one can apply in operation and therefore the lowest signal detectable. As such, the mean noise and fraction of channels with outlying noise values, computed by the POTATO analyzer, are crucial to evaluating module performance.

B. Pedestal

When an incident particle interacts with the sensor, a signal on top of the baseline voltage (also known as pedestal) is generated. By construction, the pedestal position for every channel is different, and both MPA and SSA have dedicated registers used to compensate for this difference. During the testing, a procedure is carried out to tune these registers in order to equalize the pedestal distribution and therefore set a consistent threshold across all channels. Of particular interest is the identification of channels with outlying pedestal values, which are determined from the computed mean and RMS.

C. Inter-chip communication efficiency

The inter-chip communication efficiency histograms provide information about the efficacy of data communication along the lines used for transmitting stubs and triggered data. From these histograms, the efficiency is extracted for each line as a value between 0 and 1. Failure for a module to properly transmit this information (i.e., the efficiency is far below 1) indicates that it is damaged and likely unusable.

III. GRADING

Once analysis is complete, POTATO assigns a grade to the module based on the analysis results. Grades A, B, C, etc. are given for individual parameters (for example, average noise) as well as an overall module evaluation. The assessment is summarized in a second, grading XML, such as the one in FIG. 9.

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COVERALL>A</PSECTU_CURR_AMP>
CLV_CURR_AMP>FC/TV_CURR_AMP>
CLV_CURR_AMP>FC/TV_CURR_AMP>
CLV_CURR_AMP>FC/TV_CURR_AMP>
CLV_CURR_AMP>FC/TV_CURR_AMP>
CLV_REARAMP>FC/TV_CURR_AMP>
CLV_REARAMP>FC/TV_CURR_AMP>
CLV_REARAMP>FC/TV_CURR_AMP>
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CLV_REARAMP>FC/TV_REARAMP>
CNOISE_NOUT_LOW>A</POISE_NOUT_LOW>
CNOISE_NOUT_LOW>A</POISE_NOUT_LOW>
CNOISE_NOUT_LOW>A</POISE_NOUT_LOW>
CFEHR_OVERALL>A</FEHR_OVERALL>
CFEHR_NOISE_ROUT_LOW>A</FEHR_NOISE_ROUT_LOW>
CFEHR_NOISE_ROUT_LOW>A</FEHR_NOISE_NOUT_LOW>
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CFEHR_NOISE_NOUT_LOWA-C/FEHR_NOISE_NOUT_LOW>
CFEHR_NOISE_NOUT_LOWA-C/FEHR_NOISE_NOUT_LOW>
CFEHR_NOISE_NOUT_LOWA-C/FEHR_NOISE_NOUT_LOW>
CFEHR_NOISE_NOUT_LOWA-C/FEHR_NOISE_NOUT_LOW>
CFEHR_NOISE_NOUT_LOTAL>
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CFEHR_NOISE_NOUT_LOTAL>
CFEHR_NOISE_NOUT_LOWA-C/FEHR_NOISE_NOUT_LOTAL>
CFEHR_NOISE_NOUT_LOTAL>
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CFEHR_NOISE_NOUT_LOTAL>
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CFEHR_NOISE_NOUT_LOTAL>
CFEHR_NOISE_NOUT_LOWA-C/FENSTAL_NOUSE_NOUT_TOTAL>
CFENSTAL_AWS-AC/PEDESTAL_AWS-
CPEDESTAL_AWS-AC/PEDESTAL_AWS-
CPEDESTAL_NOUT_LOWA-C/PEDESTAL_NOUT_LOWS-
CFEDESTAL_NOUT_LOWA-C/FENSTAL_NOUT_LOWS-
CFEHR_PEDESTAL_NOUT_LOWA-C/PEDESTAL_NOUT_LOWS-
CFEHR_PEDESTAL_NOUT_LOWA-C/PEDESTAL_NOUT_LOWS-
CFEHR_PEDESTAL_NOUT_LOWA-C/FEHR_PEDESTAL_NOUT_LOWS-
CFEHR_PEDESTAL_NOUT_LOWA-C/FEHR_PEDESTAL
```

FIG. 9. Example grading XML.

The grading criteria is based on a series of predetermined cuts. Currently, the cuts in place in the current version of POTATO are preliminary. As more data becomes available and the collaboration discusses the ideal grading scheme, these cuts will be updated with iterative versions of POTATO. Ultimately, the grading results will assist in deciding which modules meet the selection criteria to be included in the Phase-II CMS detector.

A. Noise

The SSAs and MPAs require distinct cuts, as the strips, having a larger capacitance, typically have correspondingly greater noise values. Based on the available test data, we have applied some preliminary cuts on the noise average, given in FIG. 10. Within this currently implemented framework, values that fall within the accepted window receive a grade A, while others are given a grade C. Low noise results might indicate an issue with the testing procedure and thus are given an unfavorable grade.

Grade	SSA Cuts	MPA Cuts
Α	3 < Noise Average < 5	2 < Noise Average < 4
С	Noise Average < 3 or Noise Average > 5	Noise Average < 2 or Noise Average > 4

FIG. 10. Preliminary grading cuts for noise average.

These cuts are also used to identify outlying channels. Channels with particularly low noise values are indicative of disconnected wire-bonds, while high values correspond to noisy channels. Those with average noise values falling outside the selected window are labelled as outliers, and additional cuts are in place to favor modules with minimal outliers. In the current version of POTATO, having less than 1% outlying channels at the hybrid level constitutes a grade A, with additional, more lenient cuts defining the window for a moderately acceptable grade B and otherwise a grade C.

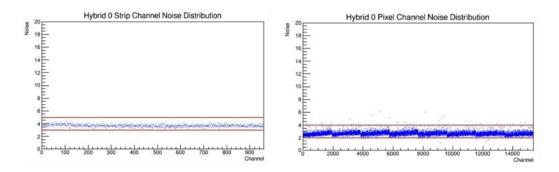


FIG. 11. Channel noise distribution histograms at hybrid-level for SSAs (left) and MPAs (right).

B. Pedestal

Similar constraints are applied to identify channels with outlying pedestal, as summarized in FIG. 12. After computing the pedestal mean and RMS, outliers are (currently) identified as channels with values $\pm 3\sigma$ from the average. Modules with exceptionally many outliers, corresponding to those having long tails in the distribution, are given lower grades.

Grade	Cuts
A	Total fraction of pedestal outliers < 2%
В	2% < Total fraction of pedestal outliers < 4%
С	Total fraction of pedestal outliers > 4%

FIG. 12. Preliminary grading cuts for fraction of pedestal outliers.

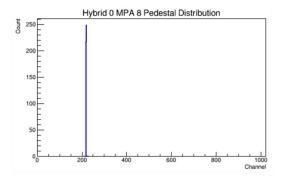


FIG. 13. Channel pedestal distribution at chip-level.

C. Inter-chip communication efficiency

For the read-out lines, it is expected that the efficiency should be very near 100% -otherwise, data communication would be compromised. As such, strict cuts are applied restricting grade A to modules with efficiency values near 1 for all read-out lines. Having any lines with values of 0 automatically assigns a grade F to the module, indicating that it is unusable.

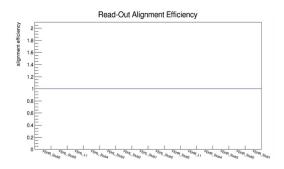


FIG. 14. Inter-chip communication efficiency histogram.

IV. CONCLUSIONS

At this time, the first version of POTATO is complete, including procedure for analyzing and grading modules based on noise, pedestal, and inter-chip communication efficiency. I have, over the course of the summer, contributed to the development of these analysis and grading scripts. Additionally, I have presented updates to the collaboration on this progress and created documentation of the current capabilities of POTATO, initiating the discussion of optimal grading methodology. This documentation will be updated in the future as more modules and test data become available and adjustment of grading criteria continues.

V. FUTURE WORK

We are continuing to update POTATO by adding more variables (i.e., including analysis of results from additional tests) with each new version. We are also currently working on implementing a method in the POTATO user interface which will allow for downloading and plotting data from the centralized database of module test results. Ultimately, POTATO will serve as the means for evaluating which modules are of the highest quality and thus should be selected for use in the experiment.

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