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FASTBUS IMPLEMENTATION REVIEW*

J. A. Appel and W. K. Dawson†

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†TRIUMF, University of British Columbia, Vancouver, B.C. V6T 2A3

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J. A. Appel
Fermi National Accelerator Laboratory*
P.O. Box 500, Batavia, Illinois 60510

W. K. Dawson
TRIUMF**
University of British Columbia
Vancouver, B.C. V6T 2A3

Abstract

For the last few years, enough has been known about the properties and capabilities of FASTBUS for it to be incorporated into the design of some experiments. As a result, despite the newness of the specification, a number of systems using FASTBUS are well advanced and a few even completed. We discuss some of these systems from several viewpoints, including why FASTBUS was chosen, how painful was the implementation and the role played by the software. FASTBUS systems in the United States, Europe and Japan are included in this review.

Introduction

In June of 1977, the Advanced Systems Study Group (ASSG) of the U.S. NIM Committee issued its report "Future Databus Requirements for Laboratory High-Speed Data Acquisition Systems."[1] In the report, they emphasized the need for

(1) ten times greater speed than CAMAC,

(2) sparse data scan,

(3) segmentable and parallel processing, and

(4) a bus architecture allowing a variety of uses.

They also emphasized error detection, innovative debugging and checkout ideas, power distribution and the importance of a uniformity and simplicity of design to aid the important software efforts.

The FASTBUS hardware specification[2] now in the hands of the U.S. Department of Energy and the implementations discussed in this paper are the result of the very significant effort which has gone on since the ASSG report and the use of these new ideas. In this review, we investigate the existing applications as a guide to the near-term and not-so-near-term usefulness of the FASTBUS standard.

The implementations (all using emitter coupled logic hardware) began with a CP invariance experiment[3] at Brookhaven (BNL-E735) which used an early version of the developing FASTBUS standard. It was followed by a charm experiment[4] (Fermilab-E400) and a CERN Muon experiment[5] (EMC) which both used a later version of the standard. These three experiments all used single FASTBUS segments. The first multi-segment implementation was built by the same Brookhaven group[6] for a new experiment (BNL-E749), but using the earliest FASTBUS version and modules from the first experiment.

A number of additional implementations are just coming into being. These include a control system for the cryogenic elements of the Mark II detector[7] at SLAC, a medical imaging application[8] and a front-end data processing system[9] by LeCroy Research Systems. All of these new implementations, as well as most of the earlier ones, will use the standard as delivered to the Department of Energy for future efforts. Commitments to FASTBUS-based data acquisition and control systems have been made by a number of experiments (e.g., CDF at Fermilab[10] and TOPAZ at KEK) and the control system for the new accelerator at KEK in Japan[11]. Other groups are also planning FASTBUS systems, but are not sufficiently advanced in their effort for inclusion here.[12]

Choice of FASTBUS

Some of the implementations listed above were motivated by the desire to gain experience with the new standard. However, some were motivated by data acquisition problems for which the available alternatives were less adequate than FASTBUS. Table I lists the earliest implementations and indicates the primary motivating factors for using FASTBUS. The variety of features is evident.

While gaining experience is a strong motivation for first uses, there is also a recognition of the appropriateness of FASTBUS for future growth in experiments where data acquisition needs are expected to expand around a core apparatus. Although the first implementations have been intentionally simple, they exercise fundamental building blocks (e.g., the protocol, interfaces and software facilities) which are required for all systems. The intention has been to solve more complex data acquisition and control problems later using the methods and tools developed for the simpler implementation.

Used/Tested Features

In any system as new and extensive as FASTBUS, it is useful to understand which features have already been used and tested in

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TABLE I

Choice of FASTBUS

Implementation	Brief Description	Major Motivations
BNL-E735	Data Buffer and Trigger Processor	Multiple Masters, Speed
Fermilab-E400	Event Buffering	Electrical-Mechanical System for 1Mby Memory
CERN-EMC	Small Angle Interaction Trigger Processor	Experience, Multiple Masters
BNL-E749	Data Buffer and Trigger Processor	Multiple Masters, Speed
SLAC-MkII	Control of Cryogenic System	Experience
Medical Scanner	Scan Data Buffering and Display	Bandwidth
LeCroy System 1800	ADC, TDC and CCD Front-End Modules	Experience, Front Panel Size, Cooling, Aux. Connect., Power
Fermilab-CDF	Data Acquisition	Segmentability, Parallelism

TABLE II

Use of FASTBUS Features

(Representative Numbers Only)

	BNL E735	Fermilab E400	CERN EMC	BNL E749	SLAC MkII	Medical Scanner	Fermilab CDF	U. of Ill. SI Tests[13]
Arbitration								
#Masters	4	1	1	7	2	3	~100	7
#Modules	16	6→10	10	32	14	5	~400	10
Module-Module Transfer	Yes	No	Yes	Yes	No	Yes	Yes	No
Logical Addressing	Exclusively	Yes	None	Exclusively	Yes	Yes	Yes	Yes
#Segments	1	1	1	5	2	1	~50	5
Max. Bandwidth	Single word only	>250Kby/sec		Single Word only	8Mby/sec	160 Mby/sec	-	4 Mby/sec
Avg. bytes/sec in spill	~50 Kby/sec	1 Mby/sec		~50 Kby/sec	-	16Mby/sec	20Mby/sec	
Address Size Used	4.3K	500K→4.2M		2.3K	-		-	
Size of Data Buffer	8Kby	1Mby→8Mby		8Kby	-	4Mby	-	
Max. Power/Card	80W	50W		80W	30W		75W	75W
Standard Software Used	No	Yes	Yes	No	Yes	Yes	Yes	Yes
Std. Routines	-	Yes	Yes	-	Yes	Yes	Yes	Yes
FDL	-	Yes	No	-	-	No	Yes	Yes
Card Size								
Old	Yes	Originally	Yes	Yes	-	-	-	Yes
Final	-	Yes, now	-	-	Yes	Yes	Yes	-

actual data acquisition situations (Table II). A large range of the FASTBUS features have been used and a number of patterns have begun to emerge.

First, once a commitment has been made to FASTBUS for one or more specific reasons, additional requirements become easy to satisfy. Second, elements used in a single segment system are directly reusable in multiple segments. This has been demonstrated in the Brookhaven experiments and is also part of the plan for the medical scanning application. Multiple scanning systems can be added as additional segments (which operate in parallel) in a straightforward manner. Thirdly, the large address space available in FASTBUS has been among the first features to be widely used. The increasingly large number of channels in experiments and reduction in memory costs has led to an increased use of large data buffers. It parallels a similar development in modern computer architecture. However, in this case, use of large memories is driven by the need for multiple levels of triggering to filter interesting events in experiments. This is just as anticipated in the ASSG report.

In order to make best use of this event buffering near the front end of a FASTBUS system, some of the experiments have implemented multiple masters (even on single segments) to process the stored events.

It is natural that none of the implementations use all the available features of FASTBUS. It was never intended or expected that this would happen. Among the features which have yet to be used are service requests, daisy chain serial lines, serial network ports and parity.

Lessons So Far

A number of lessons have been identified by implementers of the first FASTBUS systems. Physical modularity continues to be a useful feature of the new system. It was suggested that this modularity be extended to such system components as power and cooling. In fact, the first commercially-available power supplies and cooling units follow this recommendation. The power supply chasis can be fitted with any of a variety of modules with different current capabilities.

Contention resolution has been found a somewhat more difficult problem than originally expected in systems containing multiple masters acting asynchronously and concurrently. It has become clear that system organization should be arranged so as to simplify communication among the various parts. Regularity of structure and separation of functions can help remove or minimize many system and network related problems. In such organizations, network and parallel processing problems do not have to be confronted in all their generality.

A number of specific difficulties have been encountered. For example, the transfer of 32-bit FASTBUS words into a 16-bit computer may be complicated by the receipt of an interrupt between the two halves of the FASTBUS word transfer. One group found it necessary to preclude interrupts in the middle of 32-bit transfers. Similarly, transfers of very long blocks of data and slow arbitration in complicated systems may result in timeouts (e.g., 10 microseconds on PDP-11's) which may require rather complicated error handling by all the masters in the system.

One group with a single vectorized interrupt recommends the use of two or more separate hardware interrupts. Doing so may allow separation of unrelated interrupt software. This, in turn, may allow the use of non-reentrant code as well as organizational simplification.

During debugging stages, one of the most difficult things is knowing the state on all segments in multi-segment systems. Multiple segments, even with simple activity on each segment, have been found to be significantly harder to understand than single segments with multiple masters.

In order to avoid overloading a host or other processor, it is found most beneficial to do the gathering and formatting of data in the FASTBUS environment. This allows a single processor interrupt to suffice for a potentially large amount of information (spanning many detectors in an apparatus or even multiple events).

A distinction is evident between the most front-end modules and those which process the data from them. The distinction goes beyond that between master and slave modules. It involves the motivations of simplicity and economy. The simplest modules which may be the greatest in number typically have only geographic addressing.

In both cases, the software selection of features has been found to be an aid in automatic testing of modules. In many modules of an earlier era, the use of jumper options and manual switches complicated testing by both vendors and end users.

The major shortcoming identified by the growing FASTBUS community is a lack of basic building blocks which can be purchased "off the shelf" for FASTBUS systems. Some progress in this area is evident during the past year (crates, power supplies, cooling chassies and kluge cards). A significant number of products have been announced and the next year it is expected to see much greater availability of such important units as computer interfaces, segment interconnects, buffer memories and front-end modules. CERN's DD Division is expecting to deliver $_{14}25$ Starter Kits to user groups this summer.

So far, all implementations of FASTBUS have been successful in achieving the functions and goals intended. The Brookhaven and Fermilab groups have already expanded the scope of their original implementations. It is clear that all of the early groups to use FASTBUS have been capable and experienced groups. As the amount and variety of FASTBUS

components expands and the use of standardized software expands, it is expected that groups with less expertise will also be able to make successful use of the FASTBUS standard. The most apparent direction for the next FASTBUS implementations is for front-end data buffering and multiple level triggering. In a sense, this is a return to the data acquisition environment before the rise of low luminousity experiments at colliding beam machines.

Acknowledgements

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