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# OPERATING CHARACTERISTICS OF LECROY 2280/2285 ADC SYSTEM*

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## ABSTRACT

The operating characteristics of the LeCroy Research Systems current version 2280/2285 ADC System are reported. This system is currently being purchased for use in experiments at Fermilab and elsewhere. Earlier prototype systems are being upgraded to this standard.

Much of what has been learned during the development of these modules has been relevant to other components (e.g., the 2282 module) of the 2280 family. However, no testing of these other units has been carried out at Fermilab to date.

## INTRODUCTION

The 2280 ADC System is a flexible, self calibrating, data sparsifying, high-sensitivity, linear, charge integrating ADC system. As such, it is a complex device with many

* This is an updated version of FN321 (Fermilab Physics Note, December 26, 1979, unpublished). The older note describes earlier, prototype versions. Following preparation of this note, a new version hybrid (QD102) was received. We have also learned that modifications are being made to the 2280 system processor. Based on the first few production boards with QD102's, the response of the new units is comparable, though slightly inferior, to the QD101E response. None of the typical features tested appears more than 30% worse than the same feature for the QD101E. The plateau of Figure 1 may be slightly better for QD102 hybrids.

characteristics to test. The present tests are not all-encompassing. On the other hand, they relate to some of the more fundamental responses of the system in simulated experimental situations. The results relate to the following characteristics:

1. Effective gate.
2. Linearity of response to front panel inputs.
3. Linearity of test pulse response and relationship to front panel response.
4. Rate dependencies of pedestal and gain when the fast clear circuitry is used.
5. Crosstalk from channel to channel.
6. Noise rejection capabilities.
7. Gain and pedestal dependencies.

These topics are treated one at a time in the following sections. In tests (as the user must insure during operation), no use is made during digitization time of the CAMAC dataway in the crate.

## EQUIPMENT

The 2280 ADC systems tested were comprised of a system processor module (Model 2280) and individual 24 channel ADC modules (Model 2285A), all housed in a single standard CAMAC crate. The ADC modules make use of hybrid circuits (Model QD101E).

A list of modifications to the originally delivered equipment (where known to Fermilab) is given in an appendix. Many of these modifications have been adopted by LeCroy in the versions leading to the current model. However, we list all the modifications since they may be of interest to other users, especially in reference to other units in this line.

Test results are for fully modified modules only.

The tests were performed using standard NIM modules to generate gate and clear pulses and commercially available programmable digital delay generators and programmable DAC's to control gain and test level references. The various pieces of equipment were tied to a CROMEMCO microprocessor-based system which allowed computer control, immediate information turnaround and hardcopy outputs. All of this equipment was set up in the Instrumentation Evaluation Group at Fermilab.

## EFFECTIVE GATES

Using an external pulser, it was possible to vary the relative times of the input and gate. Ideally, gate level transitions should be instantaneous. The effect should be to totally integrate any portion of the input signal enveloped by the gate and to ignore any portion that falls outside of the gate. To the extent that the transition is not instantaneous, the gating efficiency at a given relative time should be independent of input amplitude. Figure 1a shows plots of the integrated signal digitization for a 6 nsec wide logic signal

applied at various times with respect to the gate. Figure 1b shows the same for an input pulse with 4 nsec rise time and 35 nsec fall time. Five features are of interest. First, comparison of the various parts of Figure 1 show a significant dependence on the input pulse rise time. Although the peculiar effect of fast rise time pulses (when they are early with respect to the gate) is not likely to be a severe problem for most present-day applications, it may be noted that the effect does not seem to be fundamental. Some samples of earlier versions do not exhibit this effect. Second, the turn-on time for the gate circuit is about 8 nsec, while the turn-off time is 4.5 nsec. Channel-to-channel variation of the effective gate width is about 2 nsec. Third, the effective gate turn-on time varies from channel to channel by up to 3 nsec relative to synchronous front panel inputs. Fourth, there is a 5% variation of gain across the 43 nsec plateau (full acceptance) for a 100 nsec applied gate. Finally, the non-linearity of the ADC response during the turn-on of the gate circuit has not changed substantially from earlier versions. However, it has moved earlier with respect to the applied gate. Figure 2 shows the size of the effect. The gain is a function of the applied charge or voltage!

## LINEARITY OF RESPONSE TO FRONT END INPUTS

One of the most impressive features of these ADC modules is the linearity of response in the middle region of the gate period over a very wide dynamic range. Table I contains the results of fits to the response to charge applied to the input for a variety of gains and full scale values. All tests were performed using an applied gate of 100 nsec and a charge pulse of 2 nsec rise time and 22 nsec FWHM. Special care was taken to insure that the pulse started well after the gate became effective.

The results are shown in Figure 3 where the deviations from the Response = (gain * charge + pedestal) fits for 24 channels in one module are shown. The rms deviation of the response to a linear fit was typically less than a count. Individual values are listed in Table I. The gains used in obtaining Figure 3a and 3b agreed within 1% for all channels. Thus, one could use the fit for the high charge levels and still agree within 1% for the low charge digitizations and vice versa (as in muon calibrations of calorimeters).

## TEST PULSE RESPONSE

Because of the charging time of the test pulse circuit (10 microseconds) and the amount of charge required for a large system, it is inappropriate to enable the test pulse circuit during normal data taking for many experiments. In this case, the pedestal value (response for no input charge) is different

between normal data and test pulse enabled data. However, the test pulse measured gain and linearity is found to be representative of the front panel response for these features. Table II shows the response to test pulse operation akin to the results of Table I with a front panel input to the same channel. The final column gives the ratio of linear fit coefficients in the two tests. Using only one normalization point, this ratio is 1, typicaly within 0.5%. This demonstrates how well the test pulse data represents the front panel response.

The earlier timing problem for some channels' test pulse has been alleviated by the faster gate turn-on of the current version.

## RATE DEPENDENCES

Two separate tests of rate effects have been conducted. One, referred to as the "pump-up" test, imposed repeated alternate gates and fast clears until a final gate was followed by readout without a fast clear. The pedestal was monitored as a function of the number of gate-clears before a readout. The pulses received by the processor are indicated in Figure 4a. The second test, referred to as the "simple rate" test, systematically changed the time between a readout and the previous clear. The pulses received by the processor are indicated in Figure 4b. In this test, two gate signals are received for each readout, a first with a fast clear quickly following and then a second after a predetermined time for

readout. In both tests, the time required for a readout was long and small variations of its length were ignored. Tests were also performed with 400pC of charge injected during the first gate. No serious degradation of performance in this "simple rate" test resulted.

The results of these tests (Figure 5) indicate minimal rate dependences, each on the order of less than .05 picocoulomb. One channel is outside this range. The typical channel's deviation is less than 2 counts for the most sensitive gain settings (30 fC/count) and unobserved at less sensitive settings.

Using the external charge pulser and putting a known charge into the ADC channel during the last gate of Figure 4a, it was possible to measure the sensitivity of the module under differing event rates. No reproducible gain changes of more than 1% were observed as a function of gating rate.

## CROSSTALK

The feedthrough of signal from one channel to another on the same board is about 60 db. That is, channels which are adjacent or share the same test pulser input cable have about 0.2% feedthrough of signals. Other channels are typically a factor of two or more better isolated.

## NOISE REJECTION CAPABILITIES

The inputs of each channel are quasidifferential. In addition, the layout on the printed circuit board is such that the chassis ground is isolated by a 1K ohm resistor per board and 0.022 pfarad capacitors per channel. These features make suppression of ground loops a function of other system elements. A series of tests were performed to determine the effects of positive and negative voltages up to 0.5 volts d.c. and 0.2 volts peak to peak 60 and 120 herz applied between the input signal return and ground. No broadening of the distribution of pedestal values for a series of readings was observed. However, the average pedestal value does depend on these levels. In this context, it should be observed that the rms width of a typical pedestal distribution is about 15 femtocoulombs with no cables plugged into the front. In two setups in running experiments, the rms pedestal width has increased to about 40 femtocoulombs. Of course, both experiments have required special care (using quite different techniques) to achieve these values. One low rate experiment uses a.c. coupling and shorts out the 1K ohm resistor on each board. The other uses d.c. coupling and no short.

## GAIN AND PEDESTAL DEPENDENCIES

The gain of the ADC modules can be controlled by using an external reference rather than the internal one. The gain and pedestal dependence of a typical channel are shown as a function of this reference for a 100 nsec gate in Figure 6. This data is for a WAIT monostable of 6 usec as supplied with the unit. The pedestal dependence on gate width is shown for another channel in Figure 7. Increasing the WAIT time (before digital conversion) can be used to reduce apparent pedestal values. In this new version, the "pump up" effect is no longer significantly worsened by this procedure.

## ACKNOWLEDGEMENT

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TABLE I

RESPONSE TO FRONT PANEL INPUT

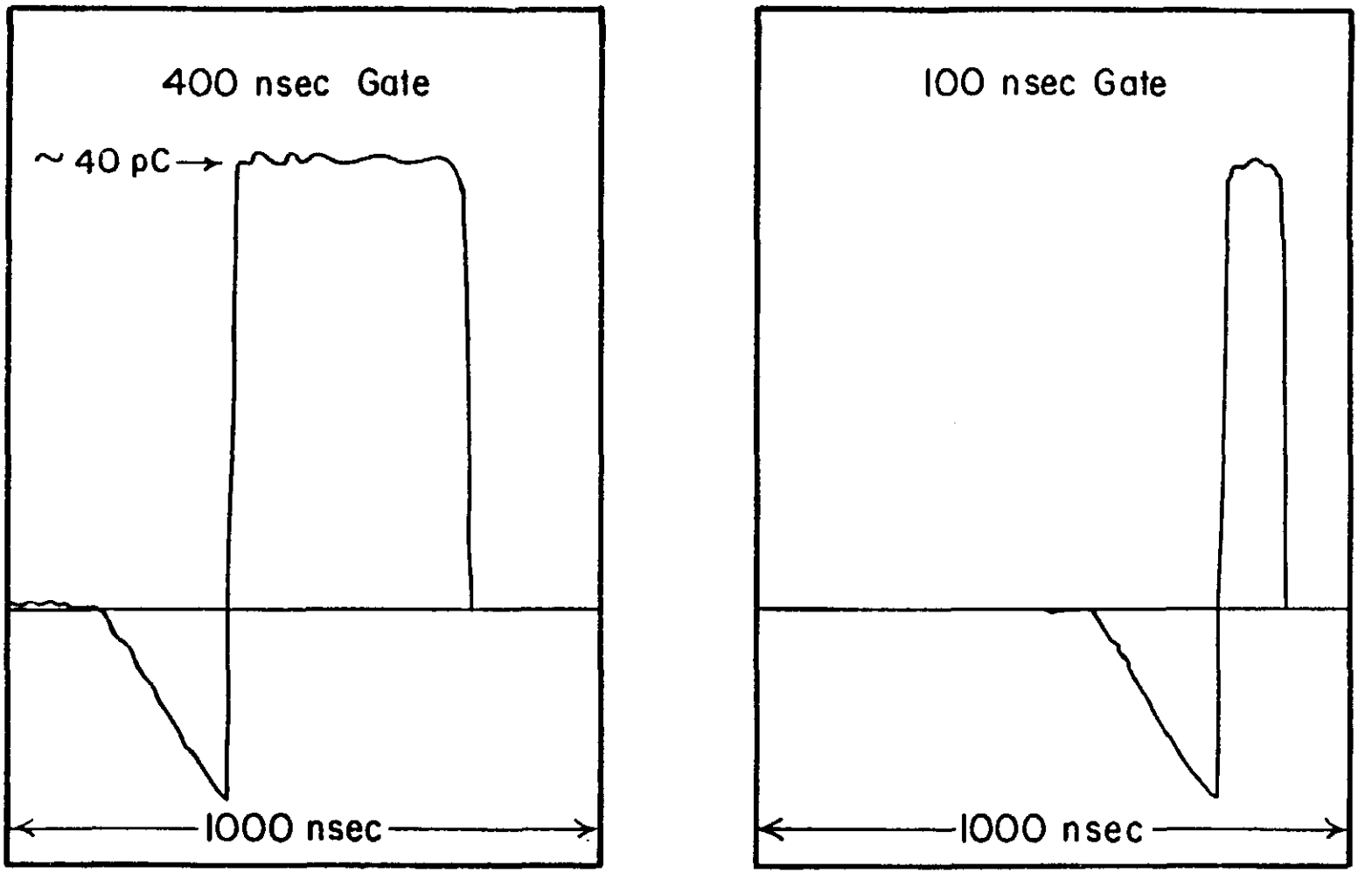
| Gain Reference (Volts) | Approximate Maximum Charge Used In Fit (pC) | Pedestal (Counts) | Gain, m Response=mQ (Counts/pC) | Avg. rms Deviation from Fit (counts) |
|---|---|---|---|---|
| 1.0 | 4 | 2897 | 61.8 | .4 |
| | 8 | 2897 | 61.9 | .5 |
| 2.0 | 4 | 1390 | 32.0 | .8 |
| | 8 | 1382 | 32.0 | .3 |
| | 20 | 1390 | 31.9 | .4 |
| | 40 | 1391 | 32.0 | 1.0 |
| | 80 | 1389 | 32.1 | 1.9 |
| 4.0 | 4 | 656 | 16.2 | .7 |
| | 20 | 653 | 16.6 | .8 |
| | 40 | 656 | 16.6 | 1.3 |
| | 200 | 656 | 16.7 | 2.2 |
| 8.0 | 4 | 285 | 8.9 | .3 |
| | 20 | 285 | 8.8 | .3 |
| | 40 | 285 | 8.8 | .4 |
| | 200 | 286 | 8.8 | .6 |
| | 400 | 286 | 8.8 | 2.6 |

TABLE II

RESPONSE TO INTERNAL TEST PULSER

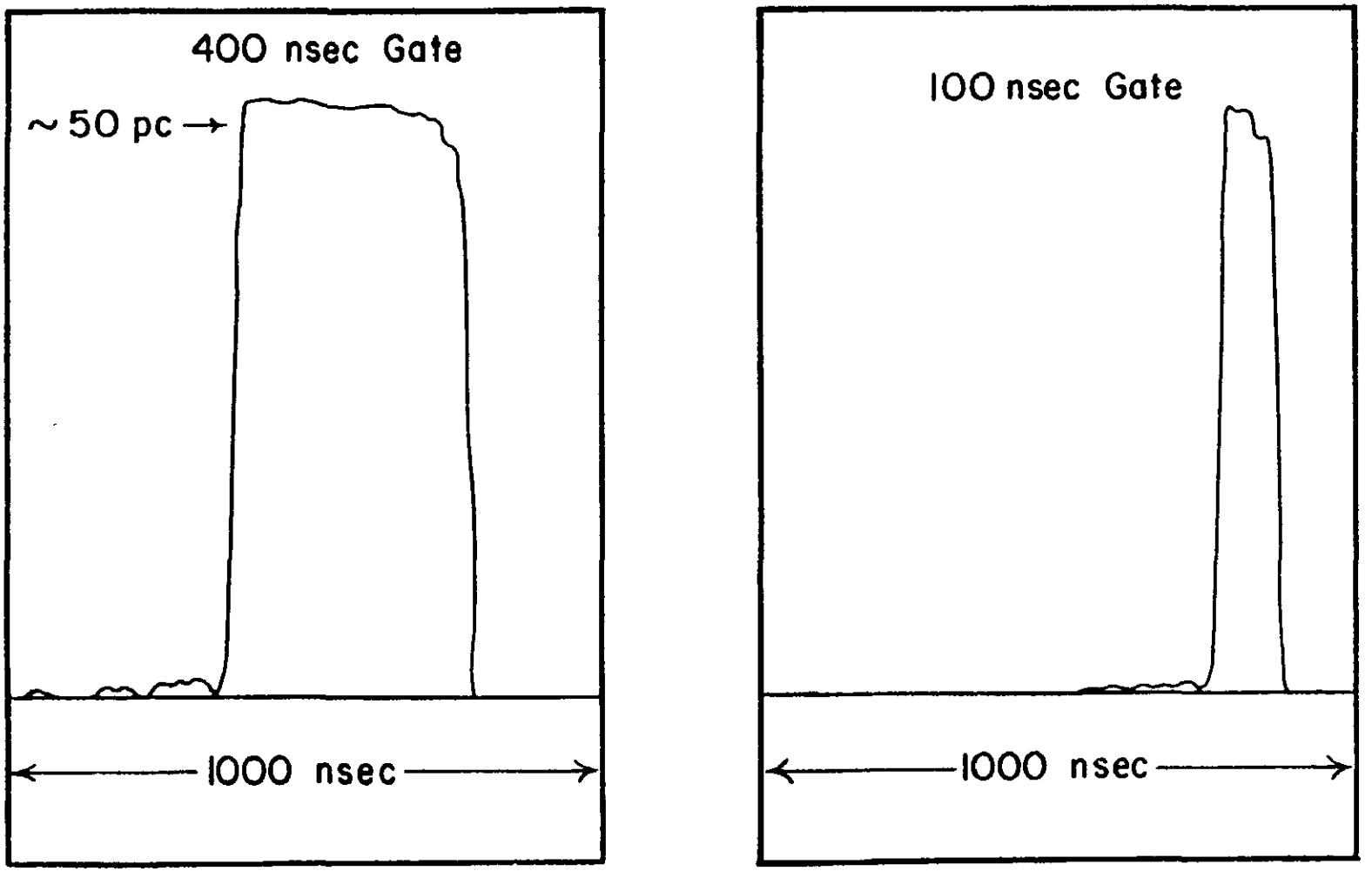
| Gain Reference (Volts) | Approximate Maximum Charge Used In Fit (pC) | Pedestal (Counts) | Gain, m Response=mQ (Counts/pC)** | Avg rms Deviation From Fit (Counts) | $\frac{m_{Internal}}{m_{Front\ P}}$ |
|---|---|---|---|---|---|
| 1.0 | 4 | 2996 | 62.3 | .4 | 1.007 |
| | 8 | 2998 | 62.1 | .4 | 1.004 |
| 2.0 | 4 | 1435 | 31.9 | .3 | .998 |
| | 8 | 1436 | 31.8 | .3 | .995 |
| | 20 | 1434 | 31.9 | .3 | 1.000 |
| | 40 | 1435 | 32.0 | .6 | 1.001 |
| | 80 | 1435 | 32.1 | 1.7 | 1.000 |
| 4.0 | 4 | 680 | 16.5 | .2 | 1.015 |
| | 20 | 680 | 16.6 | .2 | .996 |
| | 40 | 680 | 16.6 | .5 | 1.000 |
| | 200 | 680 | 16.7* | 2.3 | 1.000* |
| 8.0 | 4 | 300 | 8.7 | .2 | .983 |
| | 20 | 299 | 8.7 | .2 | .993 |
| | 40 | 299 | 8.7 | .2 | .996 |
| | 200 | 300 | 8.8 | 1.0 | 1.000 |
| | 400 | 300 | 8.8 | 1.2 | .999 |

**Normalized at * to agree with Table I.



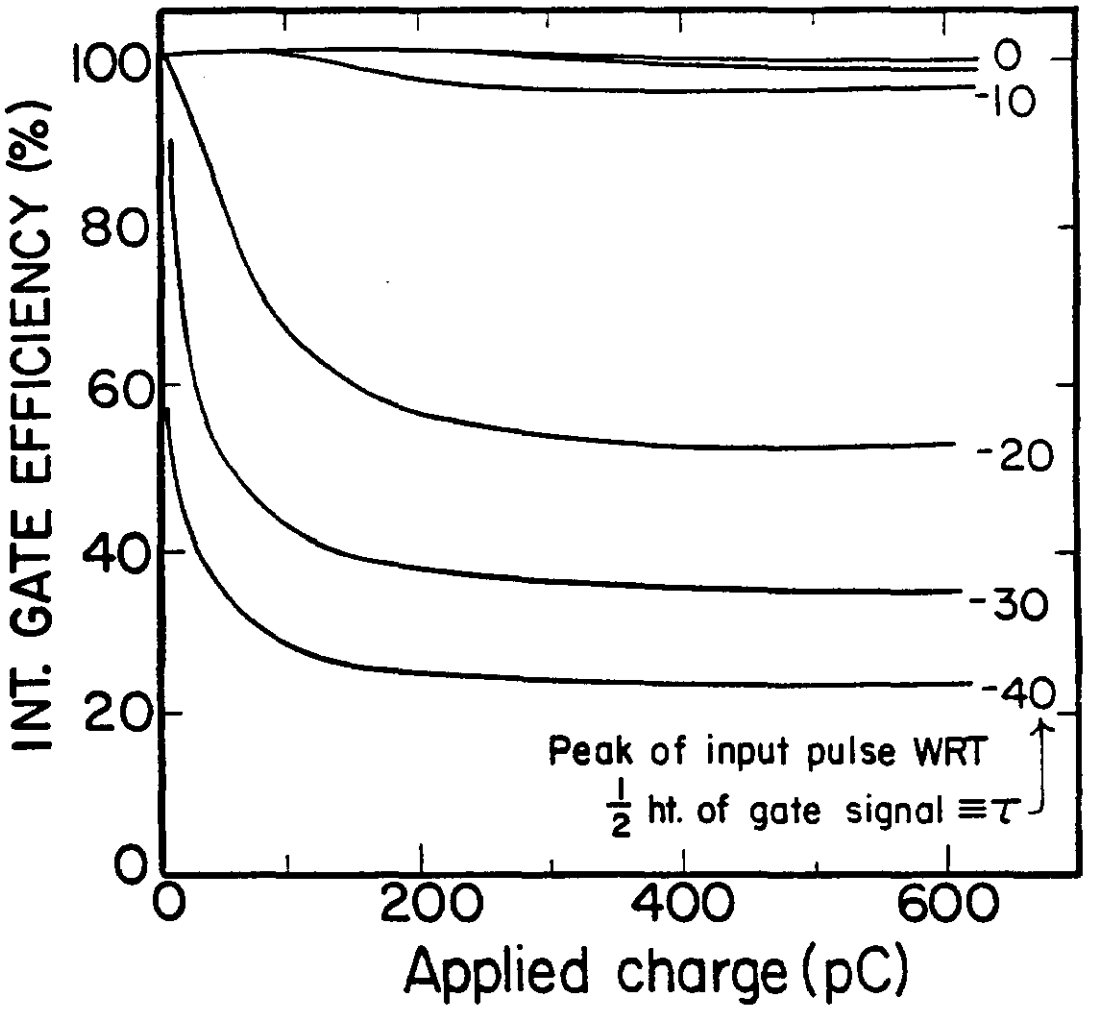

MOVING LOGIC SIGNAL THROUGH GATE

Fig. 1a




MOVING SLOWER PULSE THROUGH GATE

Fig. 1b


INT. GATE EFFICIENCY (%)
100
80
60
40
20
0
0
200
400
600
Applied charge (pC)
0
-10
-20
-30
-40
Peak of input pulse WRT
½ ht. of gate signal ≡τ

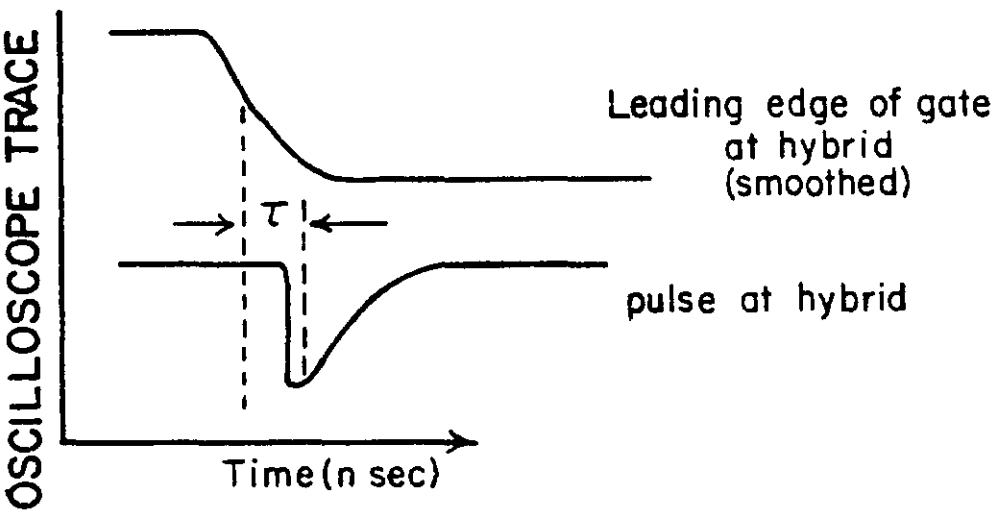
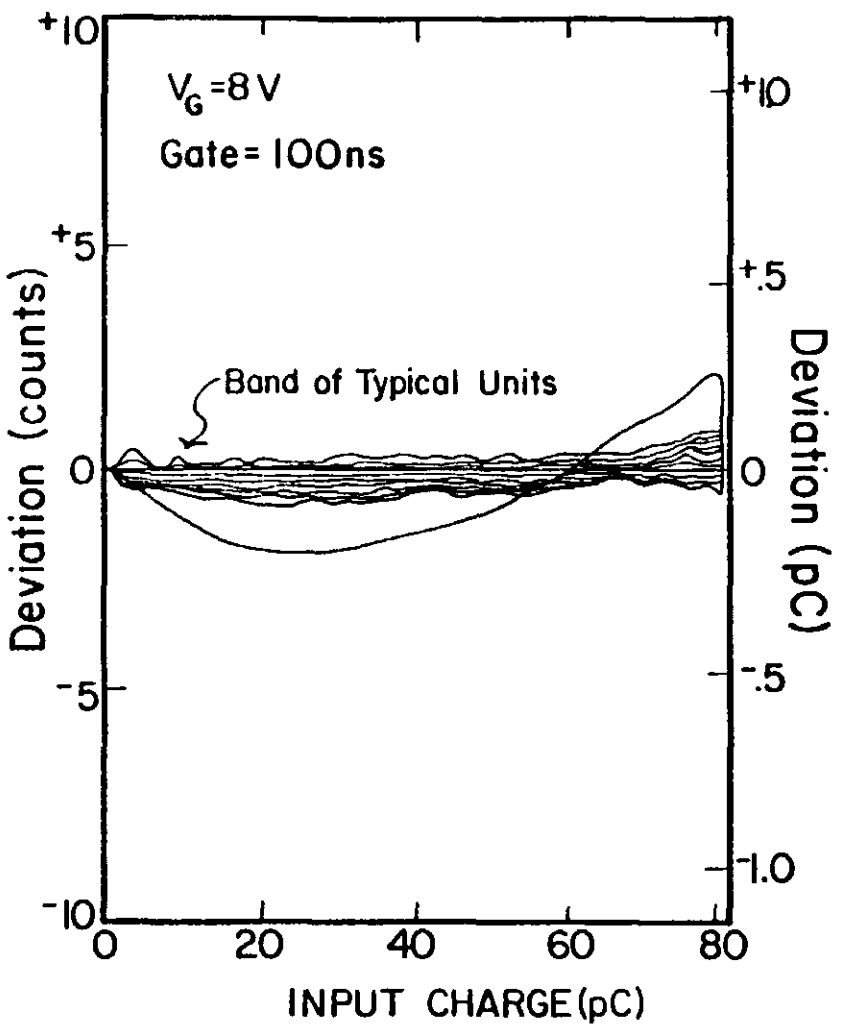
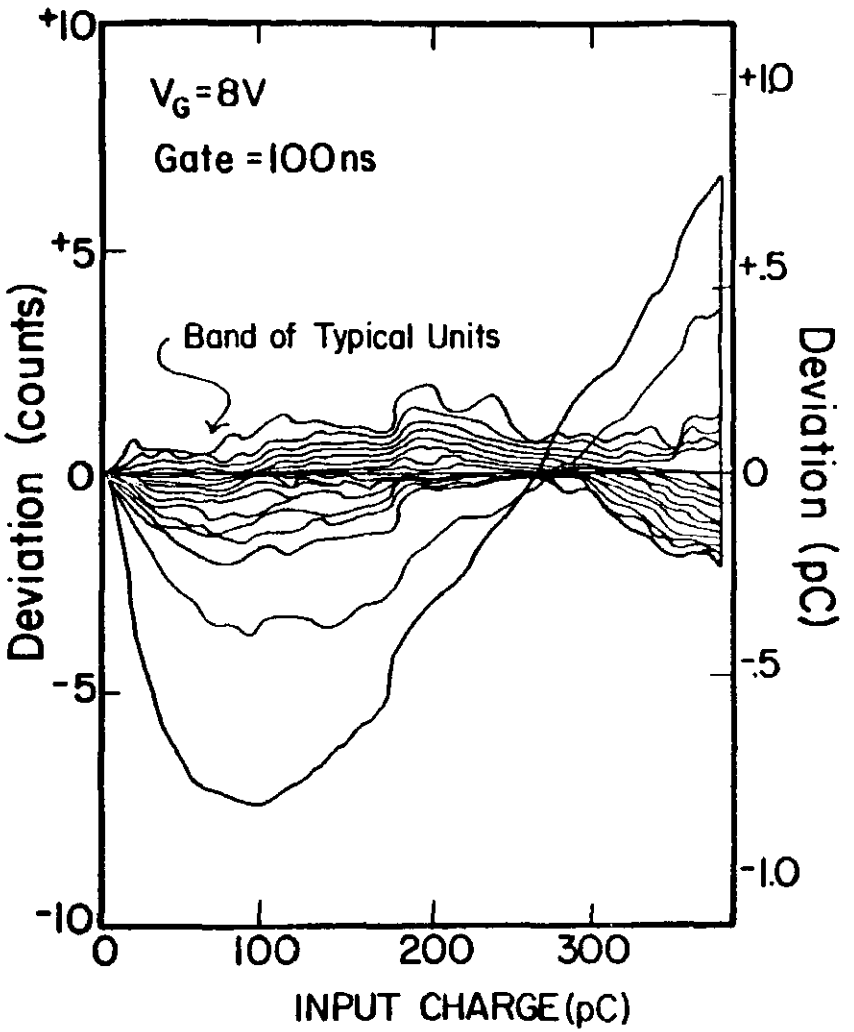

OSCILLOSCOPE TRACE
Leading edge of gate
at hybrid
(smoothed)
τ
pulse at hybrid
Time (n sec)

Fig. 2

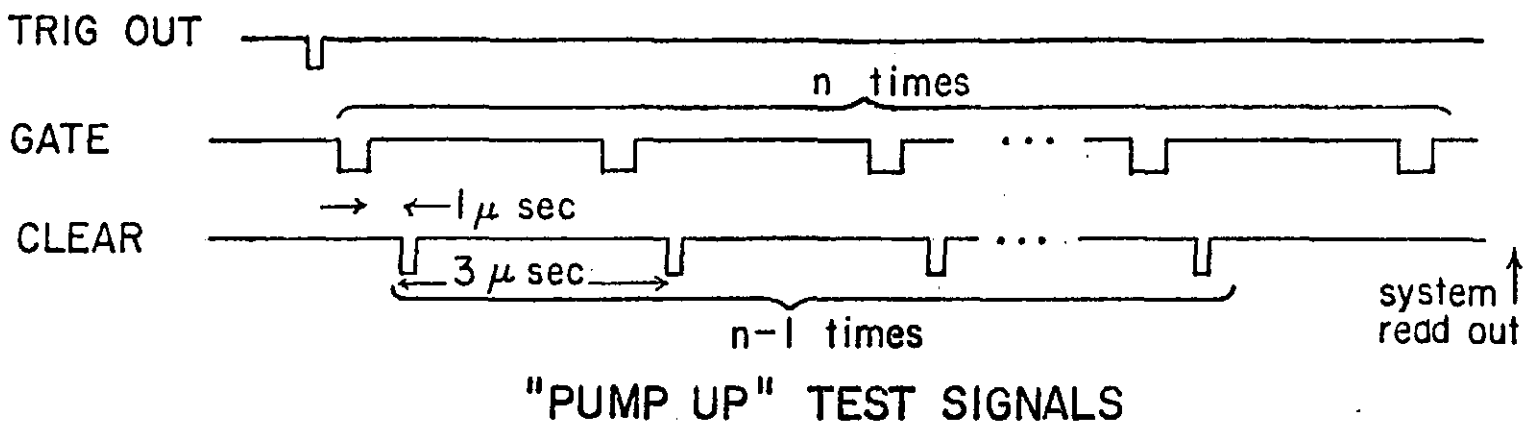



DEVIATION FROM LINEAR FIT

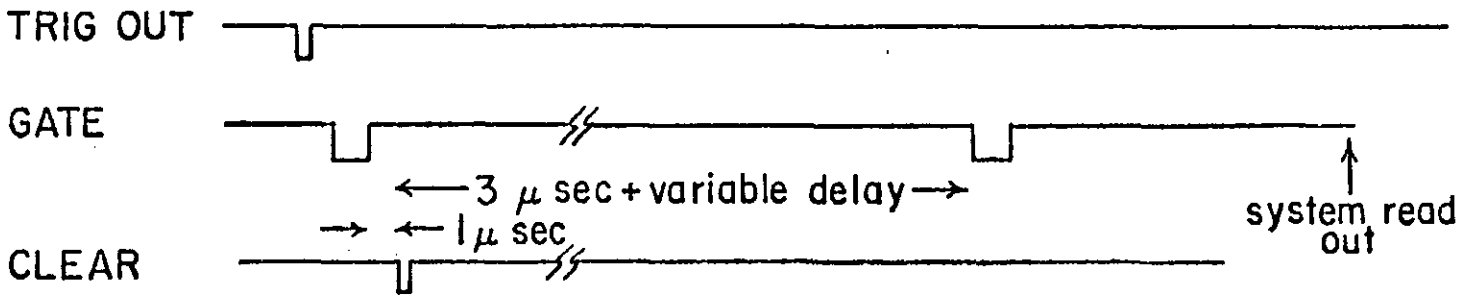
Fig. 3a

Fig. 3b



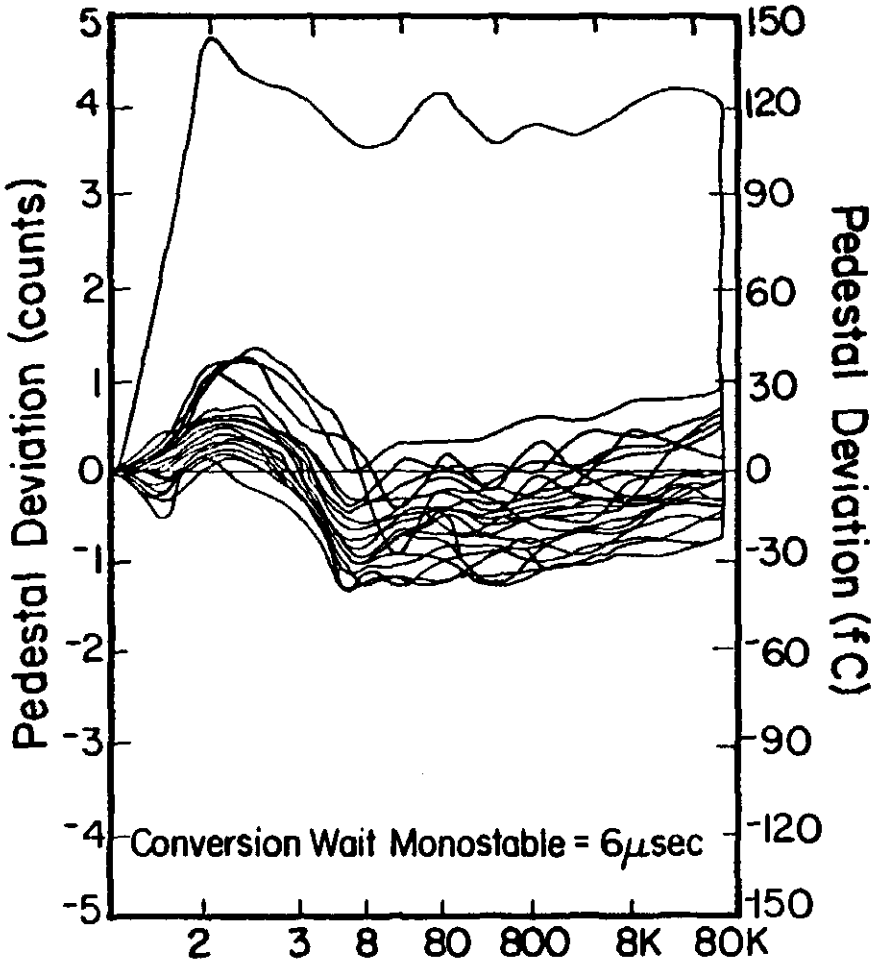

"PUMP UP" TEST SIGNALS

Fig. 4a



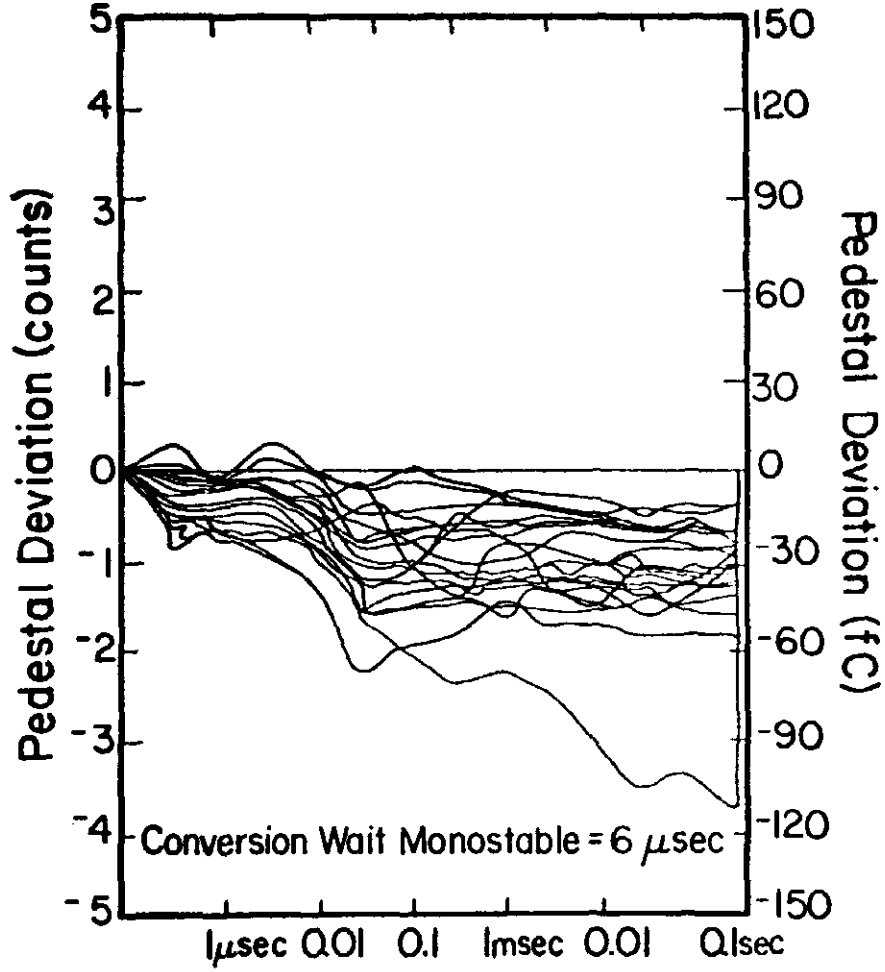

"SIMPLE RATE" TEST SIGNALS

Fig. 4b




PUMP UP EFFECT

Fig. 5a




RATE EFFECT

Fig. 5b

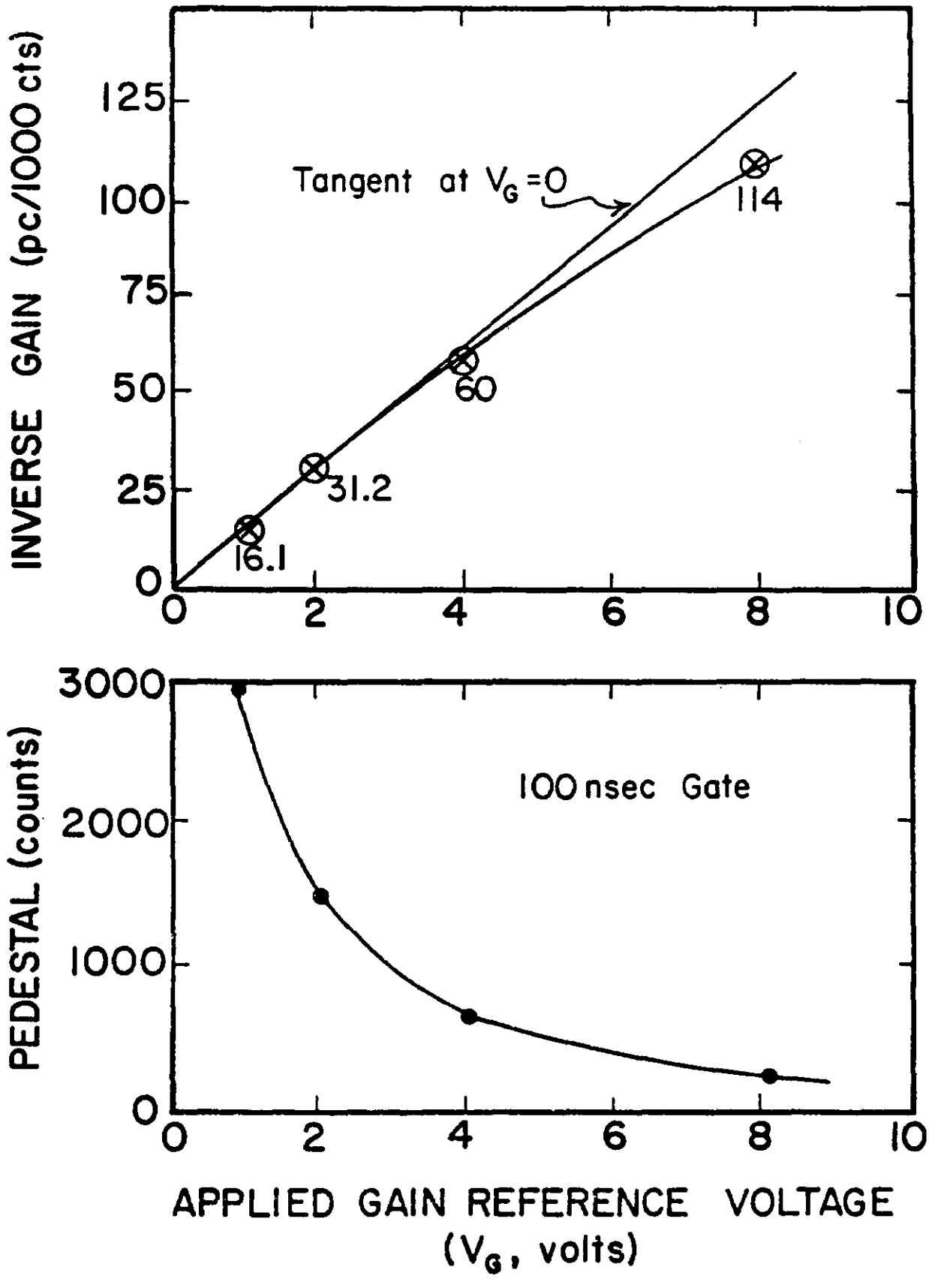

INVERSE GAIN (pc/1000 cts)
125
100
75
50
25
0
Tangent at $V_G$ =0
114
60
31.2
16.1
0
2
4
6
8
10
PEDESTAL (counts)
3000
2000
1000
0
100 nsec Gate
0
2
4
6
8
10
APPLIED GAIN REFERENCE VOLTAGE
($V_G$, volts)

Fig. 6

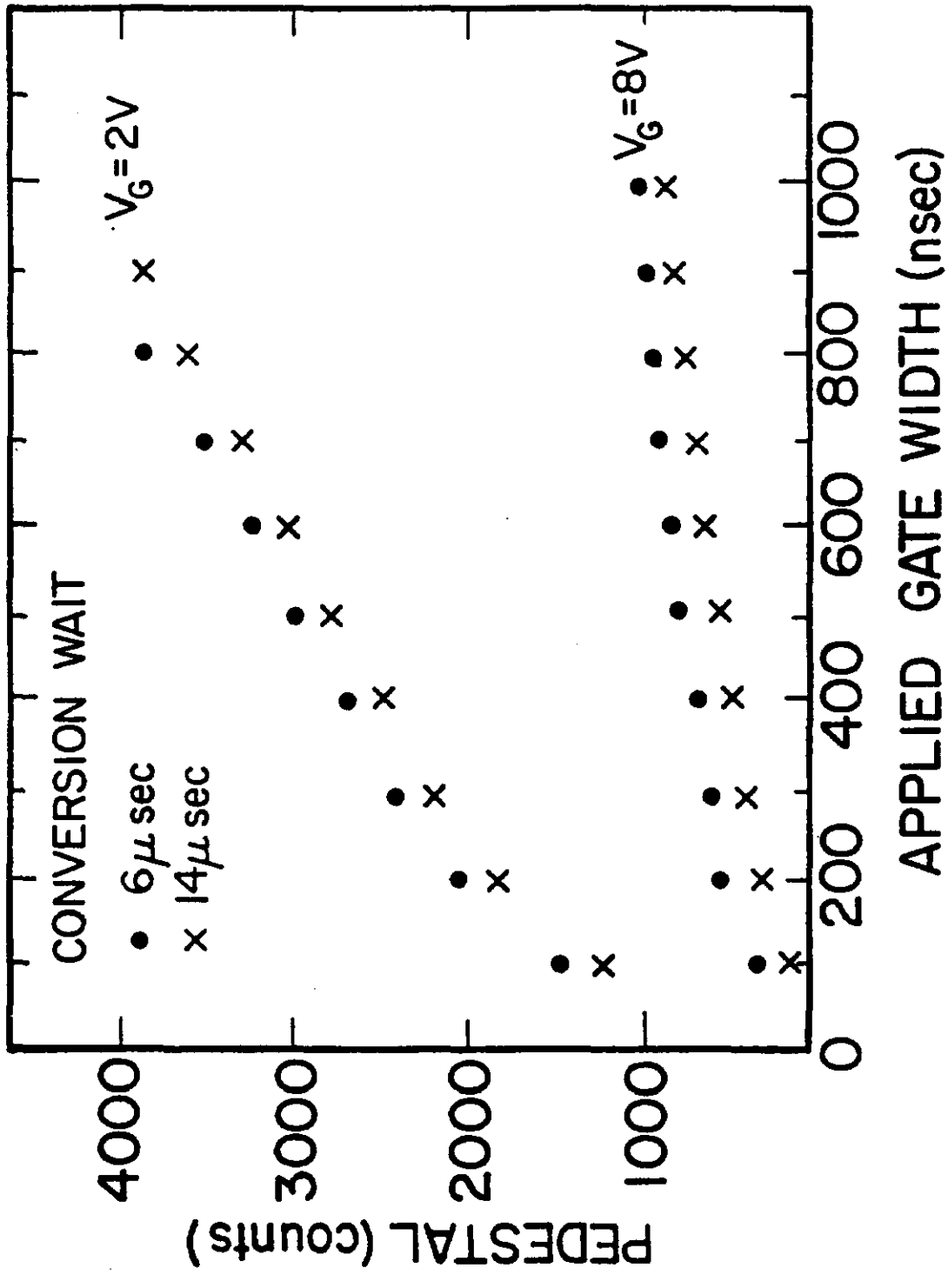

PEDESTAL (counts)
4000
3000
2000
1000
0
200
400
600
800
1000
APPLIED GATE WIDTH (nsec)
CONVERSION WAIT
• 6μsec
× 14μsec
$V_G$=2V
$V_G$=8V

Fig. 7

# APPENDIX

## MODIFICATIONS MADE DURING DEVELOPMENT STAGES OF LECROY 2280/2285

The items in the following list are arranged by category--i.e., according to the purpose for which they were intended. The bulk of these items were worked out at Fermilab, with the knowledge of LeCroy Research Systems. Most of these (or equivalent changes) have been retained for the final standard units as delivered by the manufacturer.

**Poor linearity after early fix for worst rate dependences.**

Changed pedestal compensation pin on hybrid from floated to +9 volts.

Correction of crate loading problem when more than one module is in the crate.

Sensitive reference voltages are no longer taken from the +6 volt line.

In an earlier Fermilab ad hoc fix, the six volt power supplied by the CAMAC crate was used only for the +5.2 volt power. Due to the effects of 5.2V burst loading, an additional external +6 volt power was supplied on the Y2 and G CAMAC bus lines for all other purposes. For this fix, protection Ge diodes were added to prevent damage when CAMAC and external supply are not both on or off. This technique may be of interest to other system users with older versions of this line.

Smooth response of linear gate circuit.

Removed C5 capacitor.

Gain control and front end amplifiers.

Achieved high gain without the times three amplifier at the front end of the hybrid circuit. This removed a contributor to the slow turn on of the gate.

Change of resistor network to get full range variation of gain with a one to ten volt input (changed by a factor of about two).

Linearity of test circuit response to TEST LEVEL input.

Completely redesigned original internal pulser circuit, driver, fanout and distribution.

TEST LEVEL input connector floated and cabled directly to P1 and P2 CAMAC lines. Floating the input maintains the isolation of the signal return from ground.

TEST ENABLE state enables firing of the test circuit by the application of the next gate. Prior to this, the trigger out was intended to start the sequence when the TEST ENABLE state was first initiated.

Clear operation rate dependance improvements:

Applied fast clear automatically at end of conversion--the earliest possible time.

Applied digital clear to scalers after last channel out--the earliest possible time. This early ad hoc change is no longer required for the current versions. When done, however, additional modifications are required for clearing for CAMAC F9 and C commands.

When consistent with experimental application, removed the fast clear operation completely. In this case, every gated event is read out.

Adjust wait monostable before conversion started to match experiment needs related to noise (spark chamber firings) and pedestal values.