Electronic Front-End for LHCb Electromagnetic and Hadronic Calorimeters

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ELECTRONIC FRONT-END FOR LHCb ELECTROMAGNETIC
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ABSTRACT

The electronic front-end of the LHCb electromagnetic and hadronic calorimeters will be described. It consists of a 9U 32 channel board, each channel including shaper-integrator, 12 bit ADC and lookup tables allowing to code the transverse energy information both for readout and for the Level 0 trigger. The readout information is stored in a fixed latency followed by a derandomizer. The trigger information is processed further on the board by FPGA, performing channel addition and comparison to extract the highest transverse energy local cluster for further processing. The system is fully synchronous and allows to extract candidates for calorimetric trigger at every 40 MHz clock cycle. The operation and characteristics (noise, linearity etc.) of a prototype board will be described.
1 Introduction

The LHCb calorimetry is based on an electromagnetic and a hadronic calorimeter, a preshower and a scintillator pad detector. This set of four detectors takes place between M1 and M2 muon chambers (Fig. 1). It provides high transverse energy hadron, electron and photon candidates for the first level trigger which takes a decision 4 us after the interaction. Its other essential function is the detection of photons to enable the off-line reconstruction of B-decays. These physics goals define the general structure of the calorimeter system and its associated electronics in term of resolution, shower separation, selectivity and fast response. The electromagnetic and hadronic are lead-scintillator and iron scintillator sandwiches read by light shifting fibers. The output of the plastic fibers is equipped with phototubes. The readout system will have about 6000 channels for the Ecal and 1500 for the Hcal. For economic reasons the Ecal and Hcal calorimeters will be equipped with the same electronics including fibers and PMs. The crates and the backplanes will be identical for the four detectors.

Figure 1: The calorimeter system.
2 Requirements

The main requirement for LHCb electronics is the pile-up rejection. To ensure a satisfactory independence of successive samplings, it makes use of fast fibers, fast PMs and shaping. Shaped signal has to be sampled at 40 MHz on 12 bits to cover the resolution over the full dynamic range of the two calorimeters (50 MeV to 200 GeV). The data are transcoded within LUTs into energy over 8 bits for trigger data and 12 bits for readout data. The latter has to be buffered during the first level (L0) latency of 3.2 μsec, derandomized and then rebuffered for the second level (L1) latency of 256 μsec. After the L1 trigger, an extended zero suppression needs to be performed before sending the formatted event to the DAQ. There are also trigger elements sitting in the front-end crate. The first stages concern the search for local maxima inside groups of 512 channels, with a validation by the Preshower and Pad Chamber data.

3 WLS Fiber time properties study

The pulse shape properties of different wavelength shifting fibers has been measured. This has been done both at X7 test beam and using ultra-violet N2 laser as shown on figure 2. In the X7 beam test high energy electrons are converted to showers in 5 cm of lead. The two methods have been shown to be equivalent and then allow a complete study of the fibers off the beam. Figure 3 shows the measured pulse shapes for 5 different fibers. The shortest pulse is obtained from the BCF-92 with a FWHM of 9 ns.

Figure 2: The light in the scintillating tile is induced either by high-energy electron (A) converted in lead or UV-laser pulse (B).
Due to radiation constraints the slower Y-II fiber will be used close to the beam while the BCF 92 will equip the external part of the calorimeters.

Figure 3: The recorded pulse shape for different WLS fibers: 1 - BCF92; 2 - BCF-99-29A; 3 - Pol.Hi.Tech (S250); 4 - Y-11(M250); 5 - Y-11(M200); 6 - BCF-91A.

4 Front-End overview

The electronic front-end will be situated on the top of the calorimeter. The total dose expected is 100 rads over one year thus allowing the use of commercial components. 14 Ecal crates and 4 Hcal crates receive respectively 6000 and 1500 channels. Figure 4 describes the Ecal front-end crate and its main interconnections. The PM signals are connected to the front-end board through 10 meters of coaxial cables. There are 16 Febs in the crate, each receiving 32 signals. The outputs of these boards are connected to the custom backplane, sending signals using LVDS or GTL+ levels to the Calorimeter Readout Controller and the Validation boards. The CROC performs an advanced zero suppression and the event formatting after level 1. Data is then sent to the DAQ through optical links. This board receives ECS and TTC signals and then distributes clock, global commands and the serial link which is used for
loading the hardware over the whole crate. From its 32 signals, and using also neighboring cells, each FEB computes, in pipeline mode, the maximum of the 32 sums over every 2x2 cell area. This maximum is sent to the Trigger Validation Board assuming 8 Febs for one Validation. The Preshower and the Pad Chamber validate the Ecal candidate. Ecal candidates validates Hcal ones. The output is sent to selection crate via optical links to get the highest (and second highest) of the candidates, this being done for each type of particle.

Figure 4: The front-end crate.

5 The Front-End board

Figure 5 shows the block diagram of the 32 channel front-end board. The latter is a 9U board using VME mechanics but without the VME bus. The access to the board, for initialization and monitoring, will be performed thanks to a serial bus which has still to be defined. The main data path inside the board starts with the four 8-channel coaxial input connectors. The signal goes into the cable compensation, a pole zero network compensating for a 10 % - 20 nsec signal tail, before entering the analog chip. These front-end elements will be described in the next chapter. After a 12bit ADC conversion, data undergoes a subtraction of the smallest of the two previous samples. This subtraction is intended to reduce the high bandwidth noise of the integrator, and the two
samples are used to decrease the probability that a signal is present in the sample, which is subtracted.

This operation is performed at 40 MHz and has been integrated in a big FPGA. Then data is converted into energy within two LUTs, one for the trigger which outputs 8 bits for transverse energy, the other for the readout data which outputs 12 bit words in a pseudo floating format allowing gain compensation. The latter data is then sent to the LO latency pipeline, LO derandomizer and L1 latency buffer. After L1 trigger, data is tagged with the bunch crossing ID., serialized and then sent across the backplane using LVDS levels towards the Calorimeter crate controller. At the right top of the board is the trigger part. Looking for the local maximum over the 32 channels needs to receive an extra row and an extra column of cells and therefore send it to the neighbors. This is performed via both point to point GTL+ link on the backplane and Cat5 cables at 280 MHz to the neighbor crate after serialization. Trigger data is first added in squares of 4 cells still preserving the original granularity, then compared looking for the local maximum on the board. The latter is sent with its address towards the Trigger Validation Board. Beside those data paths, some utility functions have been implemented. To correct for variable time
delay in PM, and spread time in fibers one can adjust the sampling time on the
plateau of the analog signal for every channels thanks to programmable delay
chips with a precision of 1 ns. It covers a range of 12 ns thus allowing to align
all the channels in the same bunch crossing. A functional analog calibration has
also been implemented to check the complete readout chain. This has already
been useful during the test beam operations. Another important element is the
use of test procedure generated inside the PGA dedicated to the subtraction
and which can output special pattern and allows to test and debug the complete
trigger chain.

6 The Front-End elements

The purpose of those elements is to shape the PM pulses in less than 25 ns to
avoid electronics pile-up. The characteristics aimed for are the following:

- At the input: the PM maximum current is 20 mA over 25 ohms.
- At the output: the ADC input dynamic range is 1V under 250 ohms.
- The residue after 25 ns should be smaller than 1 %.
- The sampling area should cover ± 2 nsec with a 1 % precision.
- The RMS noise should be < 1 ADC count (250µV).

To fulfill the above requirements, two problems have to be solved. The
first one concerns the PM signal. If one looks at Fig 6, which shows an PM
signal, the PM output current has a fast rise time but a slow decay that goes
over at least the two consecutive samples at 40 MHz.

![Normal and Clipped (5 + 5 ns 23 Ohms) Signal](image)

**Figure 6: PM output pulse with and without the clip.**
It thus needs to be pulled to zero after 10 ns to ensure the zero pile-up requirements. The remaining area is on the order of 60% of the original one. To perform this cut on the signal, the clipping circuit shown on Fig 7 will be used. It consists in a short 5 nsec cable located at the output of the PM base. The signal is sent towards a variable network which will send back an inverted part of it.

Figure 7: Front-end Electronics

As both the source and reflected signals are, on average, negative exponential, their superposition gives an almost zero signal, as shown in blue line on fig. 3. Now that the input signal has been shaped, we have to measure the energy deposited in the calorimeter. The corresponding information is the area of the PM signal. The best way to measure it without deteriorating too much the statistic fluctuation is to integrate this signal in a capacitor (Cf) as shown in figure 7. The difficulty then becomes to empty this capacitor. Two ways are possible:

- **Use a switch mounted in parallel** but this system induces a dead time when the capacitor is being emptied, which implies the use of two integrators in parallel and a multiplexor. But due to the inevitable injection of charge from the switches, pedestals are generated which can be the sources of offset shifts at the 1% level.
• Subtract in a linear way the signal to itself thanks to a specific configuration. The latter is the chosen solution. The configuration appears in the middle of Fig. 5. The input signal is diverted, delayed by 25 ns, then subtracted to itself thanks to the differential buffer. The latter also has in charge the division of the input current to adapt it to the small value of \( C_f \). This solution is the one already proposed in the LHCb technical proposal.

The buffer and the integrator inside the dashed line of the Fig. 5 have been integrated in a 0.8 um BICMOS Asic. It houses 4 channels in a 44 pin plastic package. The performances of the chip are summarized in Table 1.

<table>
<thead>
<tr>
<th>Simulation Results</th>
<th>Current Test Bench Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range : 1.4 V</td>
<td>(\iff 1.4 V)</td>
</tr>
<tr>
<td>Non Linearity : 0.5 %</td>
<td>(\iff &lt; 1%) over the whole dynamic range</td>
</tr>
<tr>
<td>Residue after 25 ns :&lt; 0.5%</td>
<td>(\iff &lt; 1%) (undershoot 3%)</td>
</tr>
<tr>
<td>RMS Noise after subtraction</td>
<td></td>
</tr>
<tr>
<td>1 ADC count</td>
<td>(\iff 1.1) ADC Count</td>
</tr>
<tr>
<td>Power Consumption : 40mW/Channel</td>
<td>(\iff 38) mW/Channel</td>
</tr>
<tr>
<td>Open-Loop Gain : (\approx 60) dB</td>
<td>(\iff \approx 60) dB</td>
</tr>
<tr>
<td>( gm) (Input PMOS) = 34 mA/V</td>
<td>( gm) (Input PMOS) = 18 mA/V</td>
</tr>
<tr>
<td>Fall Time : 3 us</td>
<td>(\iff 2) us</td>
</tr>
<tr>
<td>Rise Time : 2.5 ns</td>
<td>(\iff 5) ns</td>
</tr>
<tr>
<td>Input Impedance : 190 (\Omega)</td>
<td>(\iff 270) (\Omega)</td>
</tr>
</tbody>
</table>

The functionality of the chip is satisfactory and it is mounted on a prototype of the front-end board used in test beam. The results show a good adequation between simulation and real circuit, except for the \( gm \) of the input transistor. This is due to simulation models and also explains the mismatches with the measurements in the rise time and the input impedance of the integrator.

7 The prototype Front-End Board

Fig. 8 offers a picture of the board. On the left side, one can see the 2 x 8 channel input connectors, followed by the PM and cable compensation networks and the delay lines. The four 4 channel analog chips are followed by half the ADCs
and the LUTs. All the big FPGAs (10K50 and 6K16) are on the other side of the board, together with the other half of the ADCs.

Figure 8: Top layer of the prototype FEB.

8 Test Beam Results

The width of the signal at the output of the chip (figure 9) is larger than on test bench because of the fiber decay time and PM risetime.

Figure 9: Output signal after integration.

Nevertheless the shape at the output of the integrator matches the requirements with a flat top within 1% for +2 nsec and a small residue after and before 25 ns.
The figure 10 shows a pulse-height spectrum of 50 GeV electrons measured in 6 successive ADC samples with the test board.

Sample 5 contains the peak of the signal. The first sample corresponds to the RMS noise of 1.8 Adc count after subtraction. Sample 4 and 6 show the contribution of the signal less than 2%. On sample 8, we’re back to the baseline.

9 Next steps of the development

The radiation environment related to single event upset is not very well known especially on the top of the calorimeter. We use a large amount of RAMs and SRAM based PGAs which are very sensitive to this effect. Therefore we need to identify with precision what kind of particles and what energy can provoke these SEU. From literature 3) it seems that protons and neutrons with an energy over 10 MeV are the major cause of SEUs. Based on these assumptions we will extract from simulation an estimation of the order of magnitude of the radiation environment. In parallel we attempt to proceed tests on neutron test beam with the board we designed for the trigger test which is fully digital. From its 32 * 8 bit inputs we perform a 2x2 sum and output the maximum and its
address at 40 MHz, then compare it by software to the expected result. This procedure can give a precise idea of the error rate with respect to the number of rams and configuration bits of FPGA and compare it to simulation results.

10 Acknowledgements

The card, the chip design and the construction were done by electronics engineers and physicists of the Orsay LAL laboratory. Beam tests and discussions on the electronic design were done within the LHCb calorimeter group whose members I wish to thank here. I wish to mention especially D. Djeliadine and A. Konopliannikov who initiated the idea of the delay line integrator reset described in section 6.

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