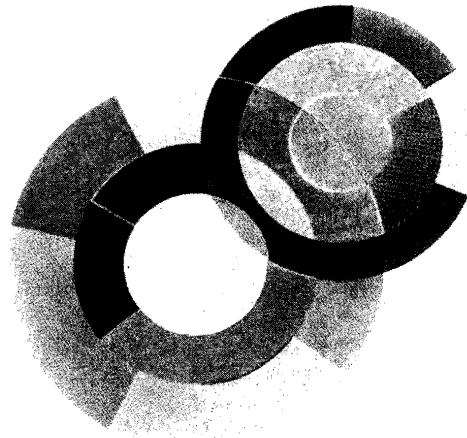
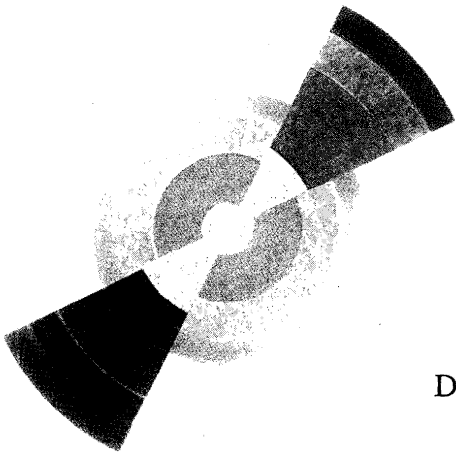
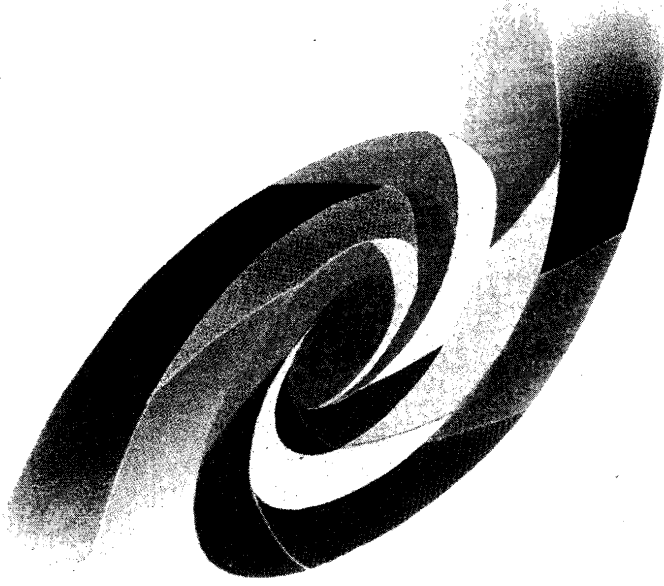


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Monolithic active pixel sensors with in-pixel double sampling operation and column-level discrimination

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Monolithic Active Pixel Sensors with In-pixel Double Sampling Operation and Column-level Discrimination

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Abstract-- Monolithic Active Pixel Sensors constitute a viable alternative to Hybrid Pixel Sensors and Charge Coupled Devices for the next generation of vertex detectors. Possible application will strongly depend on a successful implementation of on-chip hit recognition and sparsification schemes. These are not a trivial task, first because of very small signal amplitudes (\sim mV), originated from charge collection, which are of the same order as natural dispersions in a CMOS process, secondly because of the limitation to use only one type of transistor over the sensitive area. The paper presents a 30×128 pixel prototype chip, featuring fast, column parallel signal processing. The pixel concept combines on-pixel amplification with double sampling operation. The pixel output is a differential current signal proportional to the difference between the charges collected in two consecutive time slots. The readout of the pixel is two-phase, matching signal discrimination circuitry implemented at the end of each column. The design of low-noise discriminators includes automatic compensation of offsets for individual pixels.

The details of the chip design are presented. Difficulties, encountered from being the first attempt to address on-line hit recognition, are reported. Performances of the pixel and discriminator blocks, determined in separate measurements, are discussed. The essential part of the paper consists of results of first tests performed with soft X-rays from a ^{55}Fe source.

I. INTRODUCTION

Future HEP experiments will require the development of a linear collider in the TeV energy region. Because of physics requirements, the need of precise vertex measurements makes a high resolution vertex detector (VXD) an essential part of the experiment apparatus. One option considered for VXD

construction is a Monolithic Active Pixel Sensors (MAPS) based detector. The ability of MAPS, realised in a CMOS process, to provide charged particle tracking has been demonstrated with a MIMOSA* chips family [see e.g. 1]. The results were obtained on a series of small scale and 1 million pixel large prototypes, that were essentially fabricated exploiting a classical 3-transistor (3T) pixel configuration.

The use of MAPS in particle physics [2] will strongly depend on a successful implementation of on-chip hit recognition and sparsification scheme. On-chip hit processing is not a trivial task, because of very small signal amplitudes, in the range of millivolts, which are of the same order as natural dispersions in a CMOS process. The solution consisting in a storage of reference values for each pixel is impractical, because of waste of active area at the expense of large memory required. Therefore, the correction for offset, performed during every access to a pixel, has been adopted. The calibration operation consists in reading empty data from the chain with a short-circuited input and involves the pixel circuitry in this sequence. A new column-based, low power, offset compensated (auto-zeroed) multistage comparator has been developed completing the pixel design [3]. A planned final detector would include an array of identical pixels with their addressing, signal processing within the chip, sparsification and data transmission circuits. The design of the MIMOSA VI chip, focusing the interest of this paper, is a first step towards construction of high performance detection system integrated on chip.

II. DESIGN OF PIXEL

Novel ideas, optimising charge sensitive elements (CSE) for a vertex detector environment and new pixel configurations with signal amplification and double sampling operation, have been recently proposed [4]. In this new CSE, the charge generated in the lightly doped, undepleted volume is collected by the n-well/p-epi(sub) diode, as it was proposed for 100% fill factor devices in visible light applications [5]. Whereas, the

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* MIMOSA stands for Minimum Ionising particle MOS Active pixel sensor.

reverse bias is provided in a continuous way via a p^{++}/n -well diode, that is forward biased with a leakage current of the charge collecting diode. CSE, whose temporal response is devoided of the leakage current influence, is AC-coupled to all NMOS transistors, with switched power consumption amplifier providing voltage gain of 5-6. The block diagram presenting the pixel concept is sketched in Fig. 1. The double sampling operation is achieved using two storage capacitors, C_{s1} and C_{s2} , placed in the feedback path of the amplifier. The AC-coupling capacitor is C_{c1} . The output stage of the pixel is built with a linearised differential stage with a transconductance of $100 \mu S$, allowing differential output current proportional to the charges collected in two consecutive time slots.

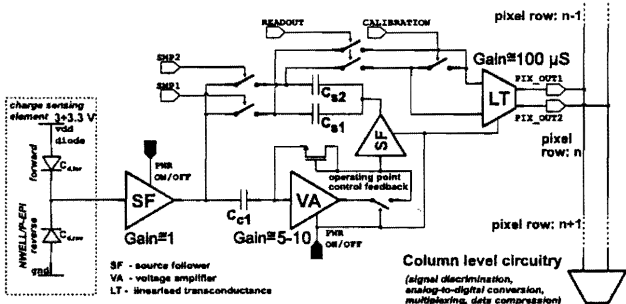


Fig. 1: MIMOSA VI pixel concept based on auto reverse polarisation of charge collecting diode.

The calibration and offset cancellation of the analogue chain can be obtained by short-circuiting the input of the differential stage. Fig. 2 shows schematic diagram of the charge sensitive element with auto-reverse polarization and a simplified schematic diagram of the on-pixel all-NMOS transistors amplifier.

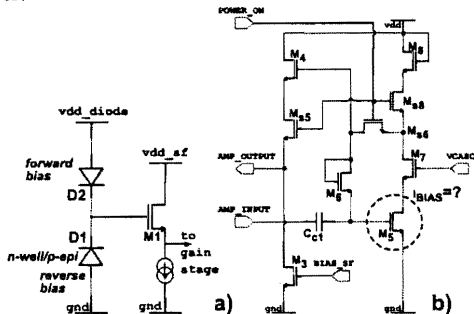


Fig. 2: Schematic diagram of the charge sensitive element with auto-reverse polarisation (a), schematic diagram of all NMOS amplifier (b) (storage capacitors are placed in the feedback path of the amplifier - not shown).

III. DESIGN OF COMPARATOR

In the MIMOSA VI chip, a single comparator is shared by all the pixels of one column and the pixel outputs are switched sequentially to the front-end of the comparator. Fig. 3 presents a simplified architecture of an offset compensated comparator developed. The width of the comparator matches the $28 \mu m$ of the pixel pitch achieved in a careful layout design. To speed up the comparator, each gain stage is realised using two cascaded

low gain amplifiers. The two source followers buffers are used to reduce the kick-back effects of the latch. All the switches are realised using PMOS transistors, with dummy switches used to reduce charge injections. The reference levels are injected in form of currents instead of voltages. The comparator has a fully differential architecture, allowing improving PSRR, overcoming substrate coupling problems and charge injection in switches.

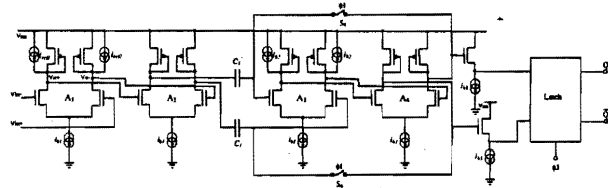


Fig. 3: Schematic diagram of the offset compensated comparator.

The timing diagram for the comparator is inscribed into the readout sequence of the pixel. Its simplified form is given in Fig. 4. During τ_1 (CALIBRATION phase), the threshold level (proportional to $V_{ref1} - V_{ref2}$) is amplified and stored on capacitors. The pixel offset voltage, after conversion from current, is applied on the gates of the input amplifier and the amplified value is stored on the capacitances together with offsets of amplifiers for later correction. Then, during τ_3 (READOUT phase), a fixed voltage V_{ref2} is applied to the gates of the current source transistors in Fig. 3, that leads to subtraction of mismatches. The amplified input signal is compared to the threshold level and the resulting logic state is latched.

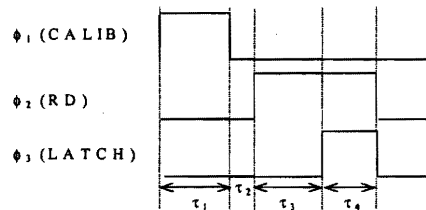


Fig. 4: Timing for the comparator.

The output current of the pixel is converted back to voltage at the input of the comparator by means of two triode region operated transistors with gate voltages imposed from outside of the chip. Thus, the conversion factor, referred to the input of the comparator, is adjustable. It can be varied from $10 \mu V/e^-$ to $100 \mu V/e^-$.

Four different design of discriminators, i.e. T0, T1, T2 and T3, implemented on the MIMOSA VI chip as a test structures, were tested. T0 and T1 are both identical designs* based on 4 differential stages of gain and a dynamic latch, T2 comprises 3 differential gain stages and a dynamic latch, while T3 features a static latch [3]. The layout dimensions of comparators are $28 \times 300 \mu m^2$ (T0/T1).

* Identical comparators T0 and T1 are implemented on the chip to observe the mismatch between them.

IV. MIMOSA VI CHIP DESIGN

The MIMOSA VI chip, fabricated in a $0.35\ \mu\text{m}$ CMOS process with $4.2\ \mu\text{m}$ of the epitaxial layer, features an array of 30×128 pixels, where 24 columns are connected to the discrimination stages for binary readout and the remaining 6 columns are connected, via simple current amplifiers, directly to the output pad, making access to the analogue data possible. The pixel pitch is $28\ \mu\text{m}$ and pixels with two diode sizes, i.e. $4.0 \times 3.7\ \mu\text{m}^2$ ($3.5\ \text{fF}$) and $5.0 \times 4.7\ \mu\text{m}^2$ have been used. Fig. 5 shows a layout of the prototype. The clock frequency used to drive the matrix of pixels is $30\ \text{MHz}$ or $40\ \text{MHz}$, and the readout of a single pixel is done in two different modes, requiring 6 or 8 clock cycles, respectively.

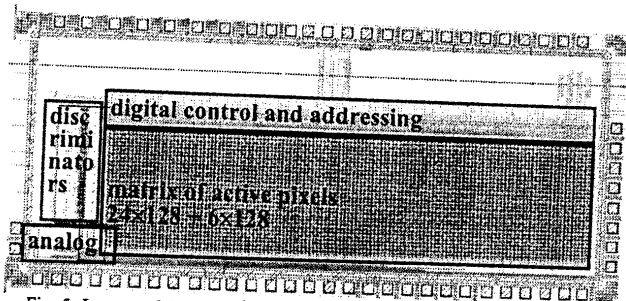


Fig. 5: Layout of the MIMOSA VI prototype.

V. ESTIMATION OF CHIP PERFORMANCES

The chip has been extensively tested. The electrical performances of constituent blocks were examined independently, i.e. pixels in the sub-array, for which direct analogue outputs are available, and the comparators in the test structures, placed aside the main array. The tests of the whole systems, comprising the discrimination stages and array of pixels were not performed, being impeded by unanticipated pixel-to-pixel dispersions of signals levels. The dispersions, that could be referenced to the equivalent input signal of one hundred and a few tens of electrons, were observed despite subtraction of the reference value. The qualitative description of dispersions and the analysis explaining their origin are discussed in the following sections. The summary of chip parameters and its performances is given in Table 1.

A. Discriminating stage

The functionality of comparators was studied with a clock of up to $80\ \text{MHz}$. The residual offset below $1\ \text{mV}$ can be achieved at the clock frequency of $40\ \text{MHz}$, which translates to the $5\ \text{MHz}$ frequency of the full processing. The power consumption was measured in the order of $200\ \mu\text{W}$ @ $40\ \text{MHz}$. The design goals for discriminators were attained. The two examples of the normalised noise response of the comparators, measured at different timing conditions versus threshold voltage, are shown in Fig. 6. The temporal noise is calculated as a derivative of curves plotted in Fig. 6. Its value remains below a few hundreds of μV , when referred to the input. It was shown that precision of the calibration operation

depends strongly on the calibration time τ_1 , due to the need of charging relatively big $400\ \text{fF}$ storing capacitances. The reduction of the time τ_1 leads to increase of the residual offset, which remains below $1\ \text{mV}$ for τ_1 longer than $60\ \text{ns}$.

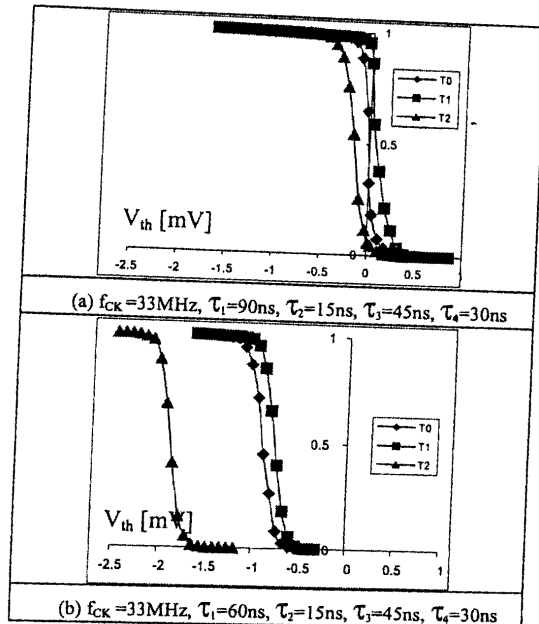


Fig. 6: The normalized noise response of the comparators versus threshold voltage with the inputs at the same reference voltage ($V_{ref2} = 2\ \text{V}$).

B. Pixel

The pixel performances were simulated using the integrated simulation environment under CADENCE, while the temporal noise has been examined in the time domain with the ELDO simulator. Fig. 7 shows the differential current rms noise during a pixel readout cycle and the differential pixel output current corresponding to the collection of $1000\ e^-$ on the n-well/p-epi diode. During the *READOUT* phase, an average noise value of $152\ \text{nA}$ (rms) corresponding to $15\ e^-$ ENC and a pixel sensitivity in the order of $10\ \text{nA}/e^-$ have been obtained.

The pixel parameters were estimated in tests of the six columns of pixels, where the analogue outputs were available. The tests were performed at a readout clock frequency of $10\ \text{MHz}$, which was limited by the readout circuitry external to the chip. Fig. 8 shows an oscilloscope view of the raw output from one column of pixels. The differential current was converted to voltage on two $825\ \Omega$ resistances and the resulting signal is amplified by a factor of 5.

Two waveforms in Fig. 8 correspond to the difference of currents transmitted in a differential mode to the data acquisition system, where ADCs were seated.

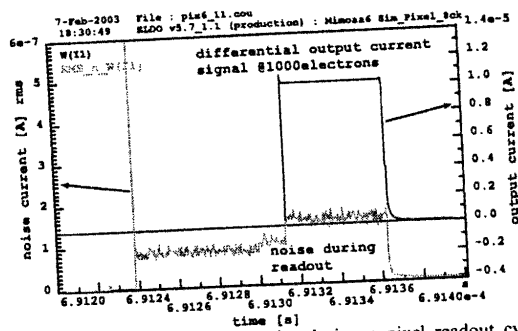


Fig. 7: Differential current rms noise during a pixel readout cycle (left axis), for a differential current signal corresponding to 1000 e^- collected.

For a readout time of the first pixel in the column, the clock frequency was slowed down to 1MHz to obtain clearer illustration of the readout phases [2] shown in Fig. 8.

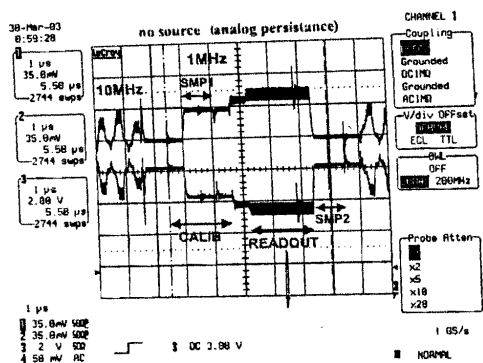


Fig. 8: Oscilloscope view of the raw output from one column of pixels.

The detection performances of the MIMOSA VI chip have been first assessed with soft X-rays by exposing the chip to a ^{55}Fe source. The tests were performed on individual pixels selected from the matrix. The measurements were used to estimate the conversion gain of the pixel. An example of the hit histogram measured on a single pixel is shown in Fig. 9. The data have been registered for an integration time of 77 μs , using a digital 8 bit oscilloscope.

At the next step, the suppression of, intrinsically present in CMOS active pixel sensors, pixel-to-pixel dispersions, using calculation of signals difference between the *READOUT* and *CALIBRATION* phases, was to be verified. Fig. 10 presents distributions of signals sampled during the both phases and of the calculated difference. The subtraction of the calibration signal level allows squeezing the level of pixel-to-pixel dispersions more than 5 times. However, the residue is still important translating to $\sim 100 e^-$ (1σ) of equivalent input signal. The non fully compensated dispersions hamper the correct setting of the comparator threshold level in a common way for all pixels from one column.

The reported level of pixel-to-pixel dispersions cannot be reproduced in Monte Carlo simulations using available models of mismatch variations. As the conclusion, it was apparent that the variation of active components parameters does not give

rise to the dispersions observed.

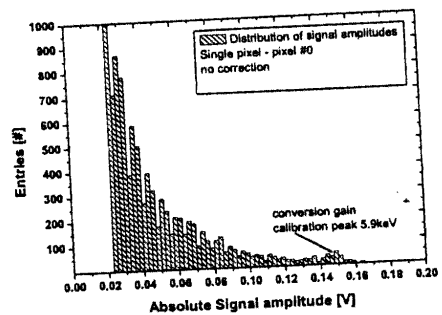


Fig. 9: Hit histogram for a single pixel for the exposure to the ^{55}Fe source.

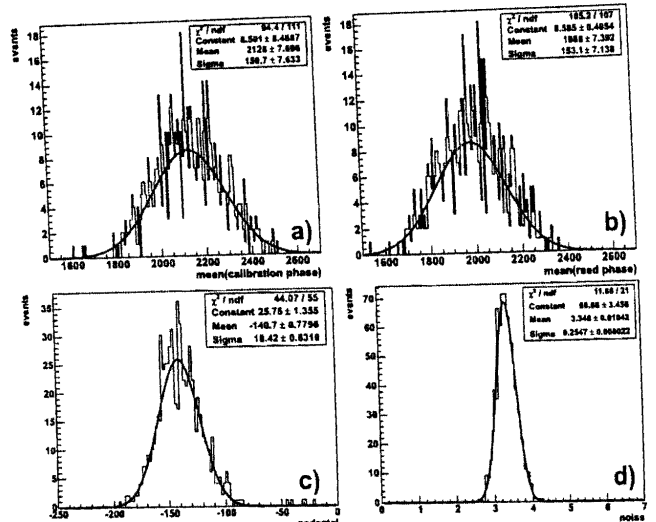


Fig. 10: Distributions of signals sampled during the *CALIBRATION* (a) and *READOUT* (b) phases and of the resulting difference (c), and the mean variance of the difference signal (all expressed in ADC units without absolute calibration).

VI. STUDY OF PIXEL-TO-PIXEL DISPERSIONS

The detailed analysis of origins of dispersions is hampered by the fact that the design-kit used for the chip design offers only limited level of device modelling. After excluding the mismatches of active components in Monte-Carlo simulations, the origin of dispersions has been attributed to the variation of parasitic capacitances. These capacitances (Metal-Metal, Metal-floating diffusion, Metal-Poly) introduce coupling between lines with switching signals and sensitive nodes of the circuit. Modelling of parasitic coupling is extremely difficult; firstly: due to the aforementioned incompleteness of the extraction model^{*}, secondly: parasitic capacitances, influencing pixel behaviour, barely exceed a few tens of aF and their variations are unknown and difficult to estimate. An "intuitive" approach was applied to carry out parasitic coupling analyses. The results obtained were comparable with

^{*} e.g. extraction of parasitic capacitances to POLY2 layer was not included in the design kit.

measurements. Fig. 11 shows an example of possible parasitic coupling with digital lines within a pixel area. The sensitive nodes are terminals of two sampling capacitors.

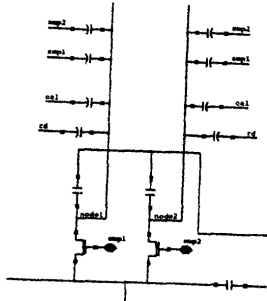


Fig. 11: Example of parasitic coupling with digital lines within pixel.

The excerpt of the pixel layout, corresponding to the situation from Fig. 11 is shown in Fig. 12. The layout has been designed in a careful symmetrical way, but variations in parameters, like isolation oxide thickness or metal line width, perturbate this symmetry, resulting in signal dispersions.

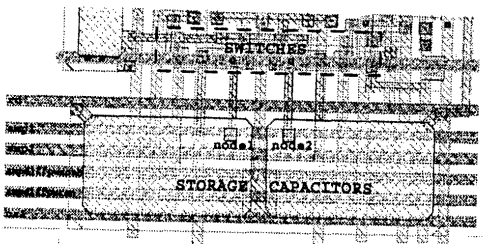


Fig. 12: Sampled output signal from a single pixel during the exposure to the ^{55}Fe source.

Simulation results of signal dispersions due to coupling through the sets of different parasitic capacitances are shown in Fig. 13. The figure shows the differential output current of a single pixel considering different coupling ways.

The important design features and main parameters extracted from the first measurements of MIMOSA VI are summarised in TABLE I. Noise level reported corresponds to the calculated difference between the level in *CALIBRATION* and *READOUT* phases and the pixel dispersions are referred as to the pixel-to-pixel variation between the DC levels for the two phases in the pixel readout cycle.

VII. CONCLUSIONS AND PERSPECTIVES

The MIMOSA VI chip is the first step towards the development of a smart MAPS based vertex detector. The functionality of the column based comparators has been demonstrated. The possibility of in-pixel integration of double sampling operation allowing to decrease intrinsic pixel-to-pixel output level dispersions has also been shown. The limited efficiency of the current implementation of zero-suppression technique is attributed to the parasitic stray and substrate capacitances. Improvement can be achieved by careful circuit and layout studies. This includes increase of the gain of the

on-pixel amplifier to the level of 10 or more, reduction of number of control lines, special care about fully symmetrical layout of critical parts and minimise coupling by pushing away "truculent" lines.

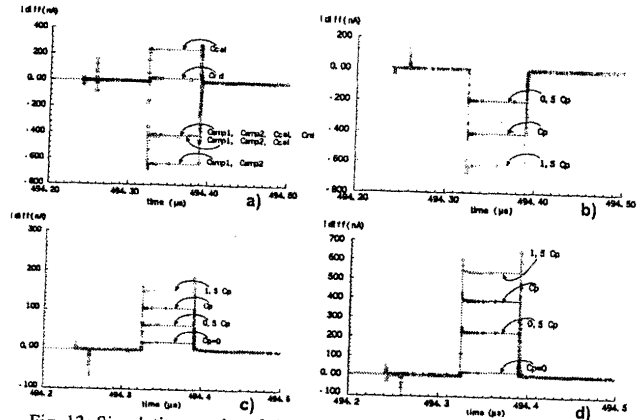


Fig. 13: Simulation results of signal dispersions due to coupling through the sets of different parasitic capacitances. The differential output current of a single pixel is shown; effects: digital control lines and 2 sensitive nodes of storage capacitors: $C_{cal-n1}=C_{cal-n2}=65\text{aF}$, $C_{rd-n1}=C_{rd-n2}=65\text{aF}$, $C_{amp1-n1}=745\text{aF}$, $C_{amp1-n2}=360\text{aF}$, $C_{amp2-n1}=745\text{aF}$, $C_{amp2-n2}=360\text{aF}$ (a); digital control lines and 2 sensitive nodes of storage capacitors, when varying all parasitic capacitors in the same direction (by $\pm 50\%$ of extracted values) (b); two analogue nodes, i.e. input of the amplifier and the internal node of differential amplifier (step from 0V two $\sim 1\text{V}$), when the differential amplifier is switching on, parasitic capacitance is only of 20aF (two adjacent M1 lines of $0.7\mu\text{m}$ long) (c); digital line (READ) at the proximity of the charge collecting diode, parasitic capacitor extracted $\sim 150\text{aF}$ (d).

TABLE I
MAIN PARAMETERS OF THE MIMOSA VI CHIP

MIMOSA VI		features				
performances of chip designed		noise ENC: $\sim 20 e^-$, conversion gain: $6.5 \text{ nA}/e^-$ pixel dispersions: $\sim 120 e^-$				
discriminator performances						
τ_1 ns	τ_2 ns	τ_3 ns	τ_4 ns	noise inp.ref.	offset inp.ref.	power
90	15	45	30	$\sim 85 \mu\text{V}_{\text{rms}}$	negligible	$\sim 200 \mu\text{W}$
75	12.5	62.5	25	$\sim 100 \mu\text{V}_{\text{rms}}$	$\sim 400 \mu\text{V}$	$\sim 200 \mu\text{W}$
60	15	45	30	$\sim 100 \mu\text{V}_{\text{rms}}$	$\sim 900 \mu\text{V}$	$\sim 200 \mu\text{W}$

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