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FASPAX ASIC revision 1.b first articles testing and support

Cooperative Research and Development Agreement Final Report

CRADA Number: FRA-2017-0022

Fermilab Technical Contact: Gregory Deptuch

Summary Report
26 July 2019

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In accordance with Requirements set forth in Article XII.A(2) of the CRADA document, this document is the final CRADA report, including a list of Subject Inventions, to be forwarded to the Office of Science and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

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CRADA Title: FASPAX ASIC revision 1.b first articles testing and support

Parties to the Agreement: Field Viewers Ltd Inc and Fermi Research Alliance, LLC

Abstract of CRADA work:

Fermi National Accelerator Laboratory (Fermilab) and Field Viewers Ltd. Inc. (FV) will work together for a period of two weeks to bring up the FASPAX_V1.0b. During this period, Fermilab will help FV come up to speed with the ASIC functionality testing and train in the usage of the FASPAX test setup at Fermilab that uses the NIPXIE architecture with FleXRIO modules. This setup will be initially used for testing of chips to ensure the basic functionality and design parameters. The NIPXIE setup was developed by the Fermilab team, but it is has not yet been verified to be capable of fully testing the FASPAX_V1.0 chip. Fermilab will offer the developed software and hardware to FV for the on-site use at Fermilab. No guarantee is given by Fermilab for the setup to be able to fully cover the scope of the necessary tests. FV will be responsible for using and modifying of the setup to achieve the DOE-BES Phase-I targets.

Summary of Research Results:

The proof of concept work in Phase I confirms the key specifications are met, which are, 13MHz fast frame rate, single photon sensitivity, 10^5 photons dynamic range. With the use of Silicon and CdTe the specifications can target soft and hard X-ray regimes. In addition, Phase I has also verified two potential vendors who can undertake bump bonding of ASIC to the detector. This is key for the four side buttable design that will be proposed in Phase II research. It is believed that in Phase II, an ASIC production version can be developed to provide a four side buttable large area detector, a glass interposer and a full-fledged product development, which will form the main research steps. With the proof of concept in Phase I, Fermilab and FV believe they can present a compelling conclusion to Phase I and lay a foundation for the Phase II proposal that will result in a commercial product for material science experiments worldwide.

Related Reports, Publications, and Presentations:

Zimmerman, Tom, and Junnarkar, Sachin. Development of the FASPAX IC for a high burst rate X-ray imager with very high dynamic range (105) capability in small pixels. United States: N. p., 2019. Web. doi:10.1016/j.nima.2019.01.032.

Subject Inventions listing:

None

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