



---

Managed by Fermi Research Alliance, LLC for the U.S. Department of Energy Office of Science

---

## **Radiation-Hardened, High-Speed Parallel VCSEL Links for High-Energy Physics**

### **Cooperative Research and Development Agreement Final Report**

**CRADA Number: FRA-2016-0009**

**Fermilab Technical Contact: Alan Prosser**

Summary Report  
9/27/2019

### NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at <http://www.osti.gov/bridge>

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:  
U.S. Department of Energy Office of Scientific and Technical Information  
P.O. Box 62  
Oak Ridge, TN 37831-0062  
phone: 865.576.8401  
fax: 865.576.5728  
email: <mailto:reports@adonis.osti.gov>

Available for sale to the public, in paper, from:  
U.S. Department of Commerce  
National Technical Information Service  
5285 Port Royal Road  
Springfield, VA 22161  
phone: 800.553.6847  
fax: 703.605.6900  
email: [orders@ntis.fedworld.gov](mailto:orders@ntis.fedworld.gov)  
online ordering: <http://www.ntis.gov/ordering.htm>

In accordance with Requirements set forth in Article X of the CRADA document, this document is the final CRADA report, including a list of Subject Inventions, to be forwarded to the Office of Science and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

**CRADA number:** FRA-2016-0009

**CRADA Title:** Radiation-Hardened, High-Speed Parallel VCSEL Links for High-Energy Physics

**Parties to the Agreement:** Vega Wave Systems and Fermi Research Alliance, LLC

**Abstract of CRADA work:**

Vega Wave Systems, Inc. has been awarded a Small Business Innovative Research (SBIR) Phase II proposal to the U.S. Department of Energy entitled "Radiation-Hardened, High-Speed Parallel VCSEL Links For High-Energy Physics." The technology proposed under this program is a significant advance (up to 4x) in data rate over current optical link technologies under development. Fermilab supports the technology developed under this proposal as a radiation-hardened, cost-effective solution for optical links for the high-speed data communications in High-Energy Physics and agrees to provide consulting and test engineering in support of this program. Fermilab staff will provide consulting services along with high speed testing of modules before and after radiation testing.

**Summary of Research Results:**

Vega Wave Systems developed an evaluation / test printed circuit board to facilitate validation and verification of the 480Gbps VCSEL optical transmitter. This test board was designed to exercise all forty-eight VCSEL channels simultaneously on a per-channel basis. The board generates various PRBS patterns as well as a 16-bit user-defined pattern. It can also be put into a repeater mode.

Under the supporting CRADA, Fermilab provided software support to develop the software necessary to communicate with and control the test board. A GUI was developed to provide low level manipulation to access register data in the parts on the board and for configuration of the parts at a higher level. The GUI provides a high-level status of all inputs and clock-data recovery (CDRs) and can be expanded to include each channel's status. A low-level register access window is included to access any devices' registers that includes a buffered history window. It also contains a configuration section to configure the chips at a high level, with the ability to change data rates if desired. Ethernet is the default configuration to run at 10GE rate. A pattern generator section is included, so easy control over patterns can be done. It can also dump registers to a file for debugging purposes.

[Click here to enter text.](#)

**Related Reports, Publications, and Presentations:**

NA

**Subject Inventions listing:**

NA

**Report Date:** 9/27/2019

**Technical Contact at Fermilab: Alan Prosser**

**This document contains NO confidential, protectable or proprietary information.**