

FERMILAB-SLIDES-24-0249-SQMS



Demonstrating the Potential of Adaptive LMS Filtering on FPGA-Based Qubit Control Platforms for Improved Qubit Readout in 2D and 3D Quantum Processing Units

IEEE Quantum Week 2024: QCE24 Submission 416

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Introduction

(Least Means Squared)

Goal: Improving Qubit Readout Through Adaptive LMS Filtering!



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Current Methodology

- Readout pulses are very noisy!
- The current method to average readout pulses in post processing for qubit readout works for smaller systems. However, this has limitations as qubit systems scale up.



Qubit Calibration



-0.004

-0.002

0.003

0.004

0.006

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Why Filter Readout Signals?

- 1. Filtered signals = faster convergence to the **center of mass** for the IQ plots.
 - By filtering readout signals on a pulse-by-pulse basis, we reduce the noise in each individual trace before averaging.
 - We can achieve the same level of discrimination with fewer traces or achieve better readout fidelity with the same number of traces.

Larger qubit systems = frequency-multiplexing = increased readout crosstalk... Therefore, faster calibrations are important for larger qubit systems

- 2. Enables us to have a new diagnostic tool for quantum system environment and noise monitoring.
 - Result of using an adaptive filter... more on this later!



Why an LMS Filter?





Commercial Solutions











CORRECTION CONTRACTOR CONTRACTOR



Open-Source Solutions on FPGA

Lawrence Berkeley National Lab's QubiC





FPGA Quantum Controller

ZCU111



ZCU216



- Gen 1
- Max Control Pulse carrier frequency = 6 GHz
- Eight 14-bit DACs @ 6.5 GSPS
- Eight 12-bit ADCs @ 4.096
 GSPS

- Gen 3
- Max Control Pulse carrier frequency = 10 GHz
 - Can push to 12-13 GHz
- Sixteen 14-bit DACs @ 9.85 GSPS
- Sixteen 14-bit ADCs @ 2.5 GSPS
 - Can be combined for 5.0 GSPS



- Gen 3
- Max Control Pulse carrier frequency = 10 GHz
 - Can push to 12-13 GHz
- Two 14-bit DACs @ 9.85 GSPS
- Four 14-bit ADCs @ 5.0 GSPS



Firmware and Readout Chain Overview



Block Diagram of System

Block Diagram of QICK Firmware





Firmware and Readout Chain Overview



Block Diagram of System

QICK Readout Chain (v1)



QICK Readout Chain (v2 = multiplexed)





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LMS Filter



- n: Sample index
- i: Tap index within the filter's impulse response
- x[n]: Noisy input signal
- d[n]: Desired/reference signal
- w[i]: Weights = adjustable weights of LMS
- y[n]: Output signal (estimated signal or noise estimation) at time index [n]
- e[n]: error signal (difference between desired and output signals) at time index [n]
- μ : Learning rate of LMS algorithm
- N: number of taps in the filter, dictating the number of past input samples used by the filter

$$w[i+1] = w[i] + \mu * e[n] * x[n-i]$$
(1)
$$y[n] = \sum_{i=0}^{N-1} w[i] * x[n-i]$$
(2)
$$e[n] = d[n] - y[n]$$
(3)





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Results: LMS Filter Demonstration on FPGA

- 30 MHz, 8 µs pulse with white-noise standard deviation of 1
- Learning rate = 0.0006
- Taps = 64
- Filter was allowed to execute over 10 pulses
- 10th pulse/iteration for both 'x' and 'e' are shown





Results: LMS Filter Demonstration on FPGA

- 30 MHz, 8 µs gaussian chirp with white-noise standard deviation of 1, 5 µs in between pulses
- Learning rate = 0.0006
- Taps = 64
- Filter was allowed to execute over 10 pulses

Latency = 527.66 ns* Took 15-20 minutes to load



Packaged Logic Blocks



Packaged logic block containing weight update
 LMS algorithm

 LMS logic block sends updated weights to FIR compiler



LMS Demo Hardware Resources

TABLE 5.1. RESOURCE OTHER ATTON FOR EMB DEMO ON RESOURCE OTHER ATTON							
Resource	Utilization	Available	Utilization (%)				
LUT	21,964	425,280	5.16%				
LUTRAM	3,529	213,600	1.65%				
FF	33,992	850,560	4.00%				
BRAM	133	1080	12.31%				
DSP	10	42,732	0.23%				
BUFG	7	696	1.01%				
ММСМ	1	8	12.5%				





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LMS Demo: Current Work







- 1. Develop an Adaptive LMS Filter: Implement an adaptive Least Mean Squares (LMS) filter on an RFSoC FPGA-based control board to dynamically fine-tune the readout signals of qubits.
- 2. Integrate and Tune the Filter with the QICK Platform: Deploy the adaptive filter onto the open-source Quantum Instrumentation Control Kit (QICK) platform to enhance its capabilities for quantum experiments.
- 3. Evaluate and Enhance Qubit Readout Fidelity: Evaluate the performance of the adaptive filter in comparison to the current methodology of ensemble averaging and timing to demonstrate its efficiency and effectiveness in improving readout signal clarity.
- 4. Characterize the Noise Profile: Utilize the adaptive LMS filter to conduct a detailed analysis and characterization of the noise affecting readout signals in both 2D and 3D QPU experiments.



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2D QPU Platform



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3D QPU Platform

• **3D QPU** = Superconducting qubits with SRF Cavities



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Characteristic Equations of Noise

- These equations are general equations for the noise power spectral density derived to fit the context of readout signals
- As the main effect of this research is to improve the Signal-to-Noise Ratio (SNR), the equations for SNR can give us insight as to what the sources of noise are





Conclusion

- Foundational work is complete, implementation is underway
- Results will be significantly contributing to multiqubit experiments when complete
 - Latency needs to be measured properly for new LMS filter on hardware, and new design needs more tests before integrating with QICK!





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This material is based upon work supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Superconducting Quantum Materials and Systems Center (SQMS) under contract number DE-AC02-07CH11359



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Backup Slides



Effect of LMS Filter on Readout calibration



Achieve this in the same number of averages!



Best Superconducting Coherence Times

Group	<i>T</i> ₁ (μs)	Freq. (GHz)	Substrate	Primary Material	Year	Ref.
SQMS/Rigetti	~600	4 – 6	Sapphire	Ta/Nb, dry etch	2024	[4]
SQMS	451	4.5 – 5	Sapphire	Ta/Nb, dry etch	2023	[4] (preprint)
Yu (China)	503	3.8 - 4.7	Sapphire	Ta, dry etch	2022	[58]
IBM	340	~ 4	Silicon	Nb, wet etch	2021	[87]
Houck/Princeton	360	3.1 - 5.5	Sapphire	Ta, wet etch	2021	[57]
IBM	234	3.808	Silicon	Al, dry etch	2021	[88]
Schuster	126	4.749	Sapphire	Nb, Fl etch	2021	[89]
Rigetti	133	3.8-4.2	Silicon	Nb	2019	[90]

 TABLE 2.1:
 BEST 2D SINGLE QUBIT COHERENCE TIMES



Transmon Qubit Timeline - SQMS



UCTING QUANTUM

FPGA Controls

- Single RFSoC FPGA is used for controller of 2D qubits.
- 3D QPU uses benchtop control stack for now due to power limitations on ZCU216
 - Xilinx ZCU111 RFSoC UltraScale+ FPGA (Gen 1)
 - 2. Xilinx RFSoC 4x2 UltraScale + FPGA (Gen 3)
 - 3. Xilinx ZCU216 RFSoC UltraScale+ FPGA (Gen 3)
 - XM655 Breakout Card or custom card
 - 16 RF-ADC: 14-bit, 2.5 GSa/s (interleaved)
 - 16 RF-DÁC: 14-bit, 9.85 GSa/s









QICK Firmware v1



QICK Firmware v2







LMS Demo Block Design



UPERCONDUCTING QUANTUM

Qubit Characterization Experiment

- Qubit calibration and measurement on QICK
- This is a standard process for determining the ground/excited state for a qubit, and then determining T_1 and T_2 measurements for a qubit
- The goal is to do this with the LMS filter active and then compare results!







