Design of an 8-Channel 40 GS/s 20 mW/Ch Waveform Sampling ASIC in 65 nm CMOS

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Abstract

1 ps timing resolution is the entry point to signature based searches relying on secondary/tertiary vertices and particle identification. We describe a preliminary design for PSEC5, an 8-channel 40 GS/s waveform-sampling ASIC in the TSMC 65 nm process targetting 1 ps resolution at 20 mW power per channel. Each channel consists of four fast and one slow switched capacitor arrays (SCA), allowing ps time resolution combined with a long effective buffer. Each fast SCA is 1.6 ns long and has a nominal sampling rate of 40 GS/s. The slow SCA is 204.8 ns long and samples at 5 GS/s. Recording of the analog data for each channel is triggered by a fast discriminator capable of multiple triggering during the window of the slow SCA. To achieve a large dynamic range, low leakage, and high bandwidth, the SCA sampling switches are implemented as 2.5 V nMOSFETs controlled by 1.2 V shift registers. Stored analog data are digitized by an external ADC at 10 bits or better.

Specifications on operational parameters include a 4 GHz analog bandwidth and a dead time of 20 microseconds, corresponding to a 50 kHz readout rate, determined by the choice of the external ADC.

Keywords: Waveform-sampling, ADC, Picosecond, ASIC, 4 GHz bandwidth, 65nm CMOS

1. Introduction

1 ps timing resolution is the entry point to signature based searches relying on secondary / tertiary vertices and particle identification. In addition, multiple hit capability and a long time buffer are desirable. An essential requirement for large fast electronics systems is a low power consumption per channel.

With a bandwidth of 4 GHz and a sampling rate of 40 GS/s, the maximum time resolution of an incoming pulse is predicted to be better than 1 ps. The architecture of the chip is designed to provide a high sampling rate with a long buffer as well as multi-hit capability.

The preliminary design of PSEC5 is in TSMC 65 nm process. Simulations predict a maximal power consumption during sampling to be roughly 20 mW/Ch. Each channel consists of four fast and one slow switched capacitor arrays (SCA). This initial version of the chip uses external ADCs. The external ADCs determine the readout rate; there are 1280 sampling capacitors per channel, read out serially once per event. Using a 40MHz ADC per channel, this gives roughly 32 μs of the dead time per event.

The organization of the paper is as follows. We present the functional block diagram in section 2, and fast and slow switched capacitor array (SCA) columns in section 3. We present the source followers we put to achieve higher analog bandwidth in section 4. The layout details are elaborated in section 5. Power consumption and source follower simulation results are shown in section 6.

Process	65 nm TSMC
Signal to Noise Ratio	1000
Sampling Rate	40 GS/s(5 GS/s)
Buffer Length	6.4 ns(204.8 ns)
Analog Bandwidth	4 GHz
Channels	8
Area	2.4 mm^2

Table 1: PSEC5 Specifications.

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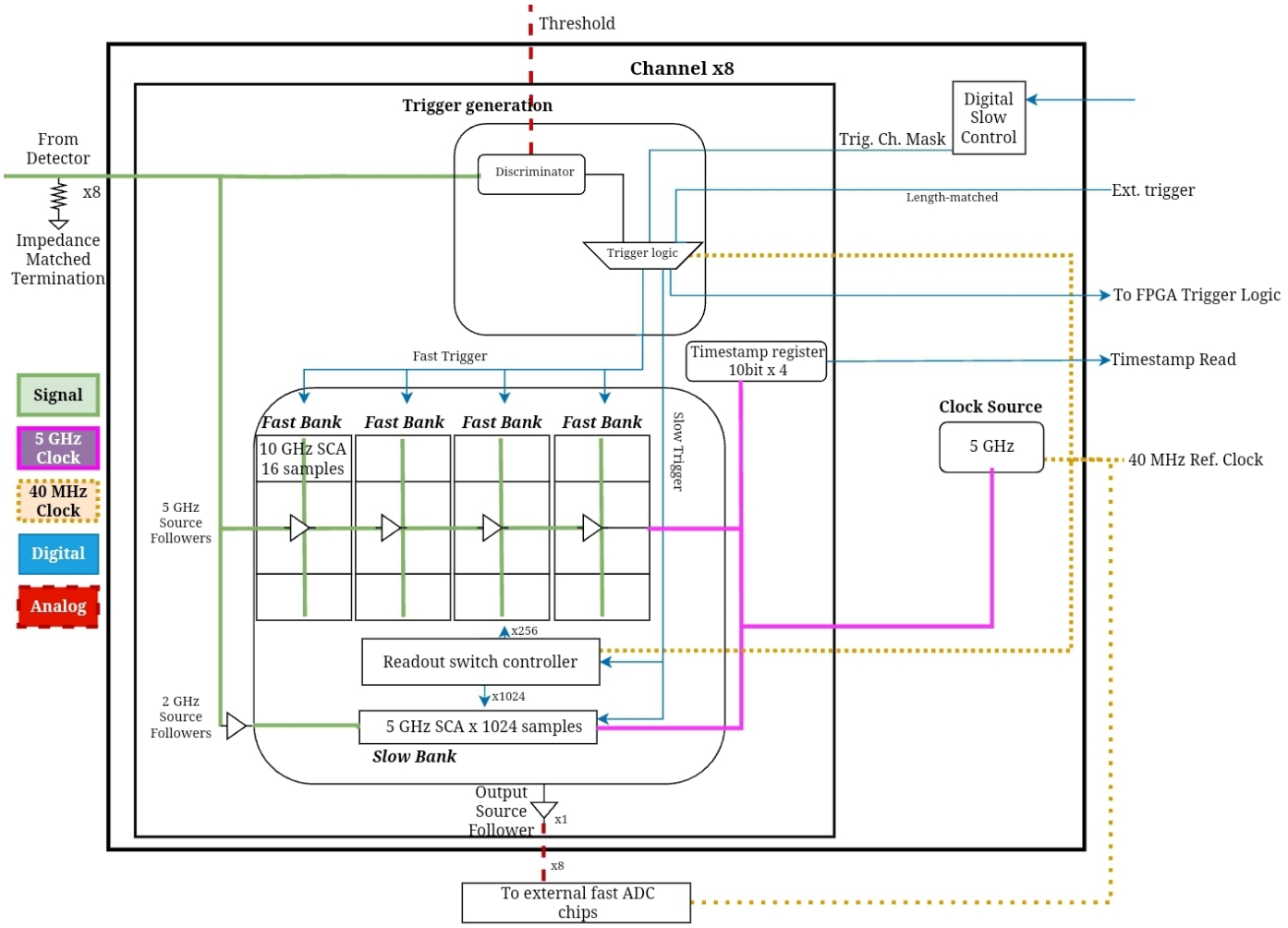

Figure 1: Functional Block Diagram.

2. Block Diagram

The block diagram is shown in Fig 1. Each channel consists of a discriminator that generates fast triggers on the rising edges of the signal.

3. Switched Capacitor Array

Switched capacitor arrays (SCA) consist of sampling capacitors which sequentially sample the voltage of the signal line.

3.1. Fast and Slow SCA

There are four Fast SCAs per channel, 64 samples each. This provides four times 1.6 ns of the sampling window, which can be configured to either run sequentially to capture multiple rising edges of the signal or run as a single longer SCA. The slow SCA is 1024 samples long (204.8 ns) and starts sampling before the fast SCAs. The fast buffers' triggered positions within the slow bank are timestamped. This architecture prevents cumulative timing errors while achieving a long sampling window.

3.2. Voltage Level Shifter

To keep the sampling switch's on-resistance(R_{on}) low, we want to keep its gate voltage high. A 2.5 V I/O nMOS is used as the switch, as the R_{on} of the minimal length 2.5 V I/O device is significantly less than that of the minimal length 1.2 V core device of the same width, given that the gate voltage is 2.5 V and 1.2 V respectively. Also, the input voltage range can be restricted to the bottom half of the drain voltage range of 2.5 V I/O nMOS, obviating the use of a complementary switch is not required. Instead, this design requires a 1.2 V to 2.5 V voltage level shifter (VLS, Fig. 2) for each of sampling switches. The limiting factor in voltage uncertainty is the on-to-off transition time of the sampling switch (t_{off}); the transition time from off to on (t_{on}) is not as important. We adjusted the device widths of the VLS to prioritize reducing the former and achieved 15ps (Best Case) - 22ps (Worst Case) for t_{off}.

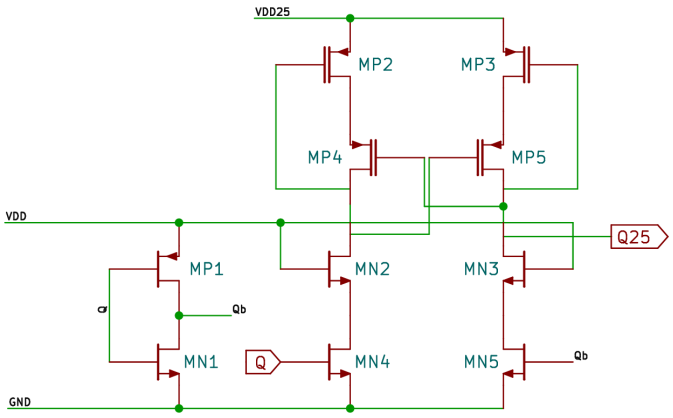

Figure 2: Schematic of the voltage level shifter. All I/O pMOS devices (MP2, MP3, MP4, MP5) are minimum size to reduce t_{off} and power consumption.

3.3. Shift Register

To achieve a nominal 40 GS/s sampling rate of the interleaved SCA, we want each fast SCA column to operate at 10 GS/s. Delivering a 10 GHz clock to a wide area of the chip, however, results in high power consumption. Instead, we used an existing design [1] of a dual edge-triggered flip-flop (Fig. 3) so that we only have to deliver a 5 GHz clock, halving the clock power consumption.

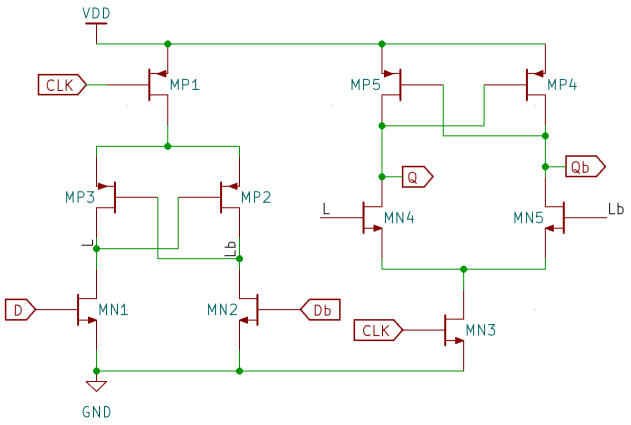

Figure 3: Schematic of a dual edge-triggered filp flop.

4. Signal Paths

4.1. Chip Entry

Wire bonds and electrostatic protection devices (ESD) are the limiting factors of the analog bandwidth.

We employ a capacitively-coupled input to control the DC bias of the signal input (Fig. 4), which affects the analog bandwidth of the sampling switches. The lower the DC bias, the higher the analog bandwidth. Both the input and output source followers have limited voltage ranges, however, so the DC bias is set to approximately 600 mV.

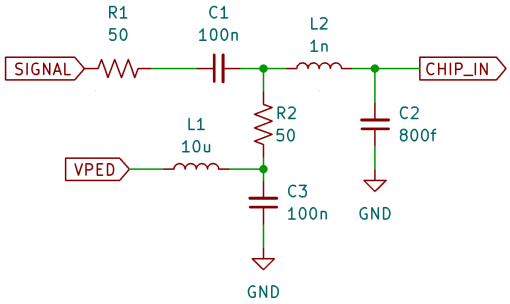

Figure 4: Equivalent Schematic of the wire bond and ESD. R1 represents 50 Ω input. C1, C3, R2, L1 are components placed on board for capacitive coupling. L2 and C2 are the parasitic inductance and the capacitance of the wire bond and ESD combined.

4.2. Main Signal Path

Because of the input inductance, delivering the signal directly to sampling capacitors results in a relatively low analog bandwidth(<2 GHz). We used a single transistor source follower (Fig. 5) to increase this to 4 GHz. The fast SCA columns are interleaved and hence the switching noise from a column may corrupt the capacitor voltage of a different column; we use a dedicated source follower per fast SCA column for the noise isolation. The entire slow bank receives the signal from another source follower since it is sampling at 5 GS/s and does not require a 4 GHz bandwidth.

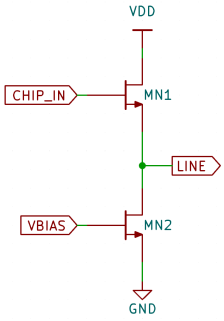

Figure 5: Input Source Follower.

4.3. Readout

Since the sampling MOM capacitors are small (35fF), charge leakage before readout is an issue. We placed two stages of source follower that deliver the signal from the capacitor to the chip output without charge leakage.

5. Physical Layout

The design has been laid out in a 2.4 mm × 1 mm rectangle, and the post-layout simulation to measure the performance is ongoing.

Both fast and slow SCA columns are laid out as 25.5μm×200μm blocks (Fig. 6) with a dedicated clock source, where each column consists of 64 samples. There are 16 slow

SCA columns and 4 fast SCA columns per channel, stacked horizontally. Naturally, slow SCA columns take four times the area of the fast SCA columns.

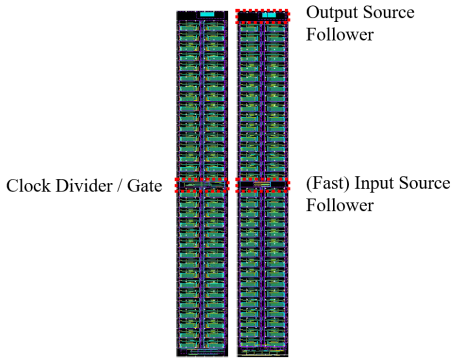

Figure 6: Layout of a slow (Left) and fast (Right) SCA column.

5.1. Clock Gating

Unlike fast SCA columns, only one slow SCA column is active at any given time during sampling. To reduce clock power consumption, we designed a clock gate (Fig. 7) so that a maximum of two slow SCA columns get the clock at any given time. This also doubles as a clock divider, as the slow columns operate at half the frequency of the fast columns.

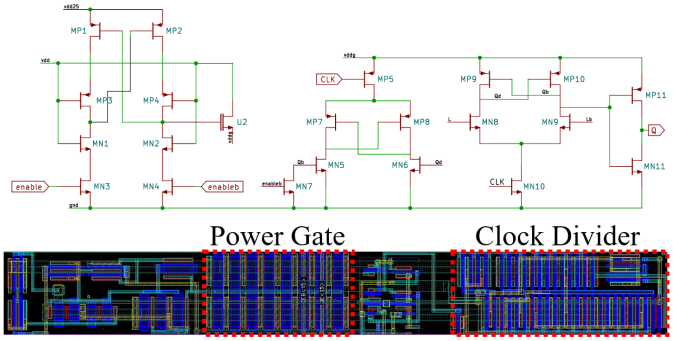

Figure 7: Schematic (Top) and Layout (Bottom) of the clock gate/divider.

6. Simulation Results

6.1. Input Voltage range

The simulation of the complete signal path, consisting of the input source follower, the capacitor, and the output source follower is shown in Fig. 8. The rough linearity of the output is maintained for the input voltage range of 300 mV to 1.1 V. Calibration software may be used to record the curve and reconstruct the input voltage from the output.

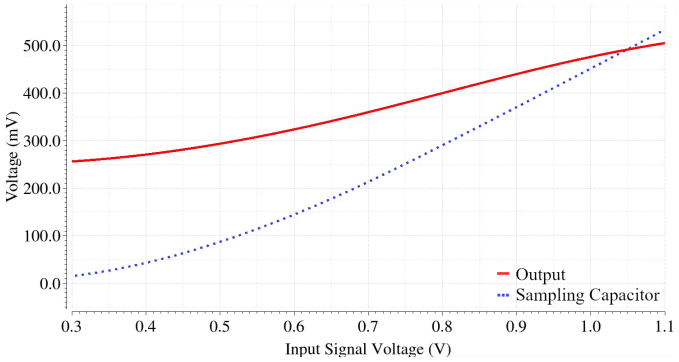

Figure 8: Voltage plot of the source follower chain.

6.2. Power consumption

The average power consumption in various process corners is simulated and shown in Table 2. The input source follower is turned off during the readout, further reducing the power consumption below 1 mW/Ch.

	Worst Case	Best Case
Input Source Follower [mW/Ch]	9.2	4.0
SCA (Sampling) [mW/Ch]	16.6	13.9

Table 2: Power consumption.

7. Conclusion and Current Status

All of the blocks in Figure 1 have been laid out. Currently, we are running post-layout simulations to estimate the voltage and time uncertainty. The intended submission is before the end of 2024.

References

[1] J. Yuan, C. Svensson, New tspc latches and flipflops minimizing delay and power, in: 1996 Symposium on VLSI Circuits. Digest of Technical Papers, 1996, pp. 160–161. doi:10.1109/VLSIC.1996.507754.