A 32-Channel Cryo-CMOS ASIC for SNSPD Biasing and Readout with Picosecond Timing

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***Abstract*—Superconducting nanowire single-photon detectors (SNSPD) are a promising technology for particle detection. Although SNSPDs have demonstrated picosecond timing accuracy, scaling up large arrays has proved challenging. In this work, we introduce a 32-channel cryo-CMOS application-specific integrated circuit (ASIC) that can be tightly integrated with SNSPD arrays. The ASIC is designed to operate at a temperature of 4K and can perform up to 32 simultaneous timing measurements with a root-mean-square (RMS) accuracy of 8.0ps. The ASIC includes on-chip circuitry for externally biasing superconducting devices, low-noise amplifiers for reading superconducting devices, high-resolution time-to-digital converters (TDC) for time-tagging events, and serializers for transmitting data to room-temperature electronics. The ASIC is manufactured in a 22nm FDSOI process and occupies an area of 4.0mm x 1.0mm. The performance of the ASIC was verified using custom cryogenic device models internally developed for the 22nm SOI process. Measurement results will be presented at the conference.**

I. Introduction

Superconducting nanowire single-photon detectors (SNSPDs) are the highest performing detectors for time-resolved single-photon counting from the ultraviolet to the mid-infrared. Over the past two decades, SNSPDs have set records for detection efficiency [1], timing jitter [2], dark count rates [3], and are becoming the detector of choice in many applications, including particle detection [4], [5]. Significant progress has been made towards scaling to large arrays, with [6] demonstrating a thermally coupled imager with row-column readout on a megapixel scale; such multiplexing architectures however present trade offs in terms of maximum occupancy and readout rate. We present a 32-channel ASIC for cryogenic operation at 4K, which provides a modular and scalable solution for the control and readout, with picosecond timing, of large superconducting nanowire arrays.

II. Architecture

Figure 1 presents the overall ASIC architecture. As shown, the system consists of 32 analog readout channels with dedicated TDCs, 5 analog bias channels, a low-jitter PLL, TDC aggregator, digital readout subsystem for serial packet assembly, high-speed differential output drivers, low-speed serial programming interface, and approximately 5 kilobytes of status and control registers.

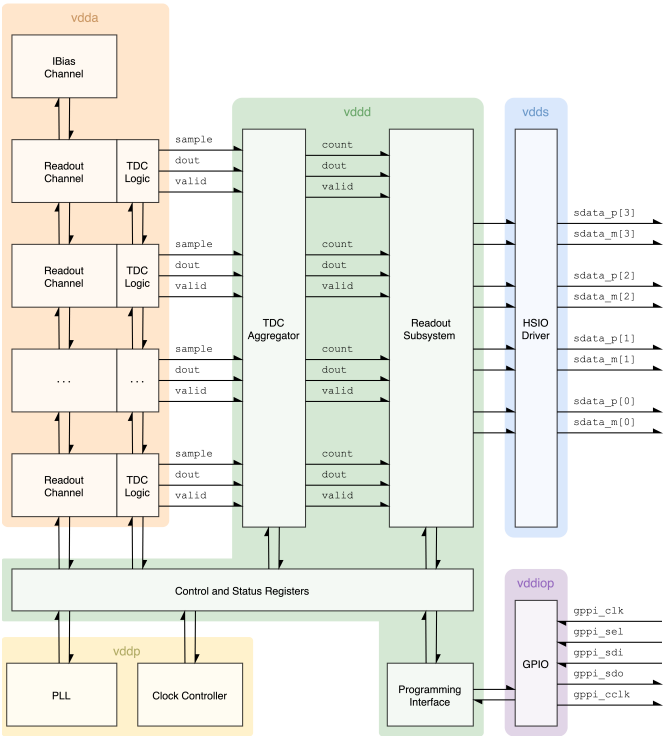

Fig. 1. Overall architecture for readout ASIC.

Each readout channels interfaces directly with superconducting nanowire devices such as SNSPDs or nTron. The channels each feature a programmable current source, $1.0\mu A - 100\mu A$, for external biasing, a programmable impedance, $20\Omega - 1.0k\Omega$, for passively quenching devices after detection, a low-noise amplifier, and a dedicated fine TDC for time-tagging events. Similar to the readout channels, the bias channels feature programmable current sources and programmable impedances, but lack an amplifier and TDC.

The readout channel TDC codes feed into a TDC aggregator. The overall time-tagging system is distributed across the fine TDCs local to each readout channel and a coarse TDC shared across channels. The TDC aggregator manages this coarse TDC and merges the coarse and fine TDC codes into a consolidated timestamp.

The digital readout subsystem assembles the received timestamp into serialization packets. The system operate either in a dynamic priority mode where higher priority channels

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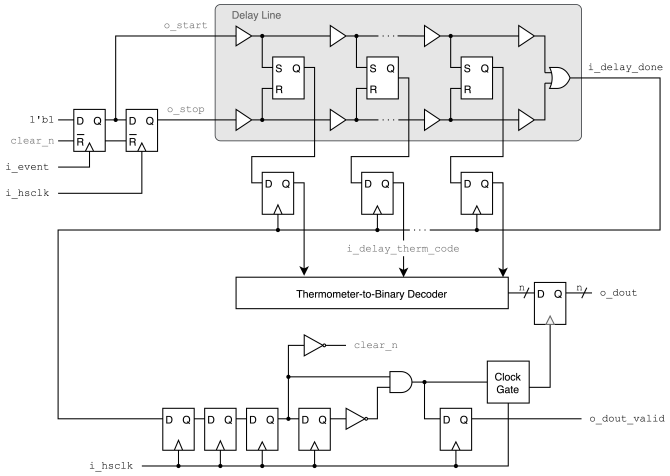

Fig. 2. Representative fine TDC stage schematic.

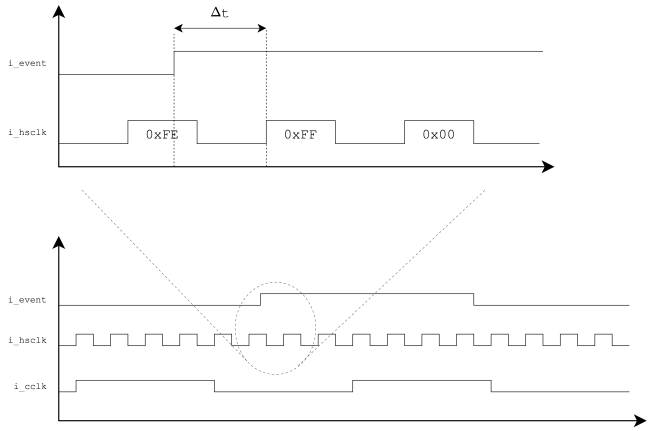

Fig. 3. Representative TDC timing measurement.

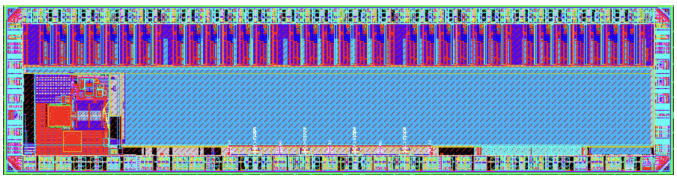

Fig. 4. Screenshot of prototype chip (4×1 mm^2).

transmit timestamps first or in fixed priority mode where channels transmit in a round-robin fashion. Additional diagnostic information such as the event hit patterns, parity checks, and various configuration data can be injected into the output data packets. The 4 high-speed drivers transmit the serialization data. Operating at a modest 1.0 GHz, these output drivers are compatible with the LVDS receivers found on many commercial FPGAs.

III. Time-Tagging

The overall TDC is a distributed system consisting of fine TDC stages operating locally within each readout channel and a coarse TDC stage shared across channels. A representative schematic for the fine TDC is shown in figure 2. As shown, the fine TDC leverages a Vernier delay line to measure the time difference between a start signal representing a detected event and a reference stop signal generated by the low-jitter PLL. The TDC further includes a thermometer-to-binary decoder and self-timed reset circuitry to re-arm the delay line after measurements are made.

Figure 3 illustrates a TDC timing measurement. A fine TDC measures the time difference, Δt, between the RISING edges of an event, i_event, and the next high-speed clock pulse, i_hsclk. The coarse TDC continuously counts the number of RISING edges in the high speed clock, i_hsclk. The overall timing measurement is constructed by concatenating the fine TDC measurement with the coarse TDC counter value. An additional reduced rate counter clock, i_cclk, also marks rollover events within the coarse TDC counter.

TABLE I
Performance Targets

Specification		Target	Units
Operating Temperature		4.0	K
Overall Timing Error	rms	8.0	ps
Amplifier Jitter	rms	5.0	ps
TDC Accuracy	lsb	5.0	ps
Clock Distribution Jitter	rms	5.0	ps
PLL Jitter	rms	75.0	fs
Overall Power	avg	114.0	mW
Single Readout Channel Power	avg	1.6	mW
Single Bias Channel Power	avg	0.13	mW
PLL Power	avg	20.0	mW
Digital Power	avg	16.0	mW
Single SerDes Lane Power	avg	6.5	mW

IV. Conclusion

The ASIC was manufactured in a 22nm FD-SOI process and occupies an area of $4.0mm$ x $1.0mm$. The ASIC operates at 4K with the performance verified using using custom cryogenic models developed from cryogenic device measurements. The overall timing accuracy of the system is targeted at $8.0ps$ with a power budget of $114.0mW$. A further breakdown of the power and timing budgets are provided in Table I. Figure 4 presents a screenshot of the submitted design. The ASIC has already been fabricated and testing results will be reported at the conference.

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