Achieving Single-Electron Sensitivity at Enhanced Speed in Fully-Depleted CCDs with Double-Gate MOSFETs

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We introduce a new output amplifier for fully-depleted thick p-channel CCDs based on double-gate MOSFETs. The charge amplifier is an n-type MOSFET specifically designed and operated to couple the fully-depleted CCD with high charge-transfer efficiency. The junction coupling between the CCD and MOSFET channels has enabled high sensitivity, demonstrating sub-electron readout noise in one pixel charge measurement. We have also demonstrated the non-destructive readout capability of the device. Achieving single-electron and single-photon per pixel counting in the entire CCD pixel array has been made possible through the averaging of a small number of samples. We have demonstrated fully-depleted CCD readout with better performance than the floating diffusion and floating gate amplifiers available today, in both single and multisampling regimes, boasting at least six times the speed of floating gate amplifiers.

Since their invention, Charge-Coupled Devices (CCDs) have been the preferred detectors in ground and space telescopes, as well as in laboratory photon imaging applications [1]. Fully-depleted thick CCDs have been developed at Lawrence Berkeley National Laboratory (LBNL) to achieve high quantum efficiency in the red and near-infrared range [2–4]. These CCDs are three-phase, p-channel devices, featuring a triple polysilicon gate structure. In order to fully-deplete the thick substrate at a reasonable voltage, they are fabricated in high resistivity n-type silicon [3, 5]. Depending on the application, they have been fabricated with thicknesses exceeding 200 μm, segmented into pixels of $15 \times 15\,\mu\text{m}^2$ and in different array formats [6]. To minimize dark current, these CCDs are operated at cryogenic temperatures, typically -140 °C. These p-channel CCDs have shown significantly more radiation tolerance than n-channel CCDs, making them more suitable for space-based applications [7, 8]. In the remaining text, we will refer to these CCDs simply as FDCCDs.

The development of FDCCDs has been driven by their application in detecting and conducting follow-up spectroscopy of high redshift astronomical objects. Examples of instruments utilizing FDCCDs include the Dark Energy Camera (DECam) [9, 10], the Baryon Oscillation Spectroscopic Survey (BOSS) [11], and the more recent Dark Energy Spectroscopic Instrument (DESI) [12]. These FDCCDs, characterized by their low readout noise and considerable active silicon mass, have also found application as competitive direct detectors in dark matter searches [13–15] and the coherent elastic neutrino-nucleus scattering [16, 17]. For dark matter searches, where active silicon mass needs to be as large as possible, FDCCD are fabricated in 725 μm thick, 20 kΩ.cm resistivity substrate, and can be fully depleted with 70 V [18]. Today, LBNL and MIT Lincoln Labs (MIT-LL) are leaders in making FDCCDs [19]. Also, relatively thick fully-depleted n-channel CCDs, $\sim$100 μm, have been developed by commercial vendors for the Large Synoptic Survey Telescope (LSST) [20, 21].

Historically, the output amplifier of choice for FDCCDs has been a floating diffusion amplifier (FDA) [3]. In the case of the Skipper-CCD, the FDA was replaced by a floating gate amplifier (FGA) to enable the non-destructive readout (NDR) of the charge packet, or the so called "skipper" amplifier [6, 22]. After averaging the pixel samples, it is possible to achieve a sub-electron readout noise of $0.068\,\text{e}^-_{\text{rms}}$/pix, reaching the absolute theoretical limit of silicon of 1.1 eV in energy threshold, allowing single-electron and single-photon sensitivity per pixel [23]. The Sub-Electron Noise Skipper-CCD Experimental Instrument (SENSEI), using a single Skipper-CCD detector, 675 μm thick, has achieved world-leading sensitivity for a large range of sub-GeV dark matter masses [24–26]. The OSCURA experiment will lead the search for low-mass dark matter particles using thousands of Skipper-CCD [27, 28]. Skipper-CCD are also being explored for terrestrial astronomy [29]. CCDs are undeniably essential in advancing scientific exploration.

The FGA operates by dumping the pixel charge onto the bulk side of a MOS capacitor in the CCD buried channel to modulate the gate voltage of an output transistor. In addition to the MOS capacitance, several stray capacitances are added to the floating gate (FG) limiting the stage sensitivity. The overall FG capacitance, combined with the resistance of the relatively large polysilicon connection between the MOS capacitor and the output transistor gate, constrains the time response of the FGA and consequently the maximum pixel readout rate [30]. The limited sensitivity of the FG, coupled with the multiple sampling operations, significantly increases

This manuscript has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.

the CCD readout time making it a limiting factor in various applications [31].

Another FDCCD with photon counting output and higher pixel readout rate than Skipper-CCDis the Electron Multipling CCD (EMCCD). In an extended serial register electrons are accelerated by an electric field and through impact ionization the signal is amplified. They have a limited dynamic range, and have shown degradation due to the gain process, limiting the device lifetime [32]. Due to the high radiation tolerance, both Skipper-CCD and EMCCD are being evaluated as detectors for future space missions in exoplanet search, where single-photon sensitivity is required [33].

In order to overcome the readout noise and speed limitation of FDA and FGA, in this Letter we introduce the first output amplifier for FDCCDs based on a double-gate MOSFET. We will refer to our amplifier as SiSeRO, an abbreviation for Single-Electron Sensitivity Readout, and SiSeRO-CCD for the CCD itself. We specifically designed the SiSeRO considering its integration and high-voltage compatibility with LBNL fully-depleted p-channel CCDs. For a more comprehensive description of the device design, please refer to [30].

Double-gate MOSFETs were originally proposed by Brewer for the readout of n-channel thin CCDs [34]. The amplifier consists of a MOSFET integrated into the CCD buried channel. In this configuration, the CCD channel is junction-coupled to the MOSFET channel, resulting in high-sensitivity modulation of the MOSFET current by the signal charge in the CCD channel [35–37]. Since the signal charge is directly coupled to the MOSFET channel, as reported in [38], this design is the most optimal for any charge detector. Currently, they are being evaluated for the readout of modern n-channel thin CCDs [39–41]. In addition to its high sensitivity, another advantage of this amplifier is its NDR capability. Using a similar sense node architecture Depleted Field-Effect Transistors (DEPFET) detectors, which are single p-MOSFET transistors in an n-type depleted thick substrate, have demonstrated a readout noise of $0.18\,e^-_{rms}$/pix after averaging 300 samples in a miniarray of 4×4 pixels [42, 43].

Figure 1 illustrates both a top-view and cross-sectional schematic of the SiSeRO-CCD output stage. Essentially, it is an n-type MOSFET integrated in the CCD-line, that has the CCD p-channel under the transistor n-channel. This p-n combination creates a junction coupling between both channels. In contrast to the FGA, the charge is directly deposited onto the junction on the bulk side of the transistor, where it directly modulates the junction potential. This change in junction potential modulates the transistor's channel conductance, and depending on the transistor support circuitry, results in either a measurable change in current or voltage. Therefore, the holes deposited into the junction act as an internal type gate (IG) to the common channel of the nMOSFET. By manipulating the gates voltages the charge can be transferred back to the SG to repeat the process and start the acquisition of another sample.

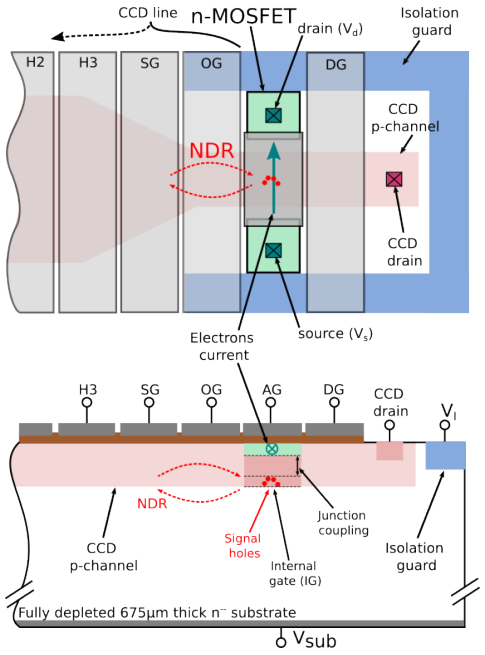

FIG. 1. Schematic top view and cross-section diagram of the SiSeRO-CCD output amplifier. The SiSeRO amplifier consist of a n-type MOSFET transistor integrated into the CCD-line. On the transistor's bulk side, a junction coupling is formed between the transistor n-channel and the CCD p-channel. Due to the direct coupling, high sensitivity and low noise are achieved. Moreover, the charge is sensed non-destructively enabling respective multiple sampling for readout noise reduction.

In order to enable the operation of the n-type MOSFET in the fully-depleted n-type CCD substrate, an isolation guard was designed [30]. As is shown in Fig. 1 it consist of a p-type implant partially surrounding the output stage. Without the isolation guard, an electron current appears between the CCD backside substrate contact and the MOSFET source/drain terminals, disabling the full-depletion of the CCD. In the nMOSFET bulk-side, a potential well (PW) is formed in the junction between the CCD p-channel and the n-type substrate. The well voltage depends on the transistor biasing point and the acceptor concentration in the junction [30]. Another important design aspect was a local p-type implant in the transistor bulk side, depicted as a dark pink region in the bottom diagram of Fig. 1. This implant creates the PW within the CCD-line well's range after transistor biasing, allowing for the transfer of charge into and out of the IG from the CCD line. As observed in Fig.1, the CCD-line is tapered in order to reduce the nMOSFET area to achieve a small junction capacitance and increase the sensitivity. It is important to mention that the integration of the SiSeRO amplifier does not require modifications of the CCD pixel array; therefore optical

characteristics and performance metrics within the array are not affected, such as dark current, quantum efficiency, and radiation tolerance. Moreover, it does not introduce any limitation on the pixel array size. The SiSeRO-CCD was fabricated at MIT-LL, using the fabrication process of triple-poly CCDs, in arrays of 1278×330 pixels in a 725 μm thick substrate, with an output amplifier on each corner for split readout and with a W/L nMOSFET of 2.5/5 μm. At the short edges of the array, a serial register is placed to shift the charge using three phases (H1, H2, and H3) towards the edges where the SiSeRO amplifiers are located.

The SiSeRO-CCD was packaged and connected via wire bonding to a 20 inches long flex cable, which serves to transmit signals into and out of the vacuum chamber. Inside the vacuum chamber, the device was cooled down to -140C using a cryocooler. The Low Threshold Acquisition Controller (LTA) was used for the evaluation of the device. Originally developed for Skipper-CCDs, the LTA low-noise biasing voltage supplies were adjusted with external hardware to properly bias the SiSeRO. The LTA can be programmed to generate a specific sequence of signals for manipulating the CCD gates. Additionally, it digitizes the video signal and performs in the FPGA the correlated double sampling (CDS) using a double slope integration (DSI) [44].

As previously mentioned, the signal holes in the IG modulate the nMOSFET drain-source current. To convert the current variations into voltage signals, a transimpedance amplifier circuit was implemented using the ADA4817 operational amplifier (OA), chosen for its very low input current noise. The OA maintains the nMOSFET drain at a constant potential, thereby preventing any impact of the flex cable's stray capacitance on the readout speed. This biasing and readout circuit ensures the highest speed and performance readout [45].

To enable multi sampling operation and achieve the single-electron sensitivity regime, a specific operating sequence had to be developed for the SiSeRO-CCD. Figure 2 depicts the developed operating sequence. It has been developed as follows: At t_0, the holes are drained from the IG to the CCD drain by lowering the dump gate (DG). At t_1, the horizontal phase H3 is raised to transfer the pixel's holes into the summing gate (SG) well. During this time, the pedestal integration takes place for a duration of T_{CDS}. At t_2, the SG is raised to transfer the holes over the output gate (OG) into the IG. The well voltage of the IG depends on the nMOSFET biasing voltages. Higher drain and gate voltages would increase the PW voltage [30]. Consequently, the charge transfer from the SG into the IG is largely influenced by the biasing point. To mitigate this dependence, we strategically turn off the nMOSFET (by setting AG to 0V) during this operational phase. Together with the additional local p-type implant, this ensures that the IG well voltage is lower than the OG well voltage, creating a sufficient voltage gradient to fully transfer the signal holes from the SG into the IG. At t_3, with the holes in the IG, both SG and AG are restored to initiate the integration of the signal level. We observed that the SG and OG are strongly capacitively coupled to AG. As a result, the voltage levels on both gates can modify drain-source current (I_{ds}) and consequently the gain. Therefore, they are maintained in the same state during both the pedestal and signal integration periods to ensure equal gain. The pixel charge value is determined by the difference between the signal and pedestal levels. At t_4, the OG is set low to transfer the holes back into the SG, repeating the process for taking another sample of the pixel charge. Figure 2 provides the high and low voltage levels of each signal as a function of time.

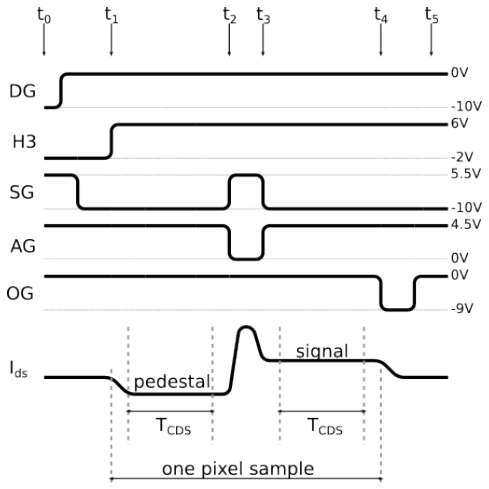

FIG. 2. Operating sequence developed for the SiSeRO-CCD output stage. At the bottom, there is a representation of the nMOSFET drain-source current (I_{ds}). Between t_1 and t_2, the IG is empty of signal holes and the pedestal level integration takes place for T_{CDS}. Between t_2 and t_3, the SG is pulled up and the nMOSFET is turned off to ensure the transfer of the signal holes into the IG. The signal level integration takes place between t_3 and t_4. At t_4, OG is pulled down to transfer the charge back into the SG to repeat the process to take another pixel sample.

The isolation guard was biased with 8 V, which was predetermined through computer simulations [30]. The nMOSFET was operated at a constant biasing point. In order to minimize impact ionization noise, the drain-source voltage (V_{ds}) was biased to 1 V with the source at 0V [30]. The nMOSFET is operating in enhancement mode, with a threshold voltage of 2.4 V. A maximum sensitivity of $1.54\,nA/e^-$ was achieved with $V_{gs} = 4.5V$. At this operating point, the source-drain current was 70 μA. This is the highest sensitivity ever achieved with a double-gate MOSFET. Typically DEPFETs has a sensitivity of $\sim 0.3\,nA/e^-$ [42]. In the case of thin n-type CCD readout, $0.7\,nA/e^-$ have been reported in [40].

Images of cosmic-ray muons and x-rays were acquired

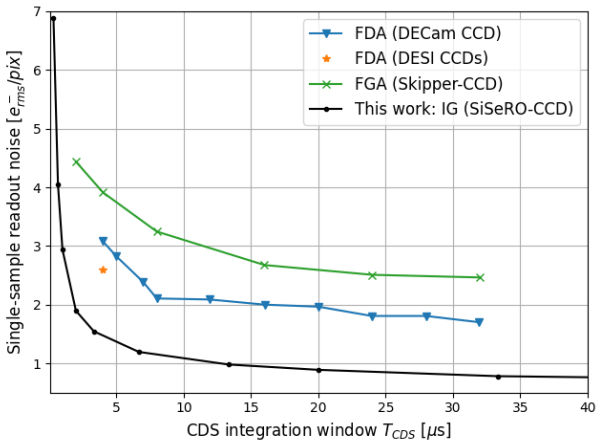

FIG. 3. Single-sample readout noise versus the correlated-double sampling (CDS) integration time T_{CDS}. As observed, the SiSeRO-CCD consistently achieves lower readout noise throughout the entire integration time range, highlighting the advantage of its internal gate (IG) sensing structure over fully-depleted thick CCDs with FDA [3, 6] or FGA [44] output structures.

with the SiSeRO-CCD. The achieved single-sample pixel readout noise at different CDS integration times (T_{CDS}) is shown in Fig. 3. A readout noise of 2.72 e^-_{rms}/pix is achieved for a T_{CDS} of 1 μs. Over 20 μs, the noise decreases down to 1 e^-_{rms}/pix and can reach a floor of 0.74 e^-_{rms}/pix at 100 μs. For comparison, results achieved in FDCCDs with FDA and FGA output stages are also presented. The FDA results are obtained from the Dark Energy Camera (DECam) CCDs [10], as extracted from [3]. Additionally, the result from the Dark Energy Spectroscopic Instrument (DESI) CCDs is included [6], that have an optimized FDA output structure [46, 47]. The FGA case corresponds to the Skipper-CCD as extracted from [44]. As observed, the SiSeRO achieves a lower readout noise over the entire integration integration time range compared to the other output structures.

Figure 4 shows the pixel charge distribution of an image acquired with T_{CDS} of 1 μs and 33.3 μs, after averaging different number of pixel samples (N_{spl}). As observed, single-electron resolution is achieved in both cases, and the unprecedented readout noise of 0.03 e^-_{rms}/pix is achieved for 33.3 μs and 1000 samples. Charge quantization has been also observed up to 600 e^-, showing single-electron sensitivity in a wide dynamic range. As a drawback, for long pixel readout times, that is proportional to N_{spl} and T_{CDS}, impact ionization holes produced by the nMOSFET electron current, can fall into the internal gate during the sampling operation [30]. This affect the measurement, as can be observed in the case of 33 μs and 1000 samples of Fig. 4, resulting in non-zero pixel count between the discrete electron levels. This is due to a single carrier from an impact ionization event collecting in the sense node at some point during the readout.

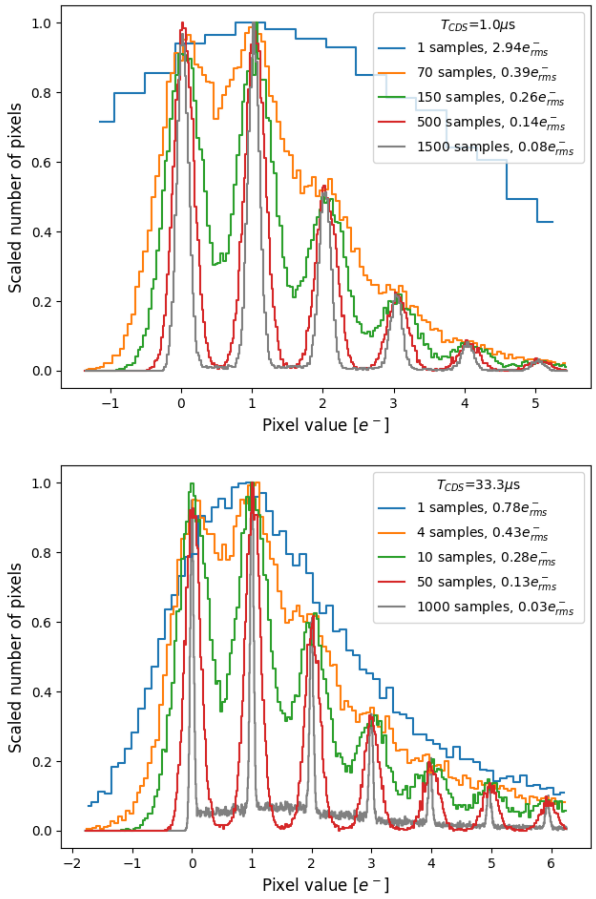

FIG. 4. Single pixel distribution of an image acquired with T_{CDS} of 1.0 μs (top) and 33.3 μs (bottom). The charge quantization starts to be revealed as the number of averaged samples increases, and single-electron charge resolution is achieved in both cases with the SiSeRO-CCD.

Fig. 3 shows the achieved readout noise after averaging different number of samples for different T_{CDS}. If the pixel samples are affected by uncorrelated noise, the readout noise decreases in proportion to the square root of the number of averaged samples [23]. As observed in Fig. 5, this is the case for T_{CDS} of 1 μs. As discussed in [22], with an increase in pixel readout time, the transistor flicker noise introduces correlation among the samples. This correlation effect is observable in Fig. 5 for longer T_{CDS}, where the achieved readout noise deviates from the behavior exhibited by uncorrelated samples. The minimum achieved readout noise has been 0.021 e^-_{rms}/pix for 86.7 μs of T_{CDS} and 2000 samples.

With the LTA readout system, 20 μs for signal manipulation was required per sample during the multi-sampling operation. Therefore the pixel readout time is given by $(2 \times T_{CDS} + 20\mu s) \times N_{spl}$. Fig. 6 shows the achieved pixel readout noise versus the pixel readout time for different values integration time. As observed, the mini-

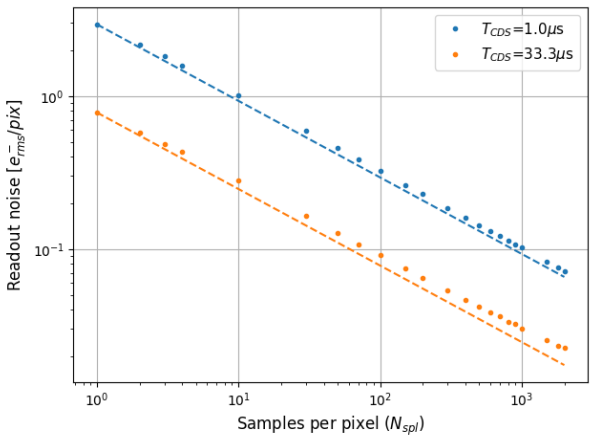

FIG. 5. SiSeRO-CCD readout noise versus numbers of averaged samples per pixel (N_{spl}). The dashed lines represent the $1/\sqrt{N_{spl}}$ projection based on single sample readout noise, as expected from uncorrelated samples.

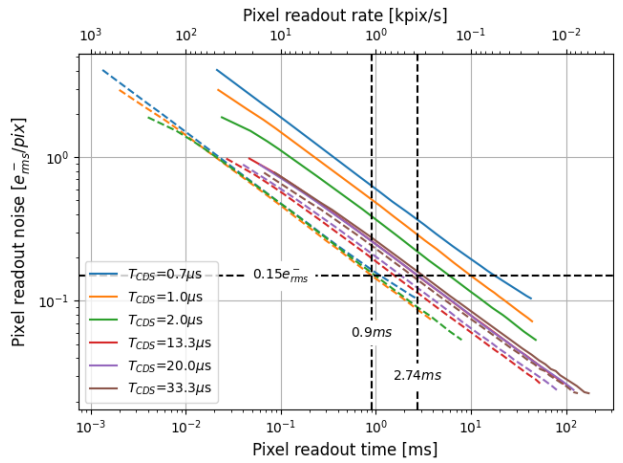

FIG. 6. SiSeRO-CCD pixel readout time. A readout noise of 0.15 e^-_{rms}/pix is achieved in a pixel readout time of 2.74 ms (365 pixels/sec) using a T_{CDS} of 13.3 μs. The minimum possible readout time, considering two times T_{CDS} as the pixel sample readout time (dashed lines), is 0.9 ms (1.1 kpixels/sec) for a T_{CDS} of 1 μs.

mum readout time is achieved with a T_{CDS} of 13.3 μs, reaching 0.15 e^-_{rms}/pix in 2.4 ms (365 pixels/sec), which is six times faster than the Skipper-CCD [23]. In Fig. 6, the dashed lines represent the readout speed limit that could be reached by reducing the readout controller signal manipulation time down to the ideal 0 μs. As observed, the minimum readout time is achieved with a T_{CDS} of 1 μs, resulting in a readout noise of 3 e^-_{rms}/pix at 500 kpixels/sec and 0.15 e^-_{rms}/pix at 1.1 kpixels/sec.

With further optimization the device performance can be improved. One possible design optimization is to develop a buried-channel nMOSFET, implanting the transistor n-channel as described in [30], in order to further reduce the noise floor of 0.74 e^-_{rms}/pix for long integration times where flicker noise is dominant. Another design optimization can be to reduce the area of the p-type local implant in order to enhance the coupling between the channels, and to reduce the coupling of the IG to the nMOSFET source and drain diffusion where a loss of sensitivity occurs [30]. It is worth note that already developed techniques for the Skipper-CCD are also applicable for the SiSeRO-CCD. For example, smart readout of the array, where only a subset of the array is readout taking several samples for noise reduction, can be combined with the SiSeRO-CCD to boost the array readout speed [31]. Multiplexed readout architectures with analog averaging developed for the readout of large arrays are also suitable for this detector [48].

In summary, we have demonstrated that double-gate MOSFETs serve as highly sensitive charge amplifiers for fully-depleted CCDs, setting new records in readout noise and speed while achieving single-electron sensitivity. An unprecedented level of sensitivity and low readout noise at shorter pixel readout times, compared to traditional FDA and FGA outputs, is attainable. Furthermore, it demonstrates single-electron sensitivity even after averaging relatively few samples. In future work, we will continue to improve performance by optimizing the device itself, the readout electronics, and characterizing its performance in specific application cases.

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