A self-certifying FPGA based pixel readout chip test system for CMS ETL upgrade

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Abstract: A flexible self-certifying pixel readout test system for testing the Endcap Timing Read-Out Chip (ETROC) has been developed for the CMS MIP Timing Detector (MTD), part of the upgrade for the HL-LHC. The system includes an FPGA-based (Xilinx KC705) test system that can take data from an emulator or up to four ETROC boards in telescope mode. A python based DAQ system simplifies configuration, calibration, and testing of the chips. **The system provides an efficient & reliable solution for testing ETROC** (ETROC2 since April 2023 with 16x16 pixels, full-size, full functionality prototype) and can be extended to other readout chips with similar architecture (AIDA integration is currently being explored).

ETROC2 Heterogeneous Testing Roadmap Enabled by Flexible Chip Testing System