

Design and construction of Cosmic Muon Veto for the mini-ICAL detector at IICHEP, Madurai

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A 51-kiloton magnetised Iron Calorimeter (ICAL) detector, using Resistive Plate Chambers (RPCs) as active detector elements, aims to study atmospheric neutrinos. A prototype - 1/600 of the weight of ICAL, called mini-ICAL was installed in the INO transit campus at Madurai. A modest proof-of-principle cosmic muon veto detector of about 1 m×1 m×0.3 m dimensions was setup a few years ago, using scintillator paddles. The measured cosmic muon veto efficiency of 99.98% and simulation studies of muon-induced background events in the ICAL detector surrounded by an efficient veto detector were promising. This led to the idea of constructing a bigger cosmic muon veto around the mini-ICAL detector. Details of the design, fabrication, quality control and construction of the detector including the electronics, trigger and DAQ systems planned will be briefly presented.

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1. Introduction

A 51-kiloton magnetised Iron Calorimeter (ICAL) detector, using Resistive Plate Chambers (RPCs) as active detector elements, aims to study atmospheric neutrinos. It will be the flagship experiment at the India-based Neutrino Observatory (INO) which is proposed to be housed in a cavern at the end of a 2 km tunnel in a mountain near Pottipuram (Tamil Nadu) [1]. A prototype - 1/600 of the weight of ICAL, called mini-ICAL was installed in the INO transit campus at Madurai, in order to gain experience in the construction of a large-scale electromagnet, and in order to study the detector performance and test the ICAL electronics in the presence of a fringe magnetic field. The 4 m×4 m×1.1 m mini-ICAL magnet with 11 iron layers, and 2 m×4 m×1.1 m active detector using 20 RPCs which is housed in the central region of the magnet, have been in operation for about 4 years and collecting cosmic muon data. A modest, proof-of-principle cosmic muon veto detector (CMVD) of about 1 m×1 m×0.3 m dimensions was set up a few years ago, using scintillator paddles [2]. The measured cosmic muon veto efficiency of ~99.98% and simulation studies of muon induced background events in the ICAL detector surrounded by an efficient veto detector were promising enough to perform simulation studies for a shallow depth ICAL detector, surrounded by a 99.99% efficient CMVD, placed at a depth of 100 m [3]. This led to the idea of constructing a bigger cosmic muon veto around the mini-ICAL detector.

2. Design of the veto detector

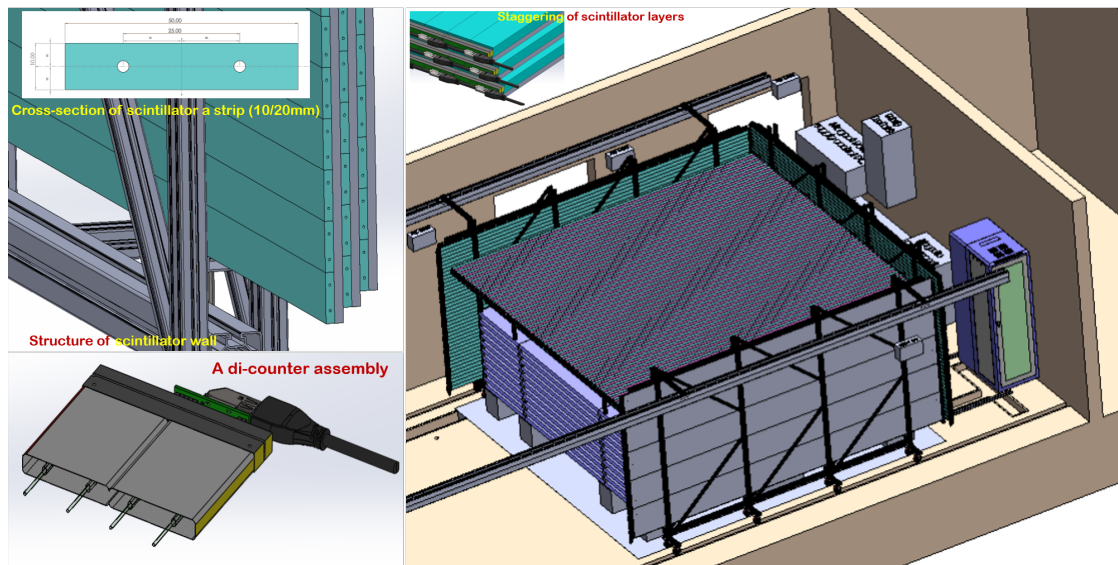


Figure 1: A collage of schematics drawings showing the overall structure of the cosmic muon detector around the mini-ICAL, staggering of scintillator layers, a view of the support structure for the side veto walls and the di-counter readout.

The veto walls around four sides and top of the mini-ICAL will be built using three staggered (by 15 mm) layers of extruded scintillator strips (donated by Fermilab) [4]. Strips of 4400-4700 mm in length, 50 mm wide and 10 or 20 mm thick will be used to construct the veto shield that aims

at 99.99% efficiency to tag cosmic muons. Double-clad WLS fibres of 1.4 mm in diameter (from Kuraray) are inserted into two extruded fibre holes along the length of the strip and separated by 25 mm to collect the light signal. Hamamatsu SiPM's of 2 mm×2 mm active area collect the light on both sides of the fibres. About 750 strips, about 7 km of fibre and 3000 SiPM's are going to be deployed. All the five veto walls/stations are designed to be movable from their designed positions, providing service access to the mini-ICAL inside (see Fig. 1).

3. Veto detector requirements

The main requirements of the veto detector are measurement of charge, position, relative arrival time of the SiPM signals on trigger from mini-ICAL trigger. An event marker is used to correlate the veto detector event data with that of the mini-ICAL data. For the charge measurement, a dynamic range of 100 pC with a resolution of 20 fC and single photo-electron charge of about 100 fC are specified. A resolution of 100 ps is sufficient for the time measurement. Closed loop gain/biasing control for every SiPM or Di-Counter as well as in-situ calibration using LED pulses or noise signals are essential for stable and reliable detector operation. Extensive characterisation and calibration studies were carried out on the main elements of the cosmic muon detector - namely the extruded scintillator strips, fibre and SiPMs. The studies were carried out using LED pulses, a ²²Na radioactive source, as well as cosmic ray muons. Using these studies, we obtained a single PE avalanche charge: 0.242 pC. The typical PE yields obtained for 10/20 mm thick scintillators are 34/57, while the typical signals for cosmic ray muons are 8.33 pC (10 mm) and 13.82 pC (20 mm). Using time-of-flight measurement across the length of the scintillator strip, a position resolution of 9.18±2.27 cm was obtained across scintillator strip.

4. Detector design

CMVD will comprise of Veto walls on three sides and the top of the mini-ICAL and will be built using pre-fabricated di-counters, which are essentially two extruded scintillators strips (donated by Fermilab) glued sideways. The top layer (the roof) of mini-ICAL will have four layers of scintillator strips and standing Veto walls on three sides (left, right, posterior) will each have three layers of scintillator strips. The layers of each veto wall will be staggered (by 15 mm) so as to minimize the effect of inter-strip gaps. There will be no anterior veto wall, so as to allow for maintenance of the mini-ICAL detector. Strips of 4500-4700 mm in length, 50 mm wide and 10 or 20 mm thick are used to construct the veto shield that aims at 99.99% efficiency to tag cosmic muons. Double clad WLS fibres ~1.4 mm in diameter (from Kuraray) are inserted into two extruded fibre holes along the length of the strip and separated by 25 mm to collect the light signal. One end of the four fibres from each of the di-counter are readout by one SiPM assembly as shown in Fig. 2. Hamamatsu SiPMs of 2 mm×2 mm active area will collect the light on both sides of the fibres. In total, 712 strips, 6.6 km of fibre and 2848 SiPMs will be used. All the four veto walls/stations are designed to be movable from their designed positions, thus enabling better service access to the mini-ICAL. The fibres are passed through the fibre guide block which is mounted on the di-counter face using sleeves and sleeve pins. A neoprene gasket cushions the fibres to terminate properly on the active windows of the SiPMs which are placed in the SiPM mounting block. The

SiPMs are actually individually mounted on tiny SiPM carrier boards “mouse-bite” boards, which themselves are locked in fixed slots in the SiPM mounting block. Finally, the counter mother board that houses the SiPM bias voltage services, the ambient parameter sensors, calibration LED source and other services is mated to the SiPM mounting block using plastic screws. The SiPM signals, power supplies, the LED drive voltage etc., are carried between the detector readout assembly and backend electronics via an HDMI connector mounted on the counter mother board.

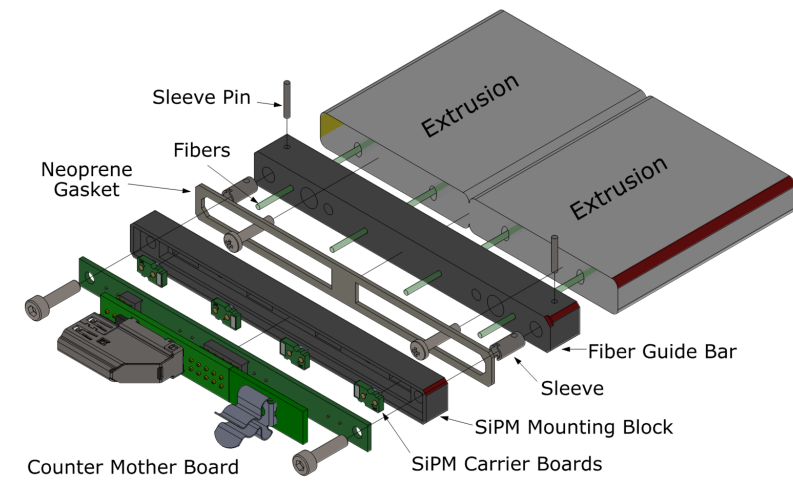


Figure 2: An exploded view of various components of the di-counter detector readout. Two such readout modules are used for readout of either ends of a di-counter.

Detector production

Before the actual production of detector modules, all their main components such as extruded plastic scintillators, WLS fibres and SiPMs are thoroughly characterised for our application as well as tested for production quality control. The CMV detector will require 736 scintillators to shield the mini-ICAL detector, and will require 2912 SiPMs for the readout. The design goal for the cosmic muon veto efficiency of the CMV is $>99.99\%$ and fake veto rate less than 10^{-5} . Hence, every SiPM used in the detector needs to be characterised to satisfy the design goal of the CMV. A large-scale testing system was developed, using an LED driver, to measure the gain and noise rate of each SiPM, and thus determine its breakdown voltage (V_{br}) and optimum operating over voltage (V_{ov}) [5]. The scintillators are stacked vertically in a fixture one by one, and are glued in order to make four Di-Counters. The Di-Counters are cut to required lengths. The Di-counter are polished on either ends to get a smoother surface. Both ends of the Di-Counter are coated with Titanium Di-Oxide paint to maximise the internal reflection of light. Two holes are drilled on the cross-sectional ends for mounting the Fibre Guide bar (FGB). The Di-Counters are again stacked to insert WLS fibres in the fibre holes from one end. Glue is poured in the guides of the FGB and carefully inserted in such a way the all the 4 fibres pass through the guide filled with glue and project out. The FGBs are then firmly mounted on their location. After the Di-Counter assembly is cured, extra portions of the fibre are cut and the FGB assemblies are polished. One tile is made up of four Di-Counters, which are glued together on a 10 mm honey comb panel. The panel is placed on the table and glue is poured. The Di-counters are placed on the panel and left the assembly for curing. The whole tile

assembly is wrapped with Teddlar paper. The tile is then inserted in an insulation sleeve and a hot air gun is used to shrink the sleeve in such a way that it is tidily shrunk all over the tile. Fig. 3 is a collage of the tile production process.



Figure 3: Various steps involved in the production of di-counters and detector tile assemblies.

Detector Readout

The SiPM signals are amplified using a trans-impedance stage of gain $\sim 1200 \Omega$ and fed to the DRS4 sampler, operating at 1 GS/s. The sampling window is chosen so as to cover the entire profile of the SiPM signal, as well as the trigger latency of mini-ICAL. On receiving the cosmic muon trigger from mini-ICAL, the sampled data is digitised. Either a zero-suppressed pulse profile data or an integrated signal charge data of all hit channels of CMVD will be transferred to the backend. The muon veto efficiency of the CMVD is computed by extrapolating the muon tracks recorded by the mini-ICAL onto the veto walls and matching them to the CMVD hits there. 72 FPGA-based DAQ boards, each hosting 40 transimpedance amplifiers, five DRS4 and ADC chips besides network interface are being developed. Customised SIPM bias supply units along with extensive configuration, control and calibration of the detector elements as well as electronics are also being designed.

Data acquisition system

Fig. 4 shows a simplified block diagram schematic depicting the overall DAQ for the CMVD using DRS4. 72 SiPM-DAQ boards will be used to cater for the 712 scintillators or 356 DCs of the CMVD. Each DAQ will be connected to the back-end server over Ethernet. The DAQ system has to measure and store the value of the charge produced by every relevant SiPM in the CMVD on every mini-ICAL trigger. For doing this we propose to use the DRS4 chip for sampling the SiPM signal. The DRS4 is a switched capacitor array which can sample input channels at up to 5 GSa/s and store the input analog waveform in 1024 cells. Whenever required the DRS4 can be stopped to

readout this stored waveform for external digitization. Thus, at any point of time we can readout the last 1024 ns of the analog waveform if we are sampling the input channels at 1 GSa/s.

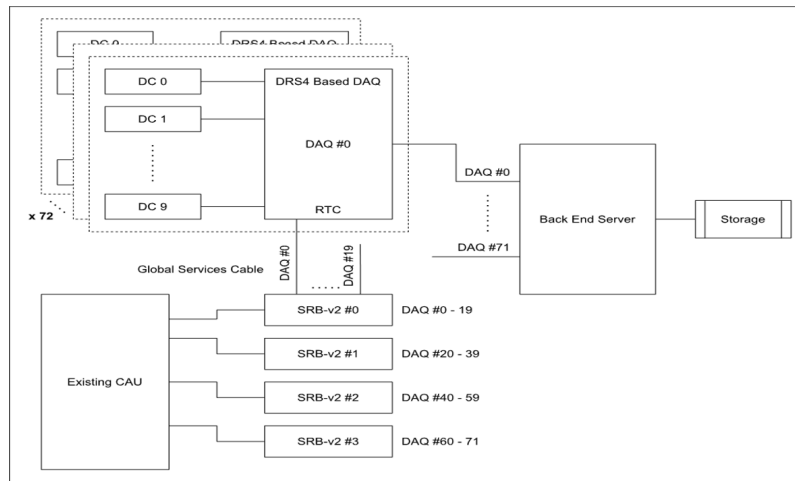


Figure 4: Block Diagram of the Overall DAQ System for the CMVD based on DRS4.

Upon a mini-ICAL trigger, the DAQ boards will be required to stop the DRS4 sampling process and readout the stored waveform for digitization, so that the status of the SiPM during the trigger can be read and stored if found relevant. Since the trigger latency can be measured, the DAQ can readout only the region of interest (ROI) from the 1024 ns of the stored waveform. The ROI can be adjusted to have the full pulse width of the SiPM signal for a typical muon event, plus some overhead to accommodate the jitter owing to the 4.7 m long plastic scintillator, the trigger latency and some part of the waveform before the pulse to determine any baseline offset. The stored digitized data can be processed online in the FPGA to perform baseline offset correction and zero suppression to reduce the data size. It can be further processed to find the charge value of the SiPM pulse so as to reduce the data size by a factor of 100.

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