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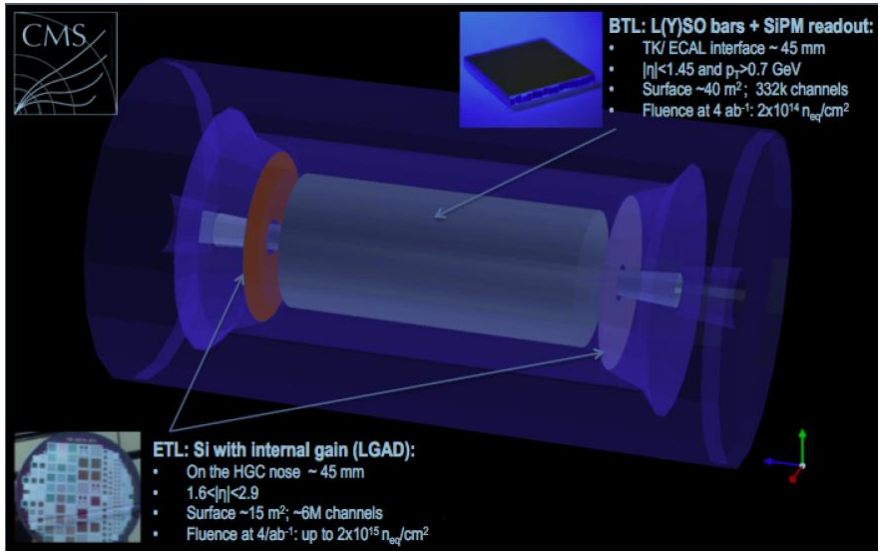
ETROC1: the First Full Chain Precision Timing Prototype for CMS MTD Endcap Timing Layer

Quan Sun, Fermilab

on behalf of ETROC Collaboration

CMS MTD



Schematic view of timing layers comprising a barrel layer, at the interface between the tracker and the ECAL, and two endcap timing layers in front of the endcap calorimeter

MIP timing detector(MTD) is a new detector on CMS planned for HL-LHC.

- Used for disentangling the approximately 200 "pileup" interaction for each bunch crossing
- Provides ability for charged hadron identification and the search for long-lived particles.
- 30-40 ps per track time resolution at HL-LHC start is required to reduce pileup significantly
- 50-60 ps by the end of HL-LHC operation (3000 fb^{-1}) because of radiation damage to the sensor

MTD includes barrel timing layer(BTL) and endcap timing layer(ETL)

- ETROC(Endcap Timing Readout Chips) is ASICs for the endcap timing layer readout.

Ref. A MIP Timing Detector for the CMS Phase-2 Upgrade, Technical Design report

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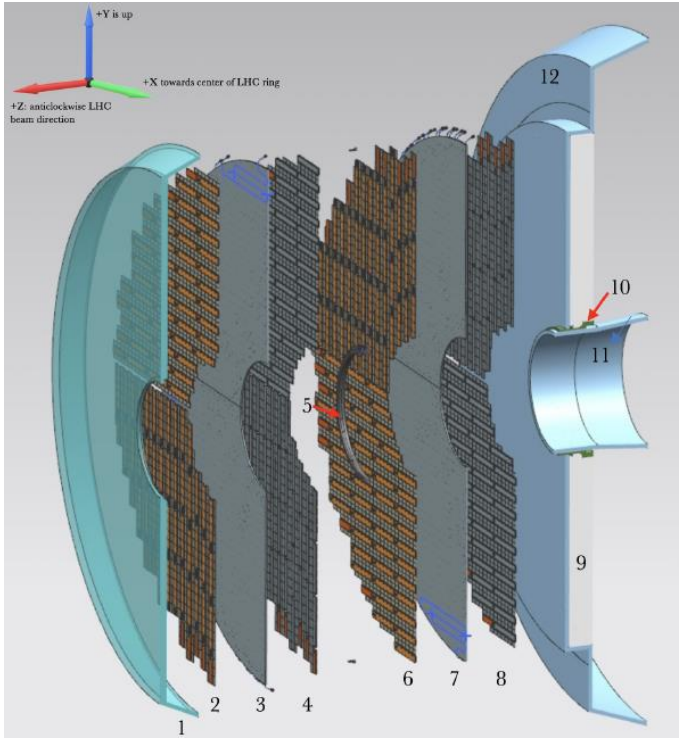
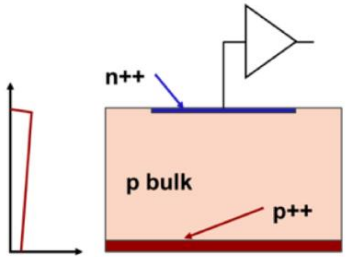
Endcap Timing Layer(ETL)

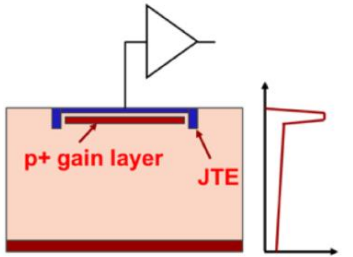


Ref. A MIP Timing Detector for the CMS Phase-2 Upgrade, Technical Design report

- Two disks per endcap mounted on HGC nose
  - 2 hits per track→ relieve FE electronics design
  - About 3 m from the interaction point
  - 315 < r < 1200 mm^2
  - Area ~ 14 m^2; ~ 8.5 M channels; ~200 wafers
- ETL uses LGAD (low gain avalanche diode) as detector
  - LGADs employ additional gain layer to generate larger signal
  - 1.3 X 1.3 mm^2 pixel: ~3.4 pF capacitance
  - 16 X 16 pixel LGAD bump-bonded to ETROC ASIC
  - ETROC extract timing information of small input signal from LGAD, **typical 10-20 fC for normal operation** (down to 5 fC at end of HL-LHC operation for inner most sensors).



Traditional silicon detector



Low Gain Avalanche Detectors(LGADs)

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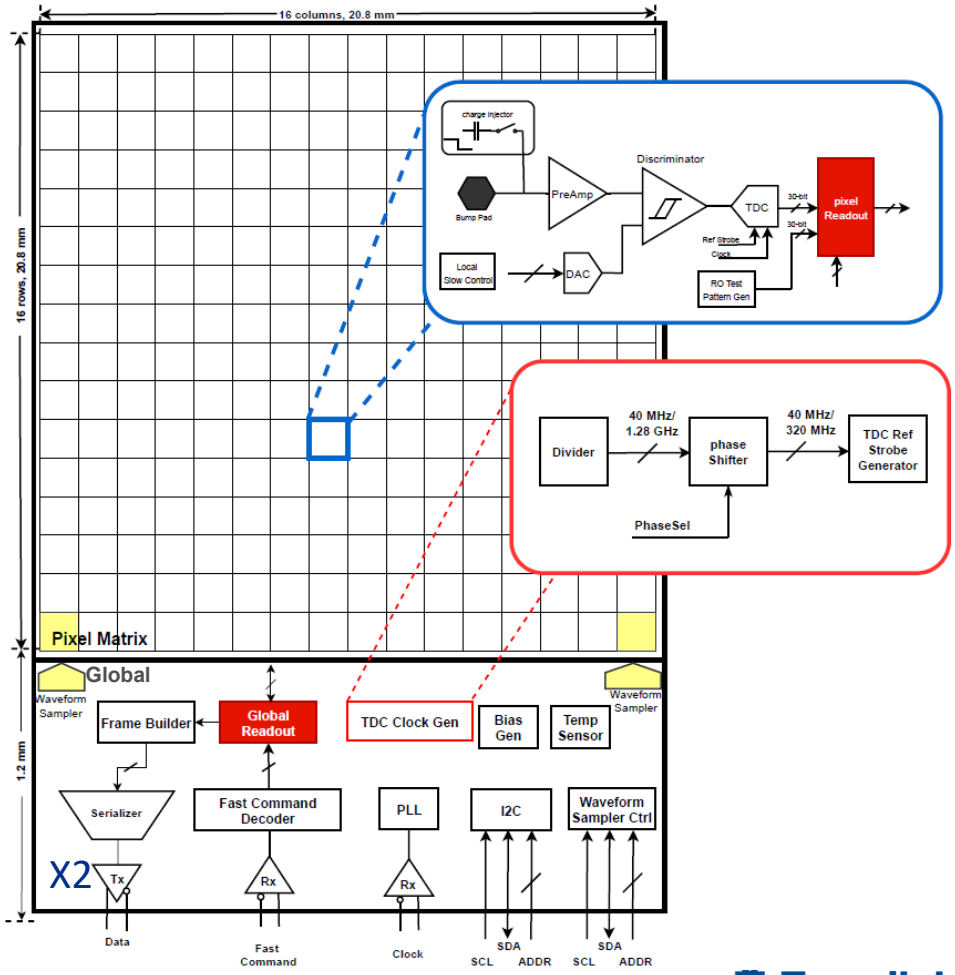
ETROC Overview

- 16x16 pixel matrix: 1.3 x 1.3 mm^2
- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
- L1 trigger-driven readout with zero suppression
- Flexible trigger path
- Fast waveform sampling for two pixels
- Interface of ETROC
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Two serial links: each up to 1.28 Gbps
- Time resolution contribution: ~ 40 ps
- TSMC 65 nm technology, 1p9m, 1 W/chip@1.2 V
- 100 MRad TID tolerance, SEE protection for controls



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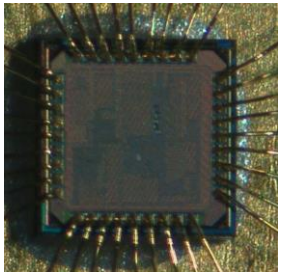
A brief history of ETROC development



ETROC0:

Single channel analog frontend

- Preamp + discriminator

- Taped-out Dec. 2018
- Extensively tested
  - Functionality verified
  - TID up to 100 Mrad
  - 30 ~ 40 ps time resolution in test beam

ETROC1: 4x4 pixel matrix with full signal chain

- PA + Discri. + TDC + simplified readout

- Standalone pixel and TDC for test
- Taped-out Aug. 2019
- Extensively tested

Waveform sampler

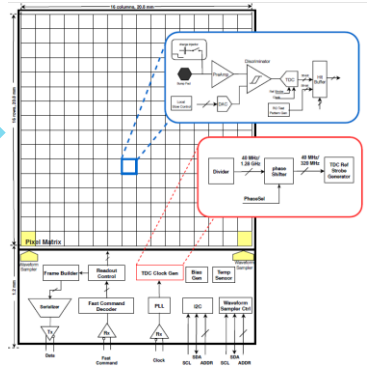
- ❑ Performance met the specs.
- ❑ TID-hard version submitted

ETROC_PLL

- ❑ PLL works as expected

ET2_test

- ❑ I2C/Temperature sensor/EFUSE/improved TDC
- ❑ Testing soon



ETROC2: full size, full functionality prototype, planed March 2022.

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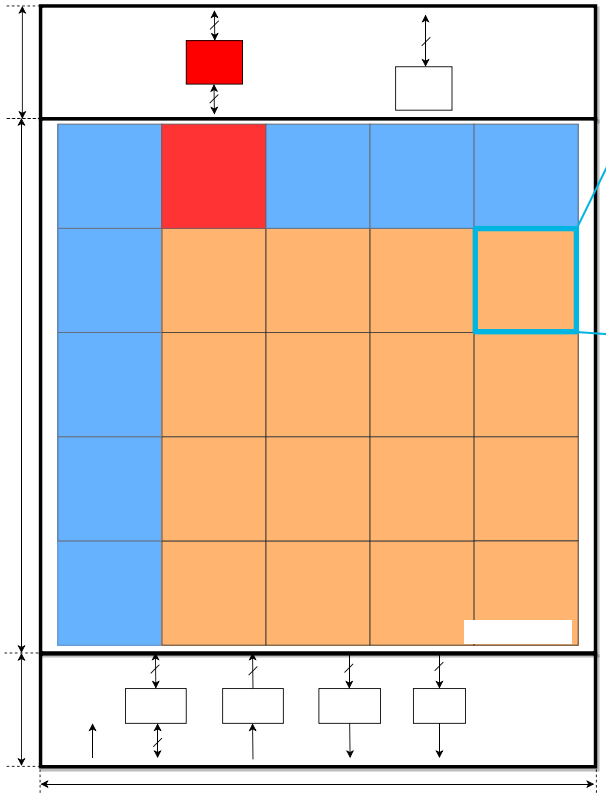
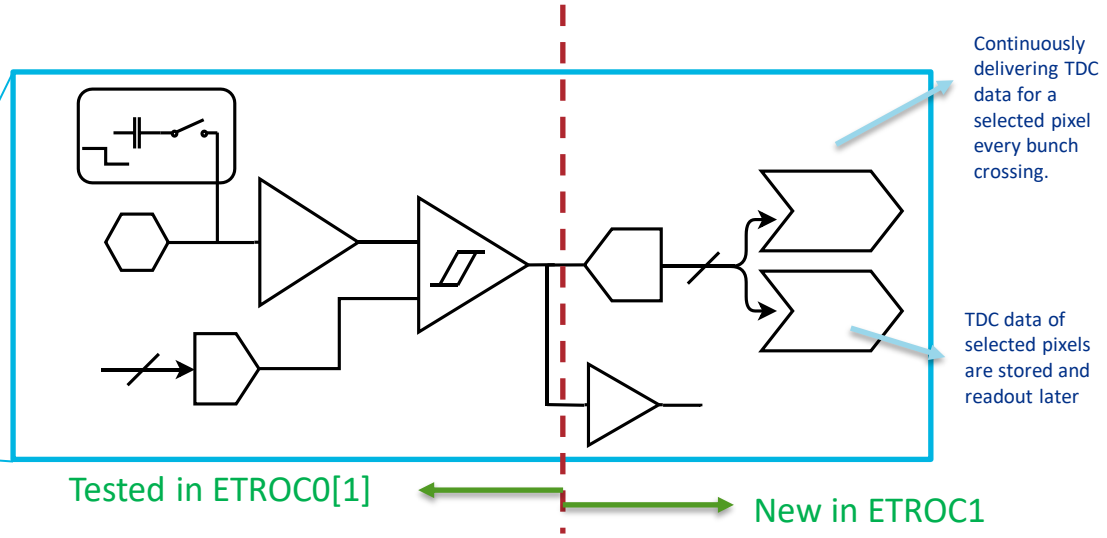
ETROC1 architecture





ETROC1 serves to prototype TDC and full signal chain in a small array

- The 4 X 4 pixel matrix including H-tree clock distribution
  - Preamp
  - Discriminator
  - TDC[2]
  - Two simplified readouts: diagnostic readout/ simple readout
- Standalone pixel (in red with full frontend)
  - Only diagnostic readout
- Standalone TDC test block
- The eight dummy pixels provide electrical and mechanical support to the sensor

[1]Q. Sun, et al, The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL
[2] W. Zhang, et al, A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

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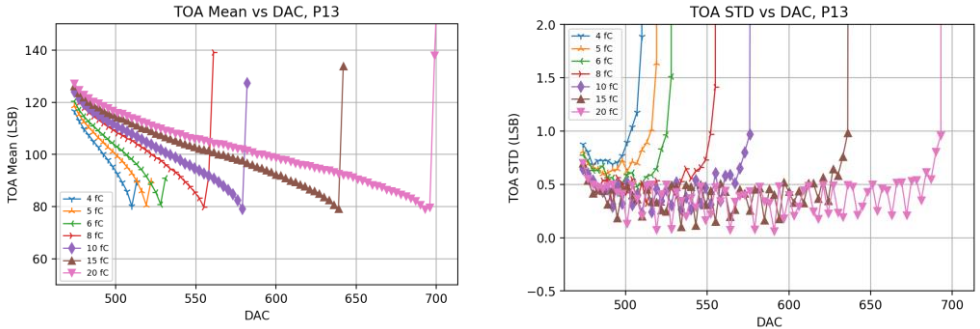
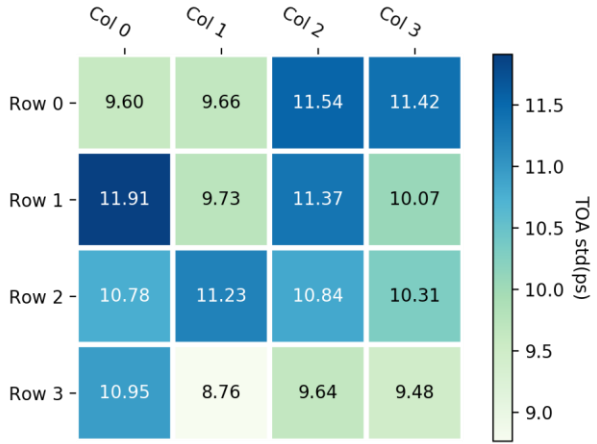
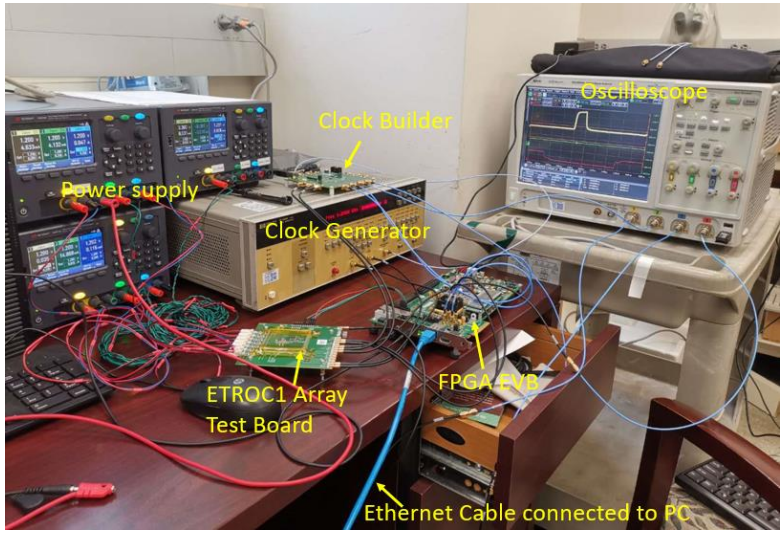
ETROC1 Test: without sensor







- Bare ETROC1 was tested with charge injection
- Performance is good and match with expectation

Full chain time resolution of each pixel from TDC data with time walk correction.

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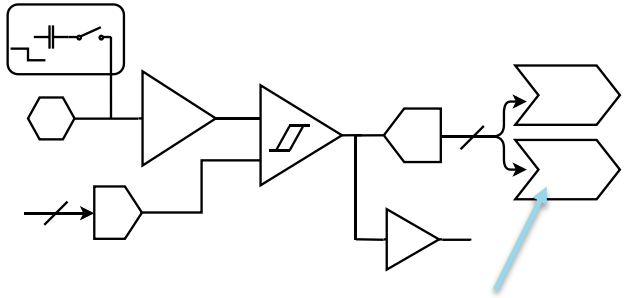
ETROC1 test with LGAD sensor

- Noise(crosstalk) related to the 40 MHz clock was observed after LGAD bump-bonded
- Noise gone at discriminator output with high enough threshold

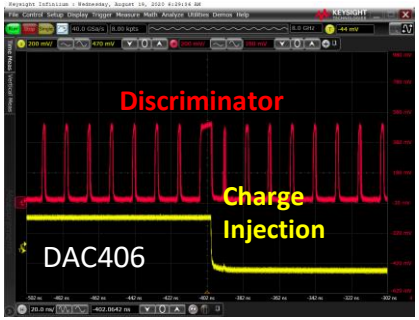


Noise source was identified as the clocking activities in the memory used in simple readout

For ETROC1 beam test, high enough threshold was used (8 fC)

Sensor board, clock enabled

- Q=20 fC
- HV=-170 V



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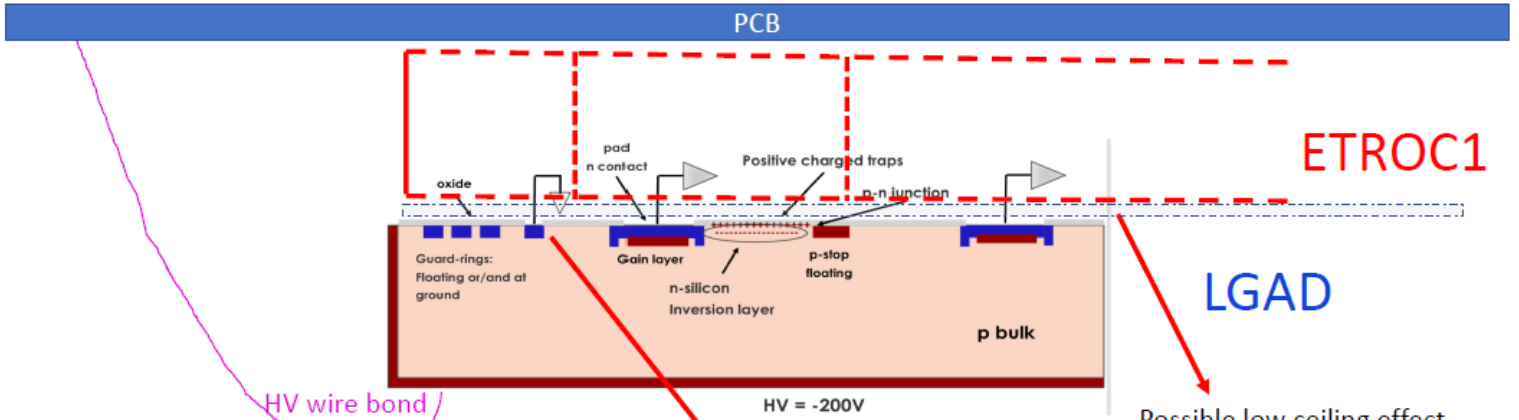
Noise coupling path exploration



Through the HV path

- *Remove all HV wires*
- *Increase wire spacing*
- PCB design optimization

Removing all HV wires
→ noise reduced by 60%

Through the guard ring pads connection

- *Connect only one pad to PCB ground*
- *Keep ALL guard ring pads floating*

(no effect)

Possible low ceiling effect

- *Increasing the spacing with bump on both sides*
  - *50um → 120 (61) um*
- Possibly use interposer with shielding between

(No clear difference)

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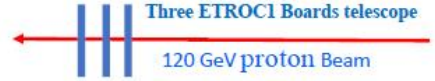
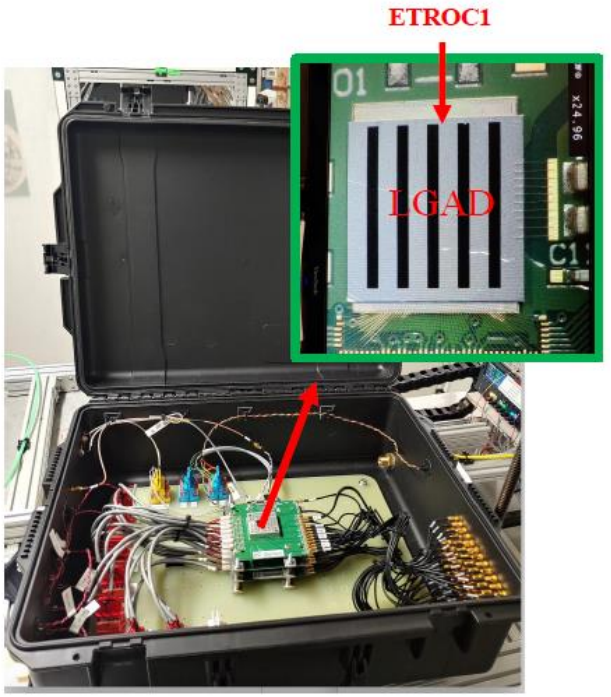
ETROC1 beam test

ETROC1 Beam Telescope @ FTBF





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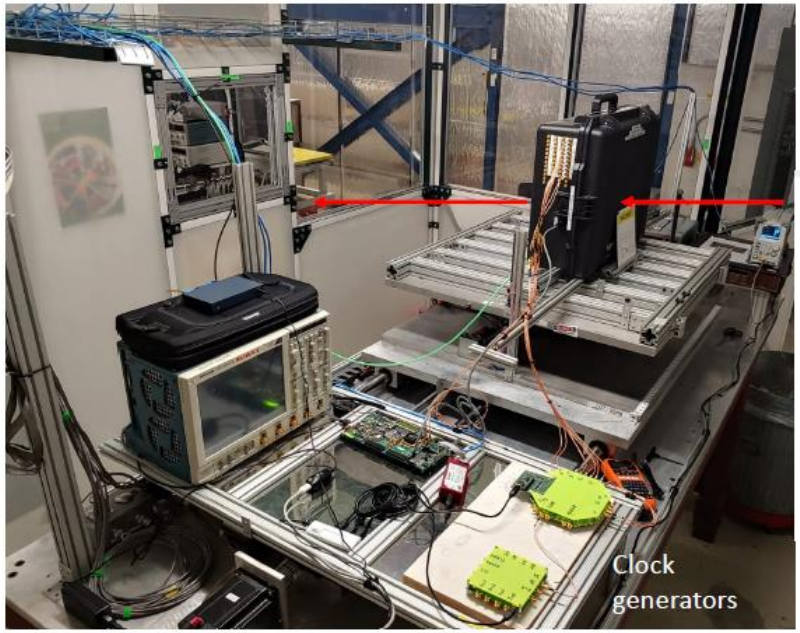
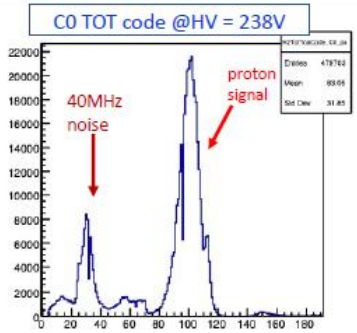
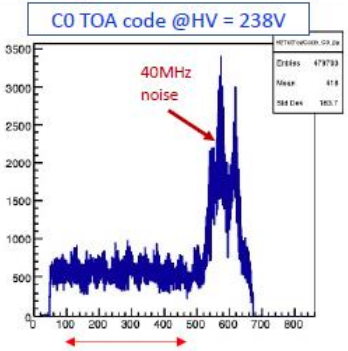
ETROC1 beam test

ETROC1 Beam Telescope @ FTBF



Telescope DAQ:
Triggered on B1
offline confirmed with B2
C0 is Device Under Test





Tevatron machine clock 53MHz
ETROC clock 40MHz

Beam TOA (time of arrival) is flat,
and 40MHz noise is not.
Can stay away from the noise this way

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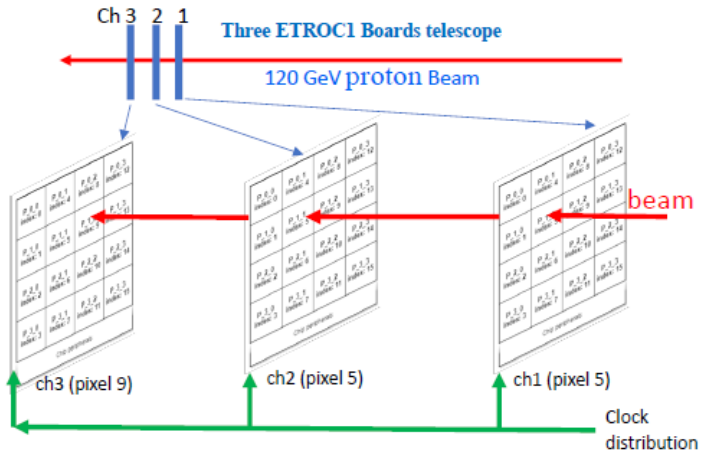
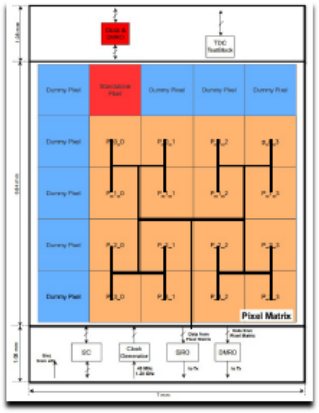
ETROC1 beam test

LGAD+ETROC1 – Preliminary Test Beam Results



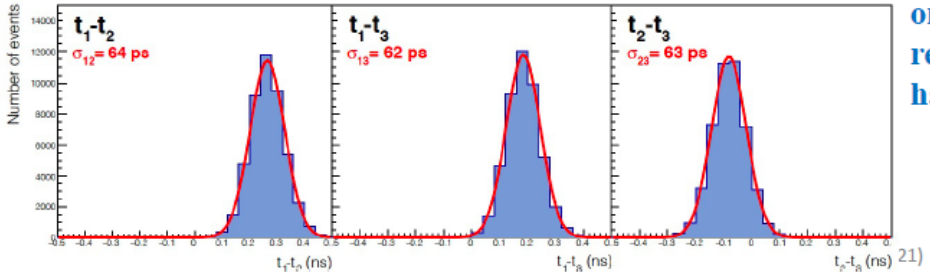
ETROC1 4x4 H-tree clock distribution within chip



ETL Time resolution

Simulation vs spec (unit: ps)

LGAD+ preamp/discriminator + TDC bin	35	
Time-walk correction residual	< 10	
Internal clock distribution	< 10	
System clock distribution	< 15	
Per hit total time resolution	41	50 ps
Per track (2 hits) total time resolution	29	35 ps



From preliminary analysis of the data from ongoing beam test at FNAL, the time resolution of each LGAD+ETROC1 layer has reached:

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$ ~ 42 – 46 ps

(with LGAD HV=230V for all three channels)

*This measured time resolution includes all **four contributions** in the table*

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Summary

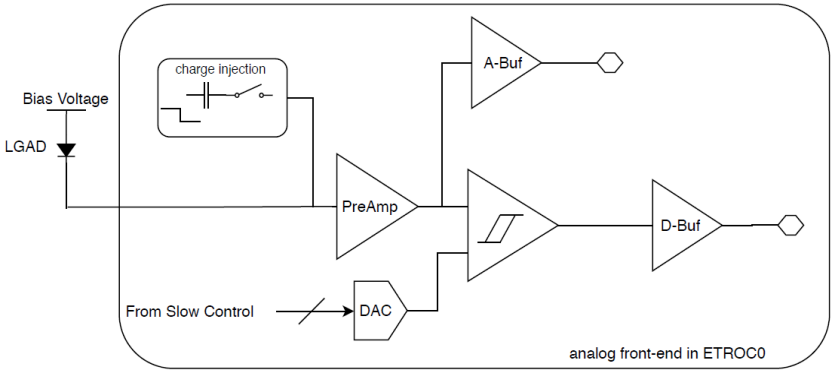
- ETROC0
  - Tested with Charge injection/Cosmic/Laser: consistent with expectation
  - TID tested up to 100 Mrad: no issue observed
  - Beam test: ~30 ps achieve(preamp waveform analysis)
- ETROC1
  - New TDC extensively tested: performance meet requirements
  - 4X4 array full chain in bare ETROC1 works well with charge injection
  - ETROC1 with LGAD sensor bump-bonded
    - noise from memory clock activities observed
    - High enough threshold (8 fC) used in beam test: 42~46 ps per hit(spec. < 50 ps per hit)

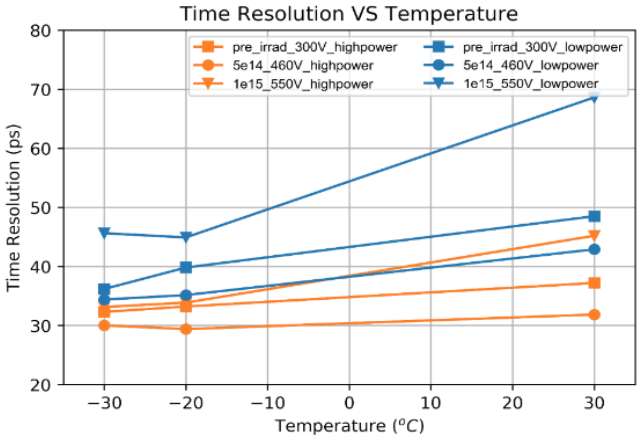
Towards ETROC2

- PLL was tested in a prototype chip and meet the specs.
- Waveform sampler was tested with good results
  - An improved version for radiation tolerance was taped out recently
- ETROC2 design in progress (planned submission in March 2022)
  - Noise source in ETROC1 has been identified and will be minimized in ETROC2 design
    - Clock/address gating based on hit is applied to memories to reduce noise injection and power consumption
    - Some of memory activities are offset for different pixel groups to reduce noise injection
    - Readout logics have ability to work under 1 V supply → significantly reduce noise injection and power consumption
    - Flexibility to disable readout clock for selected pixels (for testing purpose)
    - Pads arranged to facilitate PCB ground optimization (likely part of major noise coupling path)
    - …

Acknowledgments

This work has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the US Department of Energy, Office of Science, Office of High Energy Physics.


charge injection
Bias Voltage
LGAD
A-Buf
PreAmp
D-Buf
From Slow Control
DAC
analog front-end in ETROC0


Time Resolution VS Temperature
pre_irrad_300V_highpower
5e14_460V_highpower
1e15_550V_highpower
pre_irrad_300V_lowpower
5e14_460V_lowpower
1e15_550V_lowpower
Time Resolution (ps)
Temperature (°C)
80
70
60
50
40
30
20
−30
−20
−10
0
10
20
30

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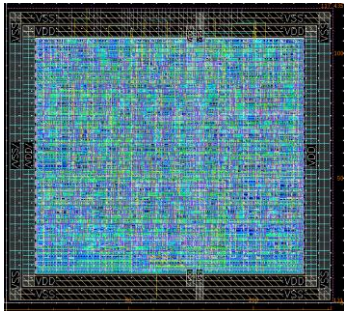
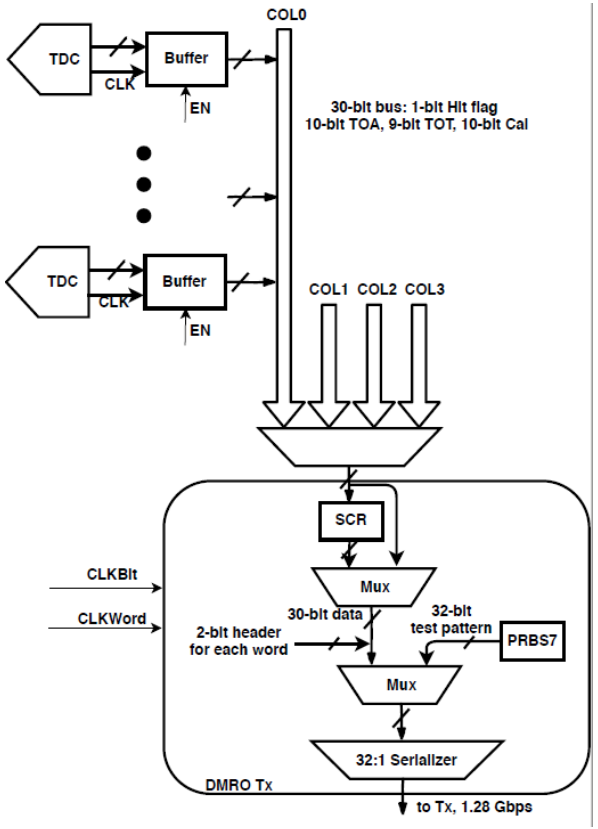
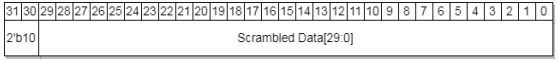
Diagnostic Mode Readout(DMRO)

- Only a selected pixel is readout at one time
- The 30-bit data from the TDC is encapsulated and transmitted at each BX clock
- No zero-suppression
- 30-bit Data is scrambled with a polynomial: $X^{58}+X^{39}+1$
- A 2-bit header(2'b10) is added in each word for alignment
- PRBS7 pattern is used to test the serializer
- Data rate: 1.28 Gbps
  - Raw data rate: 1.2 Gbps(30-bit/word * 40 Mword/s)
  - MSB out first
- DMRO block
  - implemented with digital flow
  - size: 130 um X 120 um
  - Power consumption: 1.2 mW







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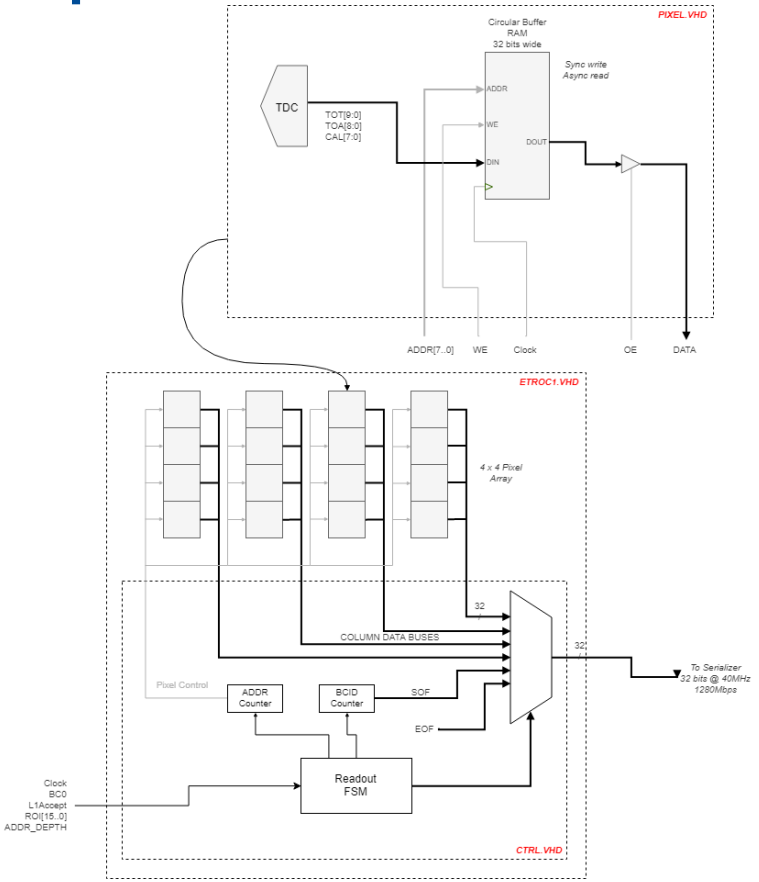
Simple Readout Scheme



- One or more pixels could be selected for readout at one time.
- A circular buffer in each pixel stores data from TDC
- Once L1 acceptance presents, data in the circular buffers is frozen.
- All the data in the circular buffer of selected pixels is then readout at 1.2 Gbps with DMRO block
- Circular buffers accept TDC data again when all the data is delivered.

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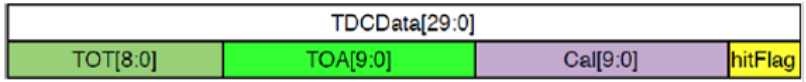
TDC data interpretation

Details of TDC in the published paper and a set of dedicated slides

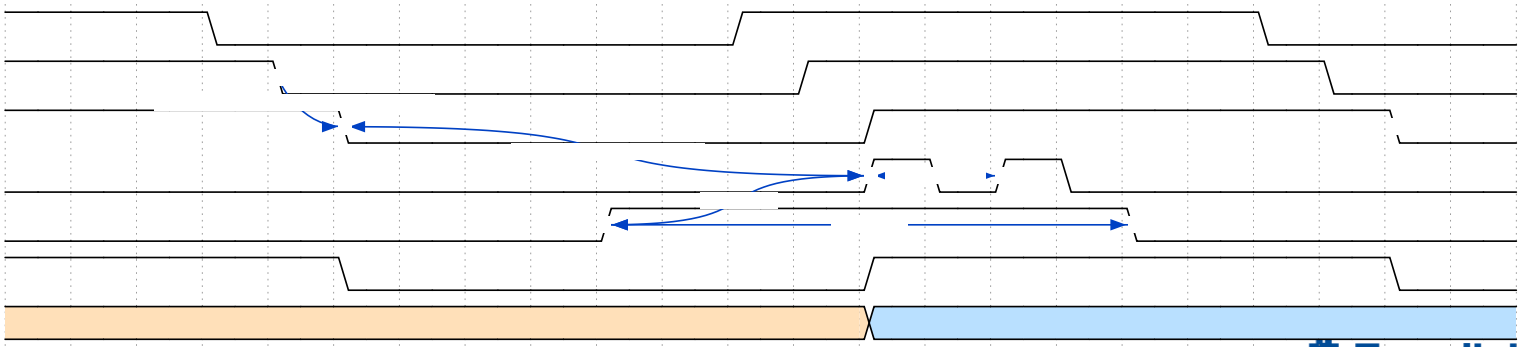


hitFlag: discriminator pulse detected in a BX or not

- bin= T3/Cal_code
- TOA=bin*TOA_code
- TOT=(TOT_code*2 – floor(TOT_code/32))*bin

  T3 is programable, 3.125 ns by default.

- A clean reference strobe is critical for TDC performance
  - Good clock distribution required



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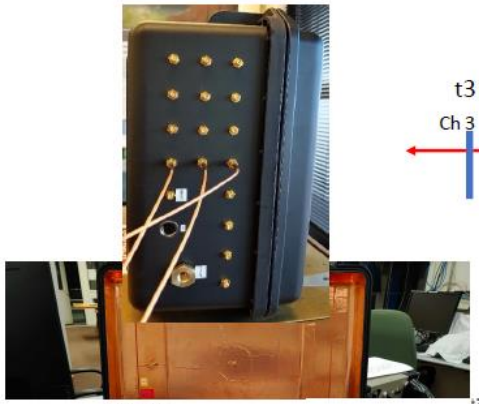
ETROC0 beam test results

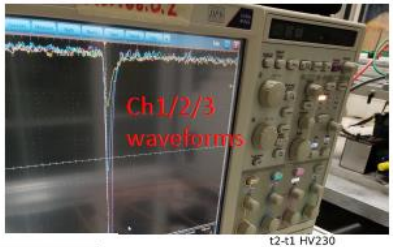
Comparing to ETROC0: A simple ETROC0 Beam Telescope (with 3 HPK-ETROC0 boards)

Jan-Feb 2020

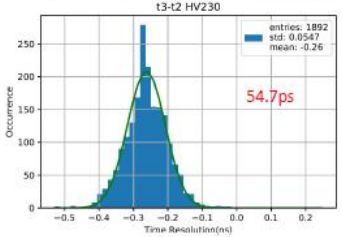
Simple "suitcase" setup in parasitic mode running at FNAL MTest

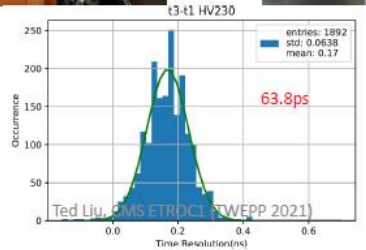


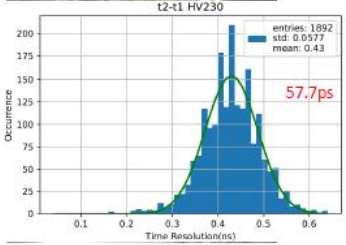
$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx 33\ (ps)$$



preamp waveform analysis







9/23/21

Ted Liu, CMS ETROC1 (TWEPP 2021)

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TDC

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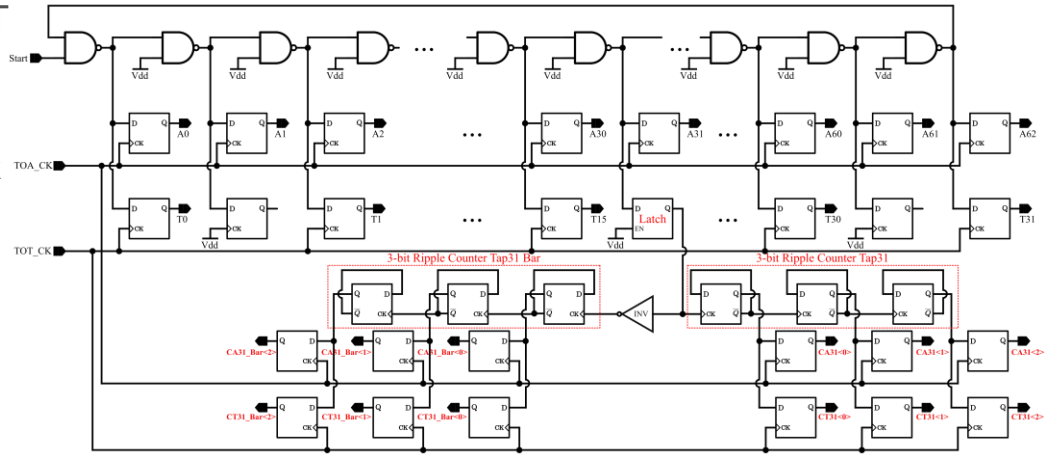
  control, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- In-situ delay cell self-calibration technique
  - For each hit, will use two consecutive rising clock edges to record two time-stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - The average delay of delay cells is thus derived.
- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
    - Measured TOA bin ~ 18 ps, TOT bin ~ 36 ps
  - ETROC TDC power goal: < 0.2mW
    - Measured power at 1% occupancy: 0.1 mW
- TDC improved for power robustness and taped-out



ETROC1 TDC core schematic

Ref: W. Zhang, et al, A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

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