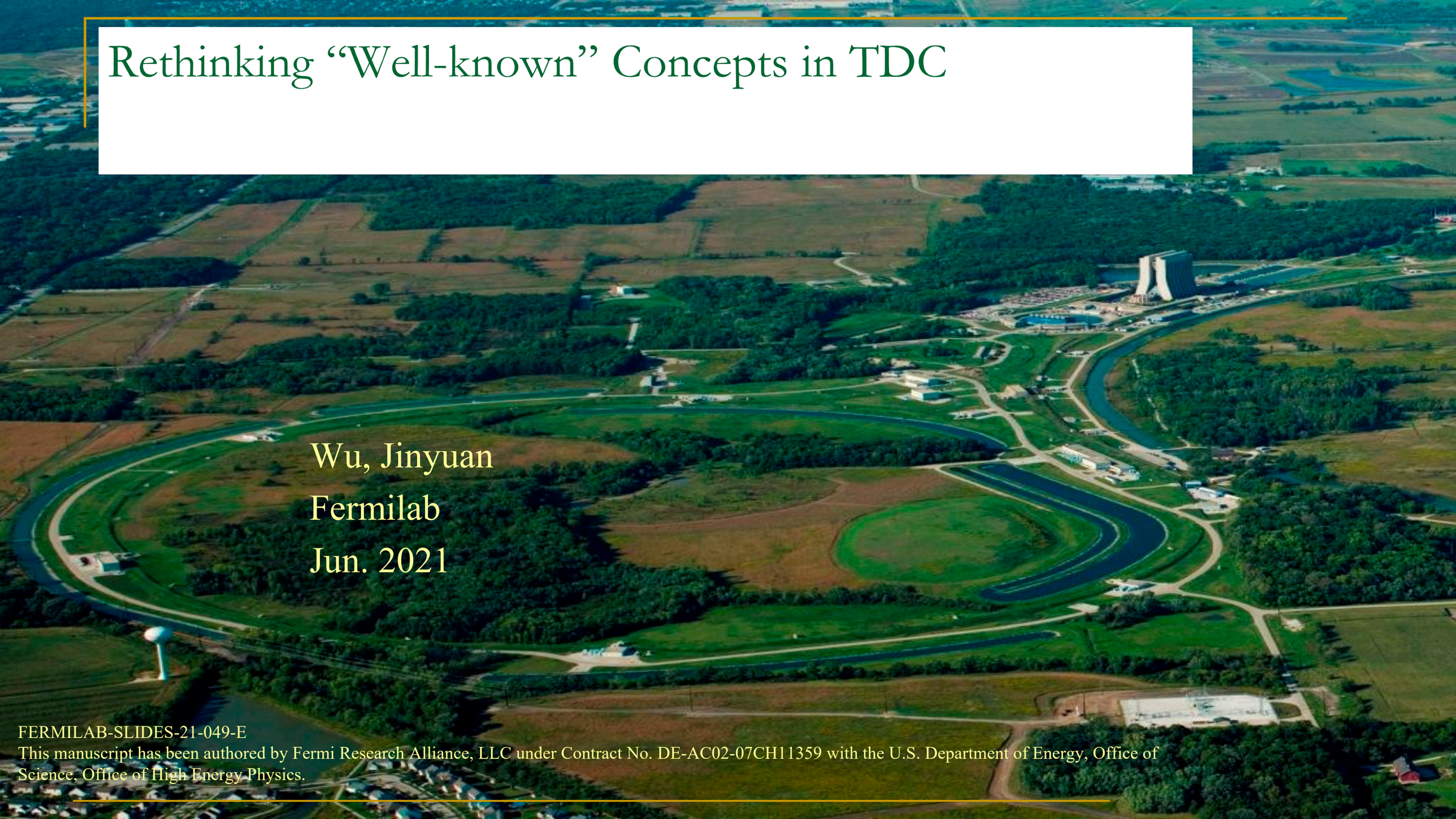
Rethinking "Well-known" Concepts in TDC



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Fermilab
Jun. 2021

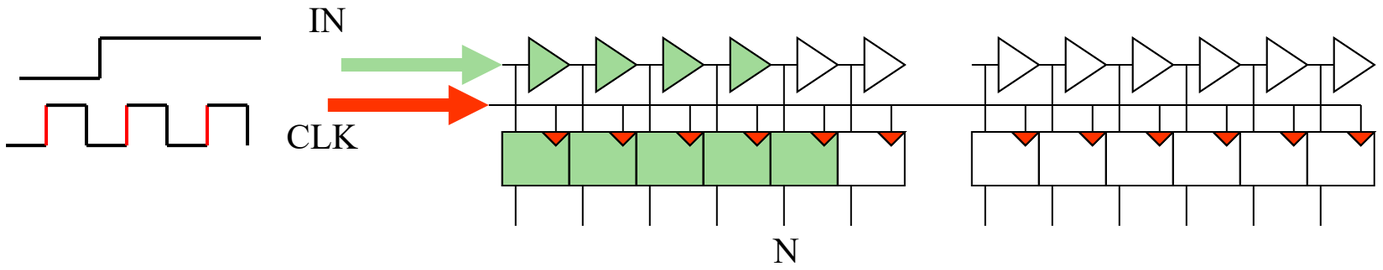
FERMILAB-SLIDES-21-049-E

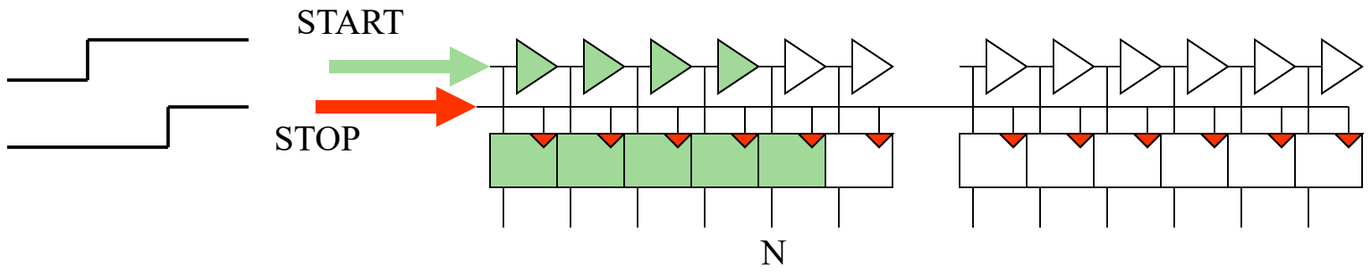
Introduction

- Should TDC always have START and STOP signals?
- Should we implement delay cells with exact bin width?
- Is Gray code a good thing in TDC?
- Should we only use “random” events to calibrate TDC?

START/STOP or IN/CLK

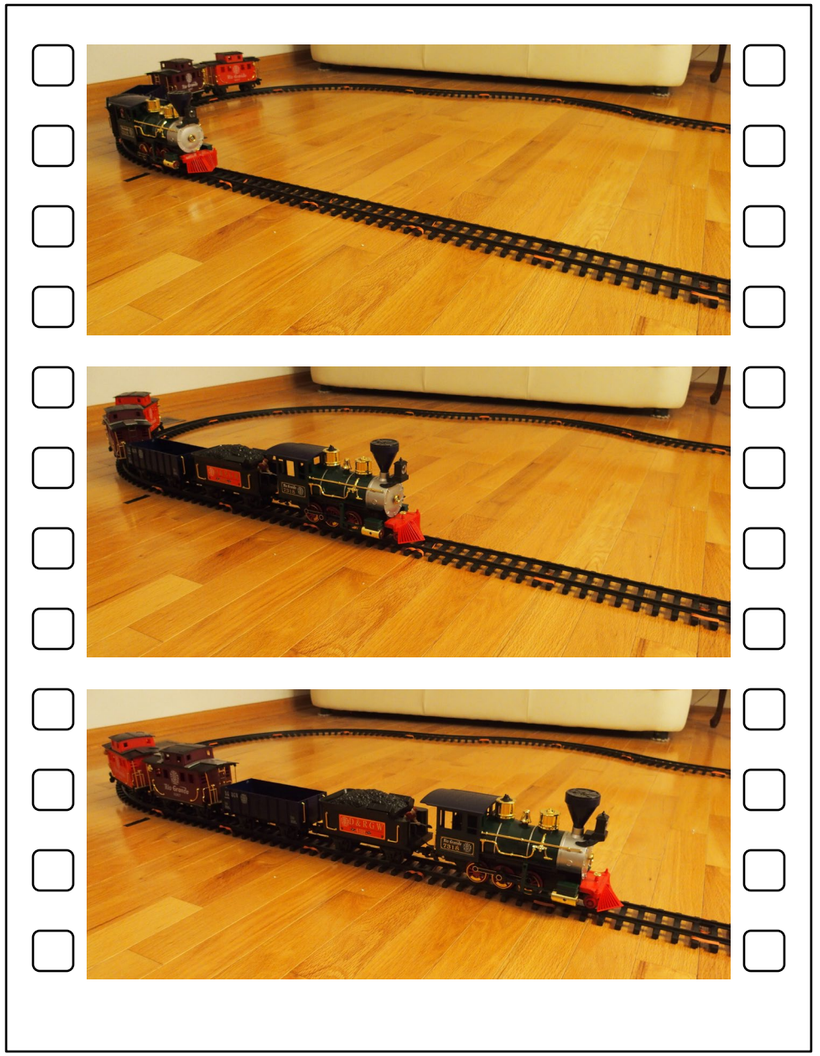
Start/Stop vs IN/CLK





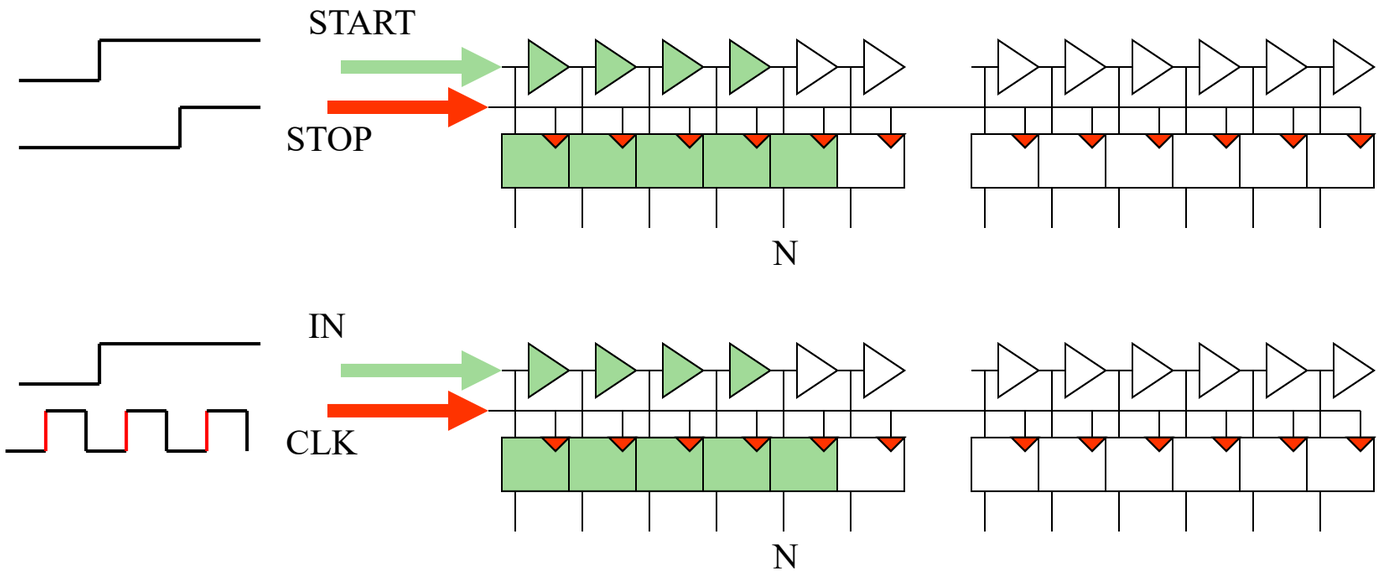
- Start/Stop type TDC: Measures time interval between START and STOP signals.
- IN/CLK type TDC: Measures absolute arrival time of IN since reset of CLK.
- These are two different visualizations of TDC.

Visualization: Stopwatch or Video Camera



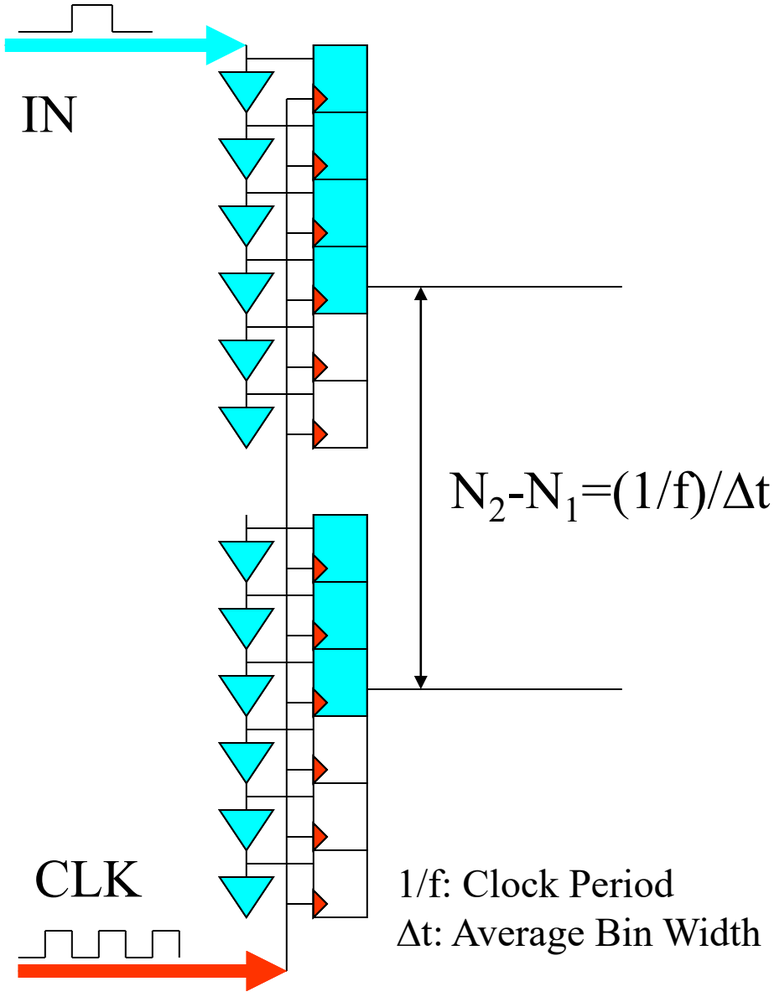
- The Start/Stop TDC looks like a stopwatch.
- The IN/CLK TDC looks like a video camera.

A Never Stopped TDC



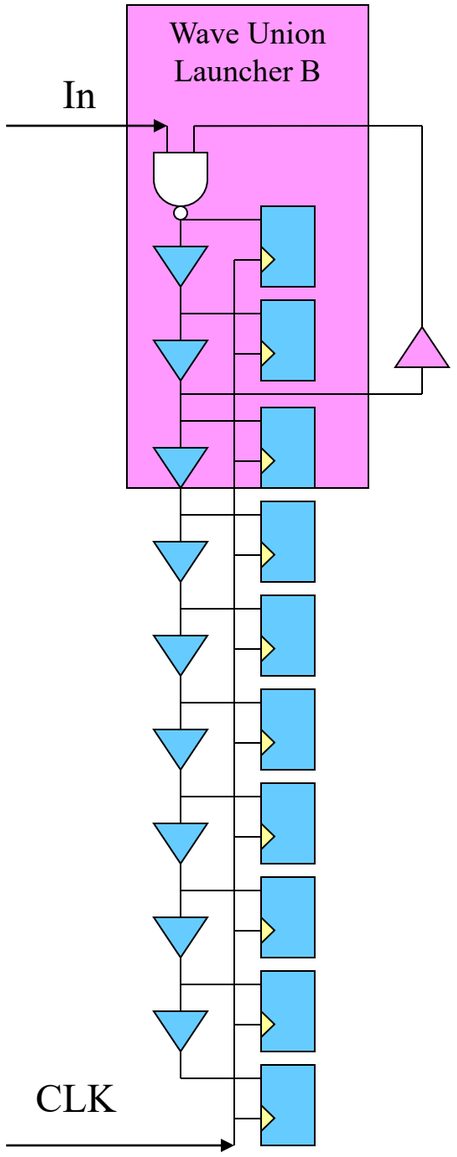
- Wide measurement range.
- Multiple hits, No deadtime.
- Multiple measurements:
  - For Averaging
  - For Calibration
- Wave Union TDC

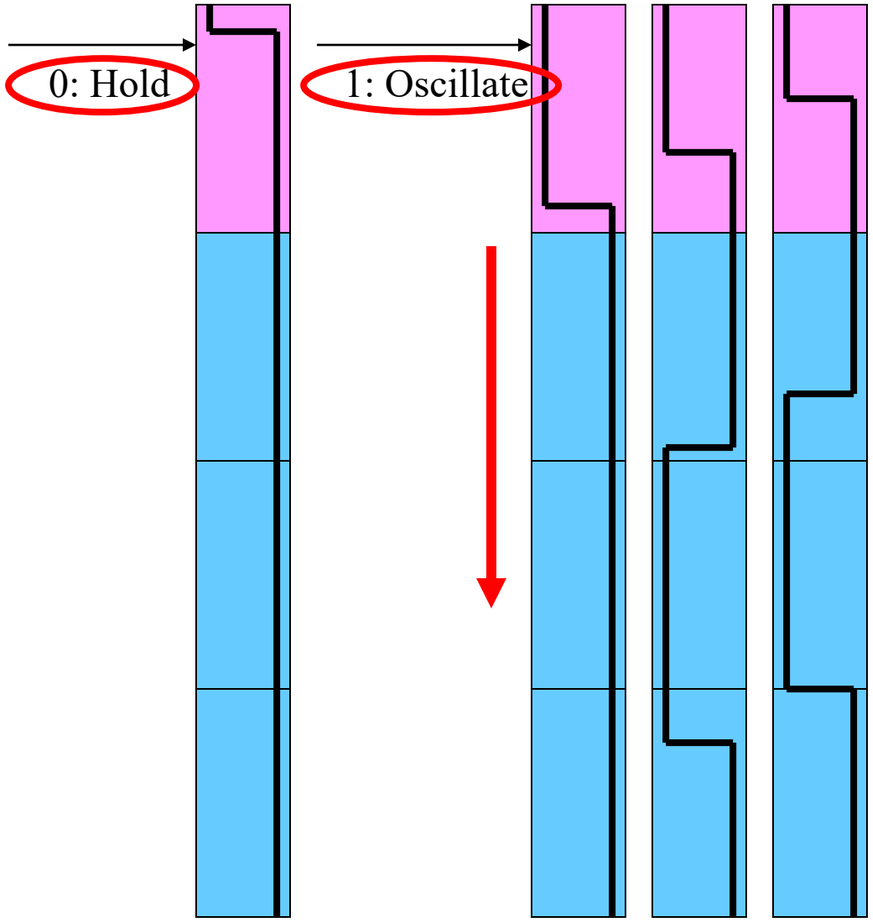
Multiple Measurements for Calibration

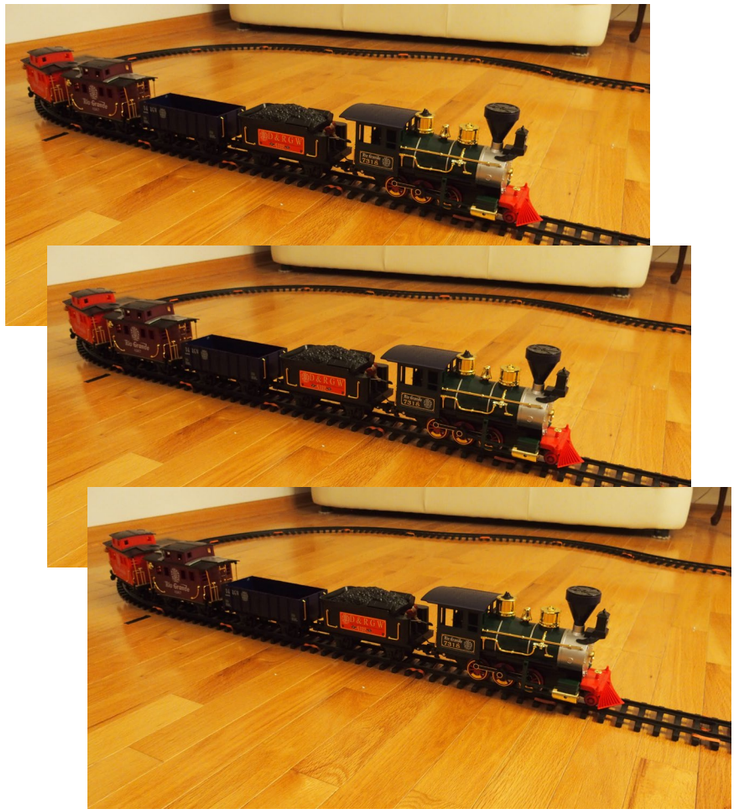


- For each input, make two or more measurements.
- The extra measurements can be used to calibrate temperature variation as well as increase measurement precession.

Wave Union TDC (B Type)





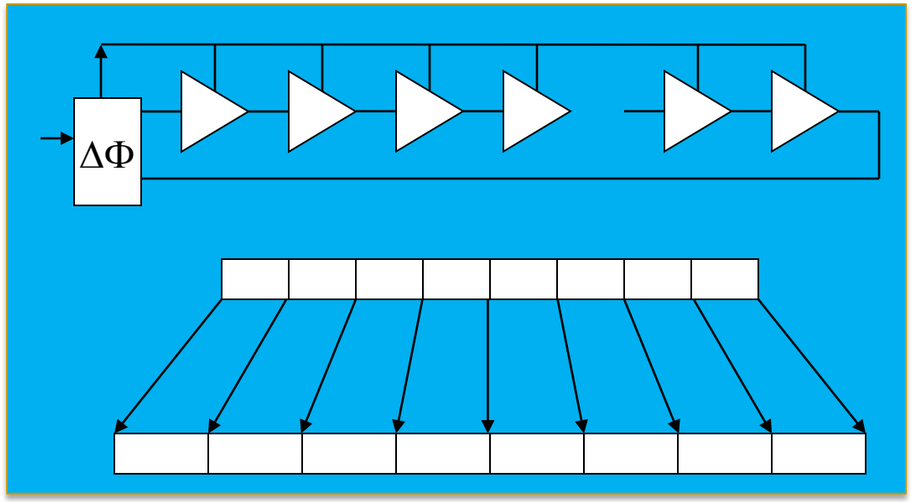


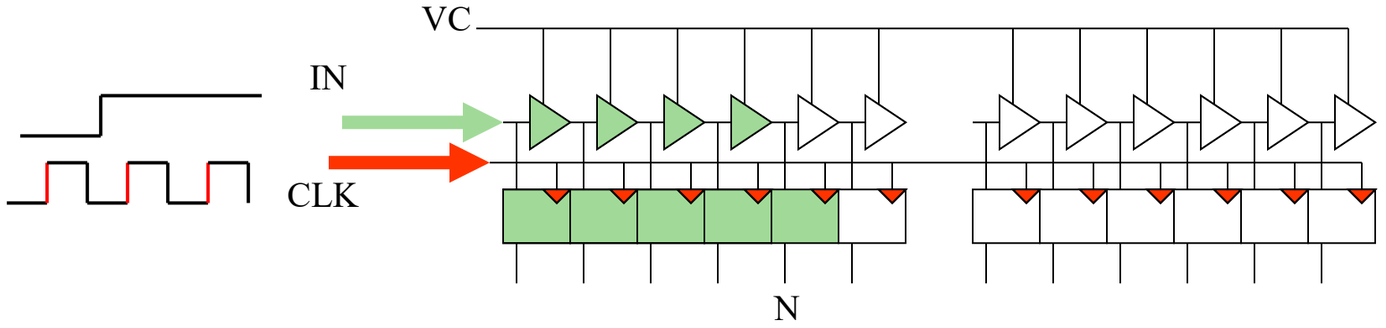
- The Wave Union Launcher can also be a gated ring oscillator.
- Many “snapshots” can be taken.

Even Bin Width: Maters or Not?

Bin Width Adjustment In ASIC TDC

- In ASIC TDC, the delay cells can be “staved” to slow down to predefined bin width.
- The control voltage VC is generated by a phase detector circuits.
- The adjustment is convenient, but the analog circuits consume extra power.

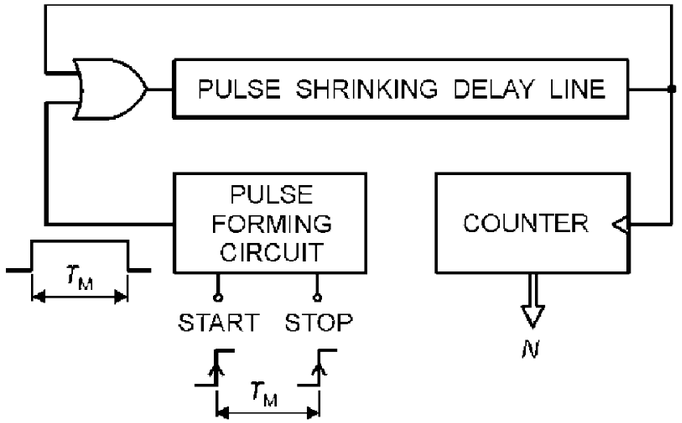


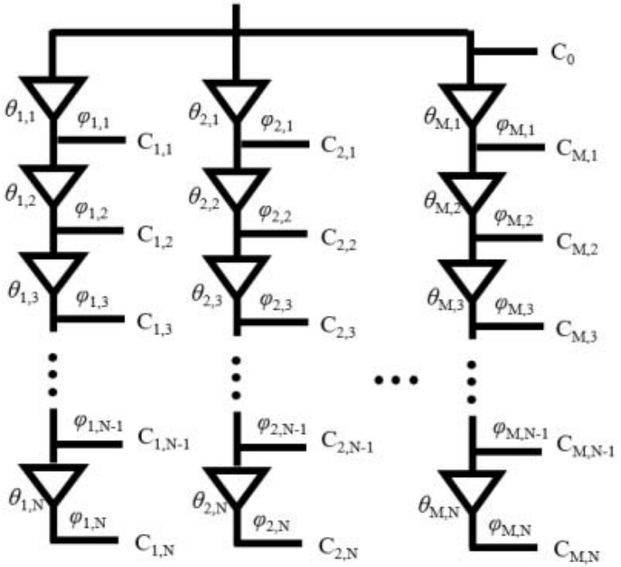


- The bin width adjustment is not necessary for TDC.

Phenomena Suitable for TDC

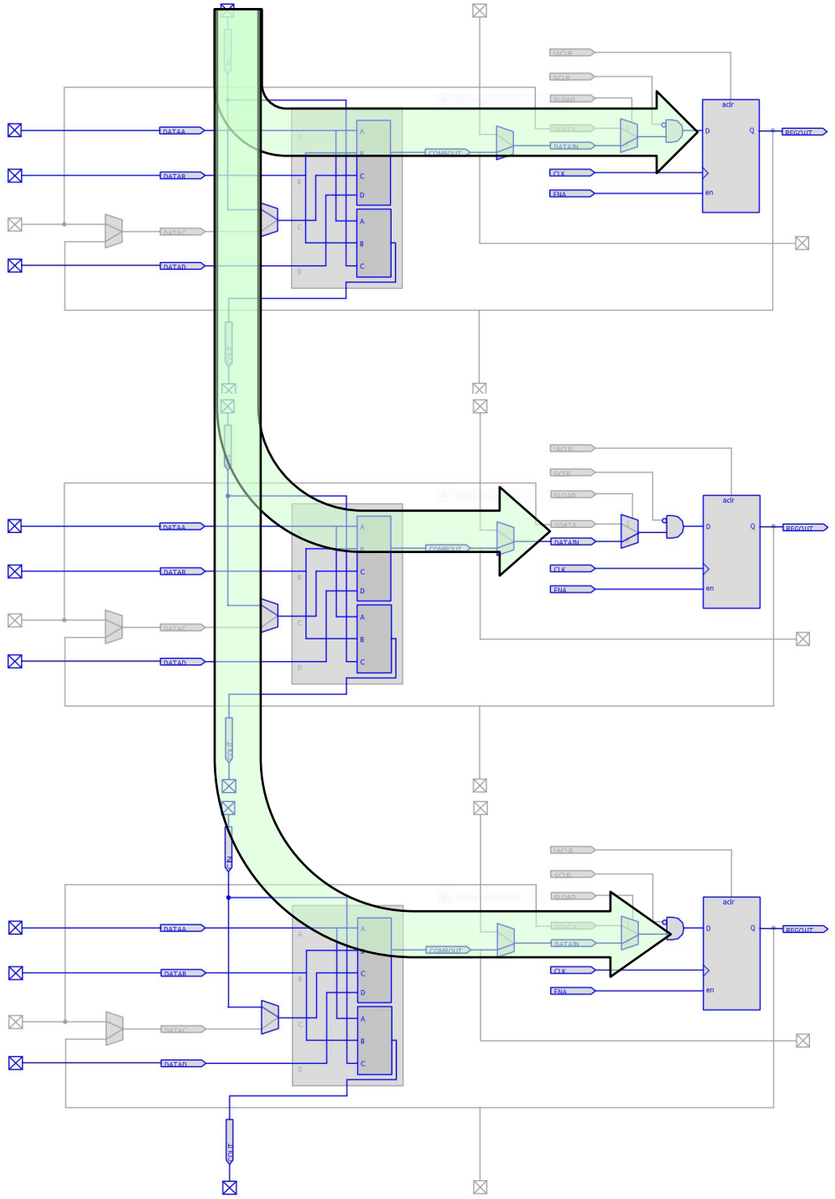
- Any phenomena with detectable change when the arrival time changes can be used to implement TDC.
  - Delay Chain.
  - Time to Analog Conversion.
  - Pulse Width Shrinking. (Ryszard Szplet, et. al.)
- No need to restrict yourself for even bin width, chronical order etc.





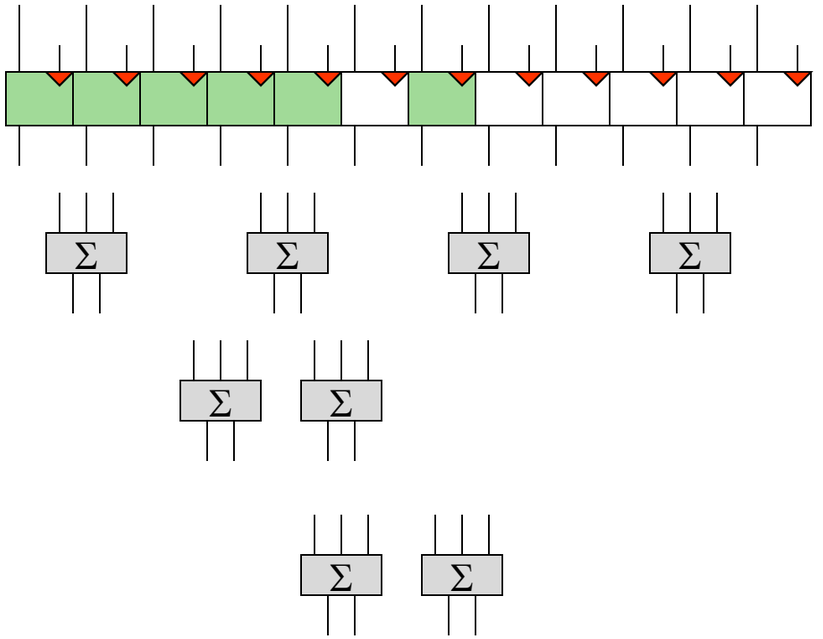
Missing Code

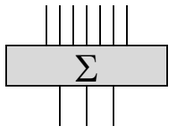
- In some circumstance, the “later” delay cells may see the signals before the “earlier” cells.
- A “bubble” would show in these earlier cells.
- If using thermometer encoder, the code corresponding to these earlier cells would be missing.
- The “missing codes” are not actually missing.



Multiplicity Encoder

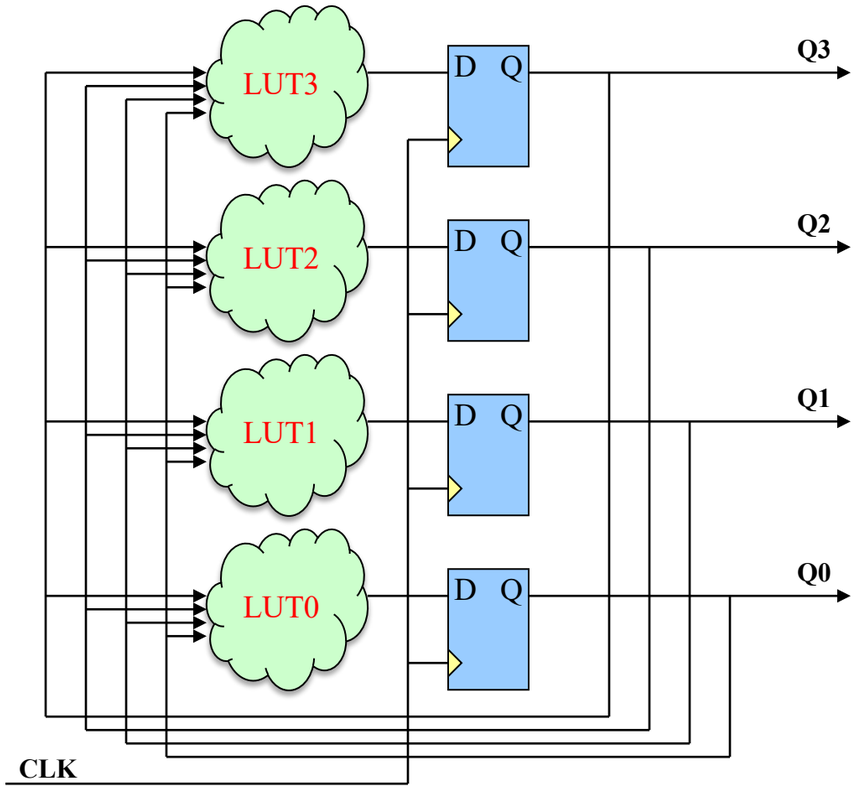
- The Multiplicity Encoder simply counts number of 1's in the input array.
- Typical implementation uses 3-to-2 reducers (full adders).
- In FPGA, one may consider 6,7-to-3 reducers (full adders or encoders).

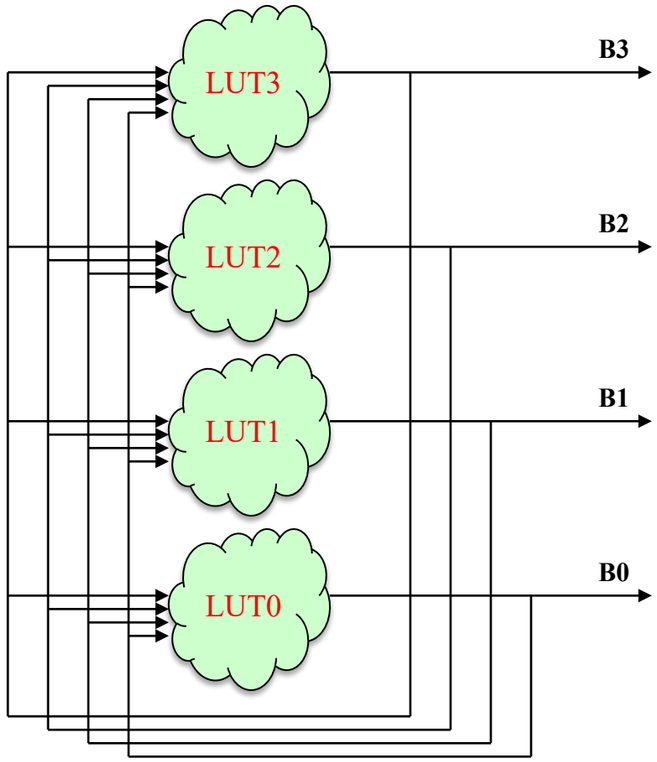




Gray Code

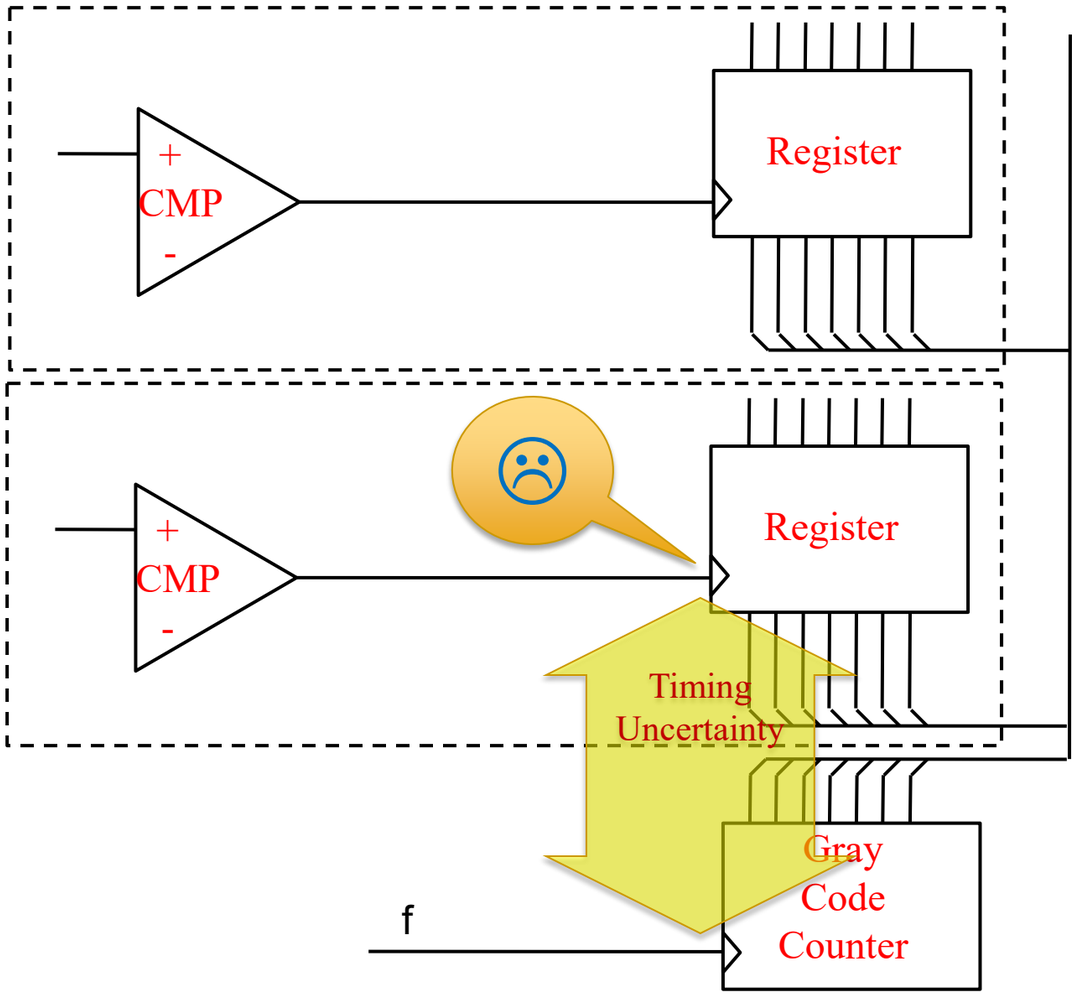
Gray Code Counter vs Gray Code Oscillator



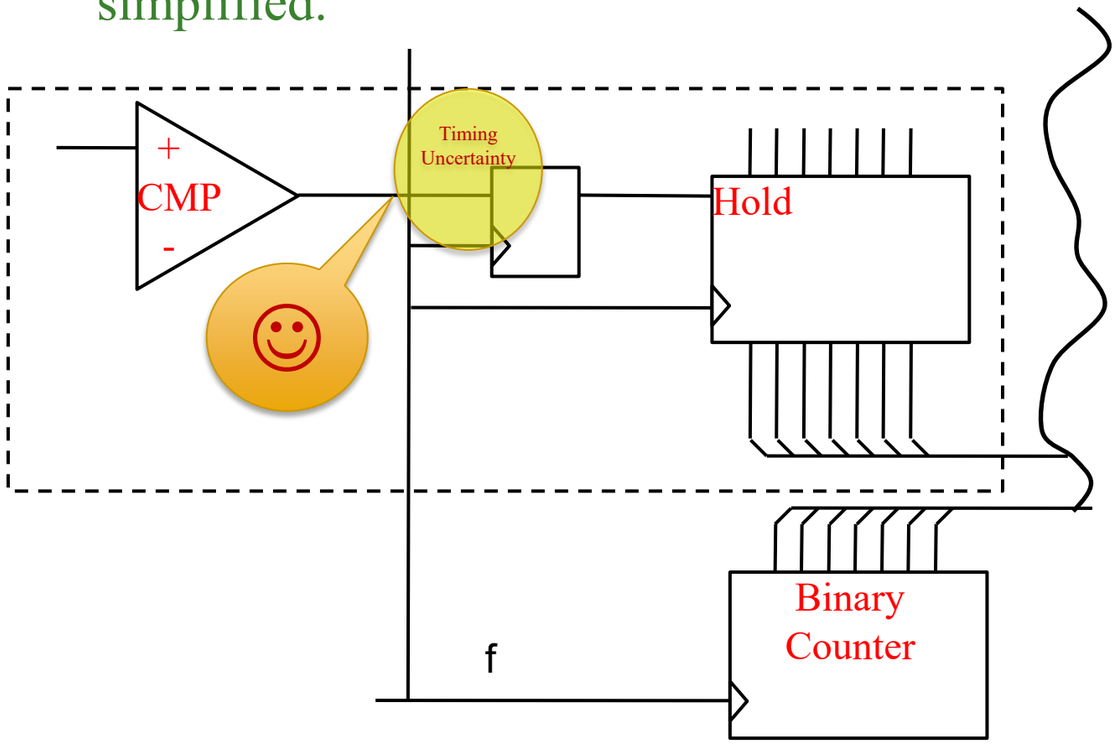


- The Gray code counter or oscillator changes a single bit when steps to next state.
- The Gray code counter steps to next state at CLK leading edge.
- The Gray code oscillator steps to next state spontaneously.

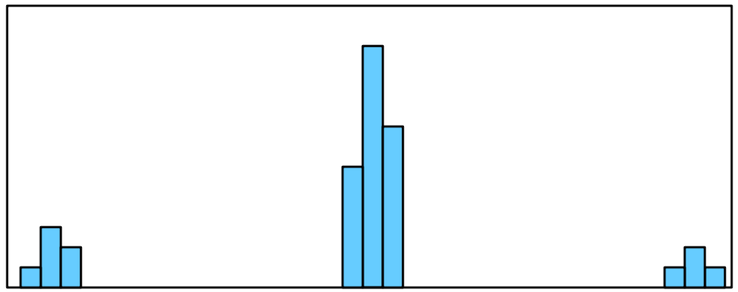
Gray Code Counter?

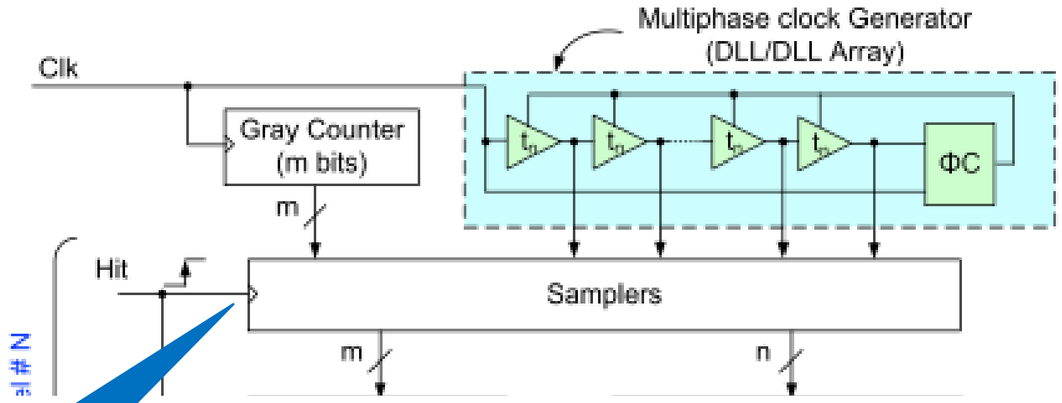


- Some low resolution TDC may use Gray Code Counter.
- All bits must be distributed with good delay match and the output results must be translated.
- With small circuit adjustment to confine the timing uncertainty, many things are simplified.



“Outlier”





Hit to the CK port
Timing uncertainty
while capturing
coarse time

- New TDC designers may see “outlier” issue, i.e., ghost peaks +- 32 (64) bins.
- The “outlier” issue is due to timing uncertainty while capturing coarse time when “Hit” is fed to the CK port of the D-FF.
- There are solutions, but the whole issue can be avoided from beginning.

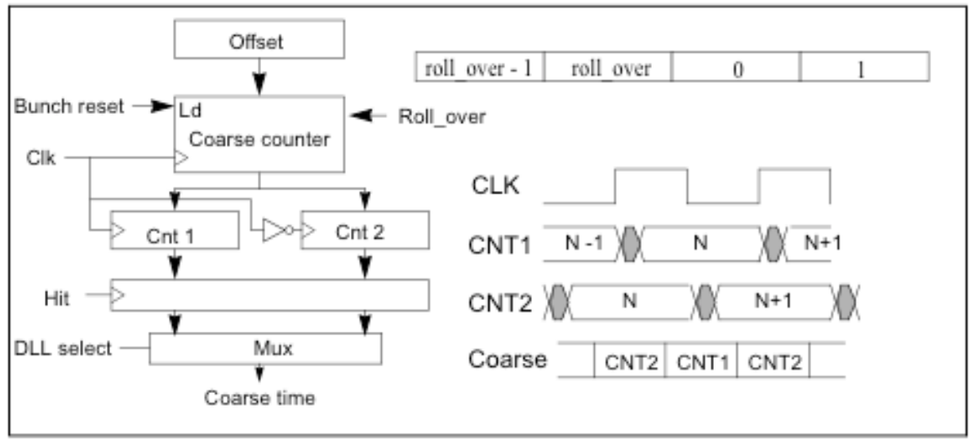
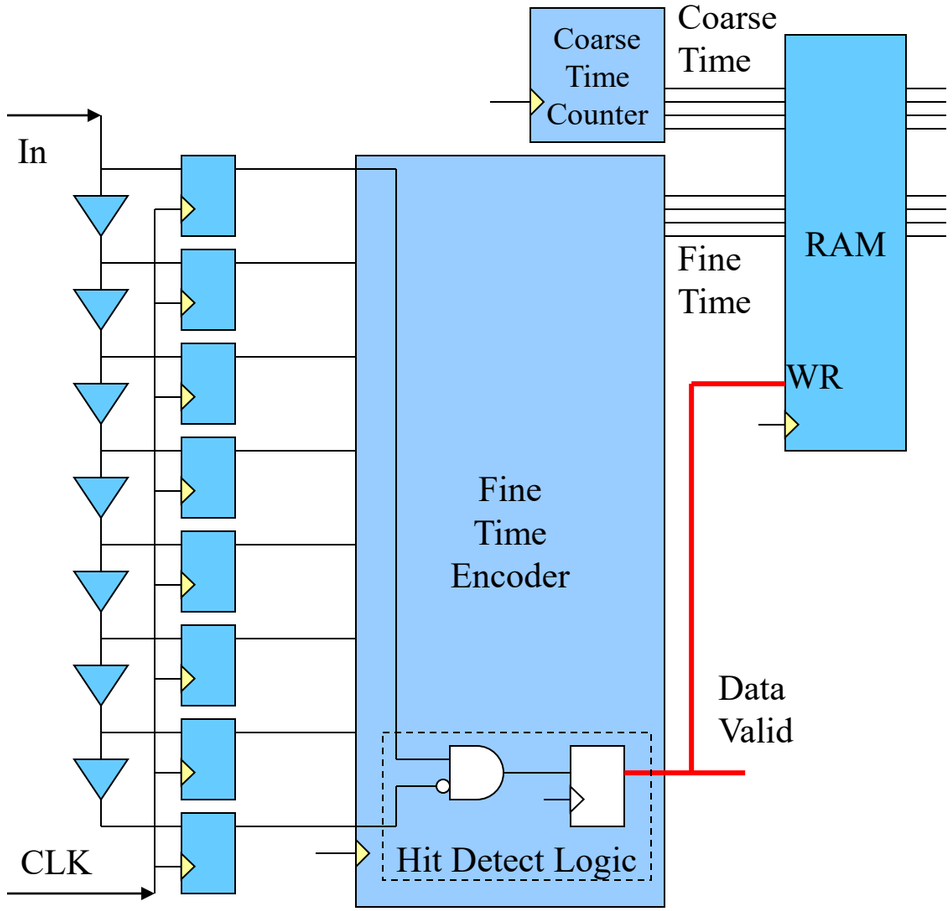


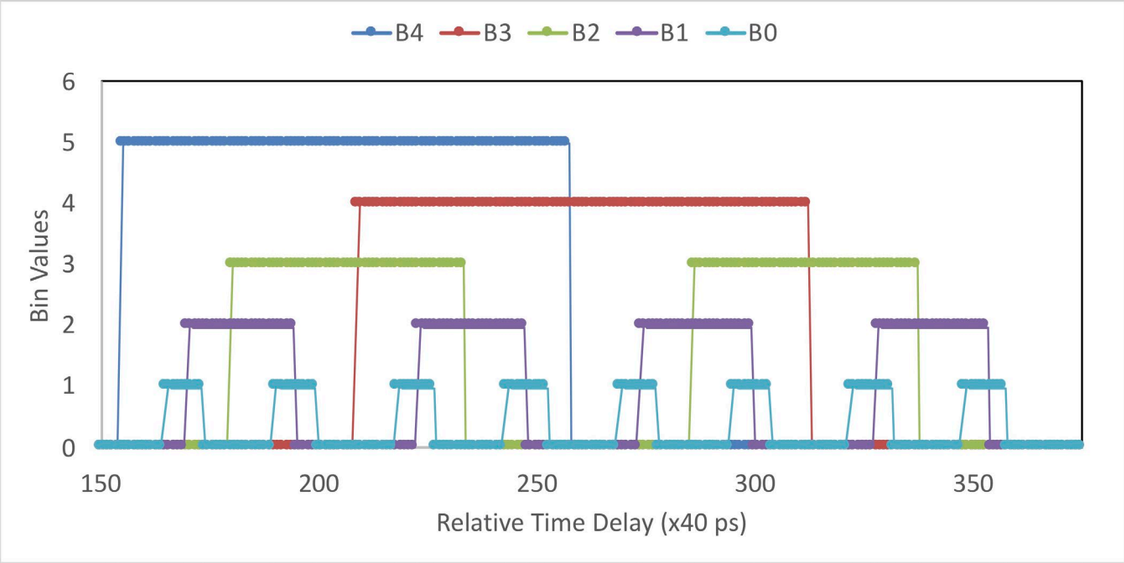
Fig. 6 Phase shifted coarse time counters loaded at hit.

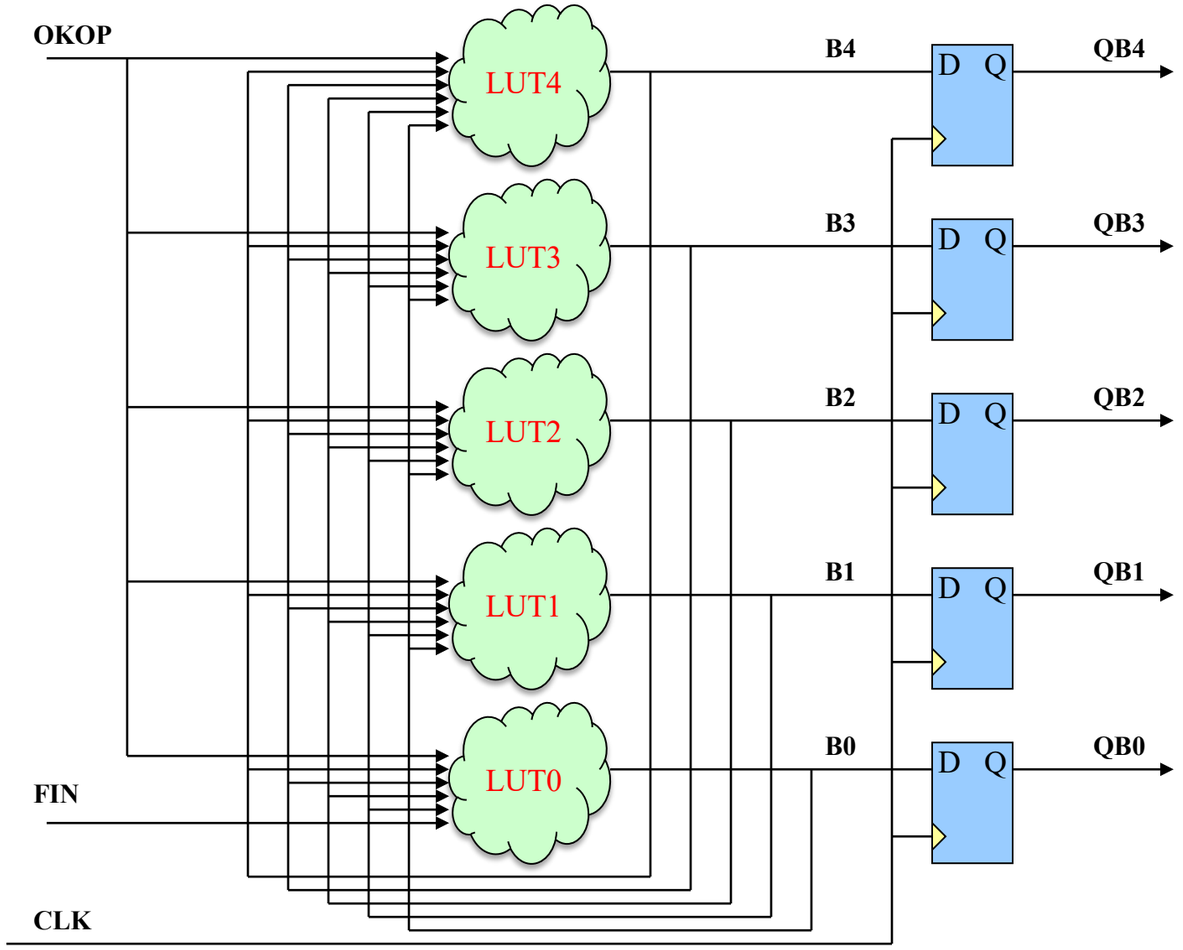
Coarse Time Counter in FPGA TDC



- The FPGA structure forced designers to feed CLK into the CK port of the D-FF.
- Timing uncertainty is confined at the input of the register array.
- The coarse time counter timing condition is satisfied automatically.

Gray Code Oscillator Based TDC

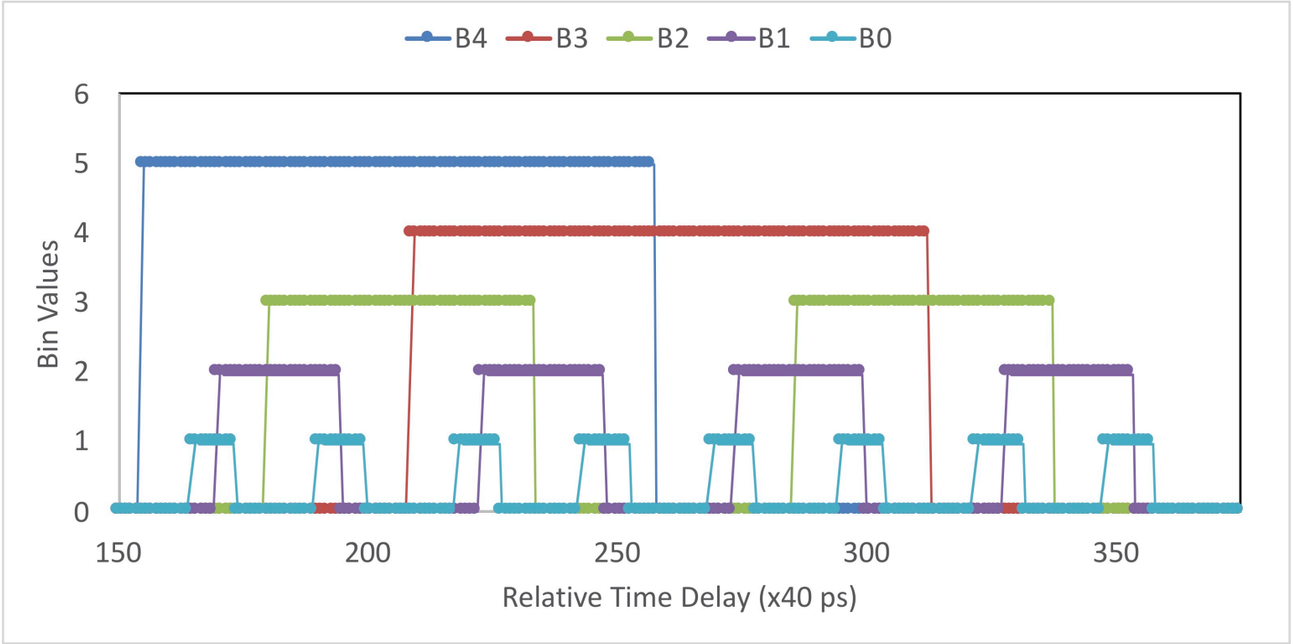


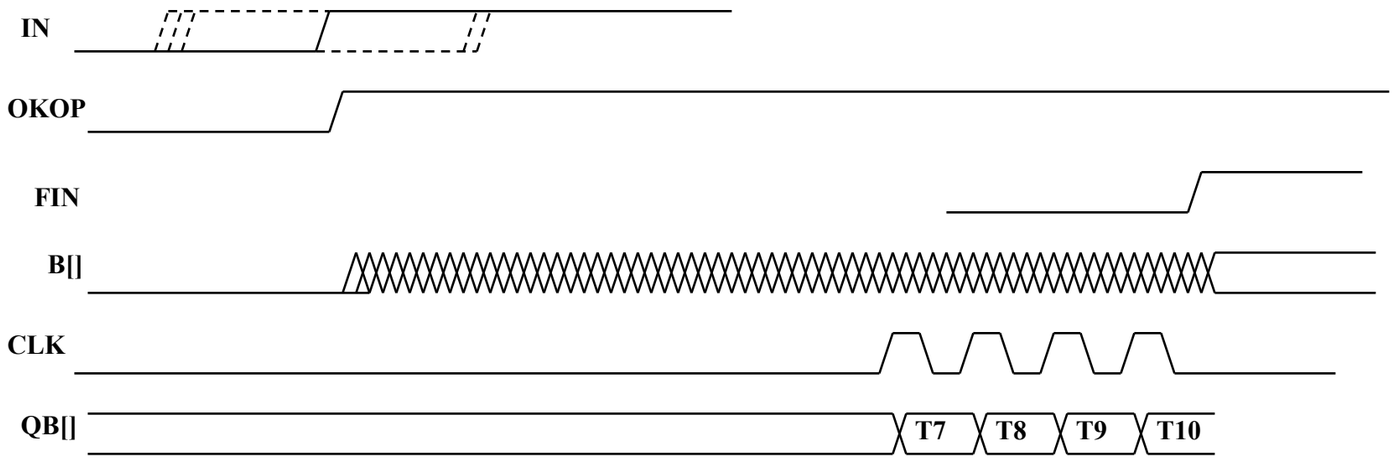


- The Gray code oscillators have wide application including TDC.
- Typical bin width: 100 to 500 ps.
- Improvements are possible. (See: Simão Araújo, et. al.)

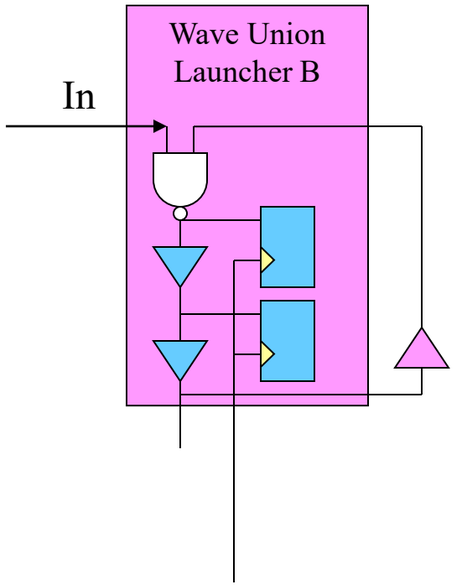
Operation of Gray Code Oscillator Based TDC

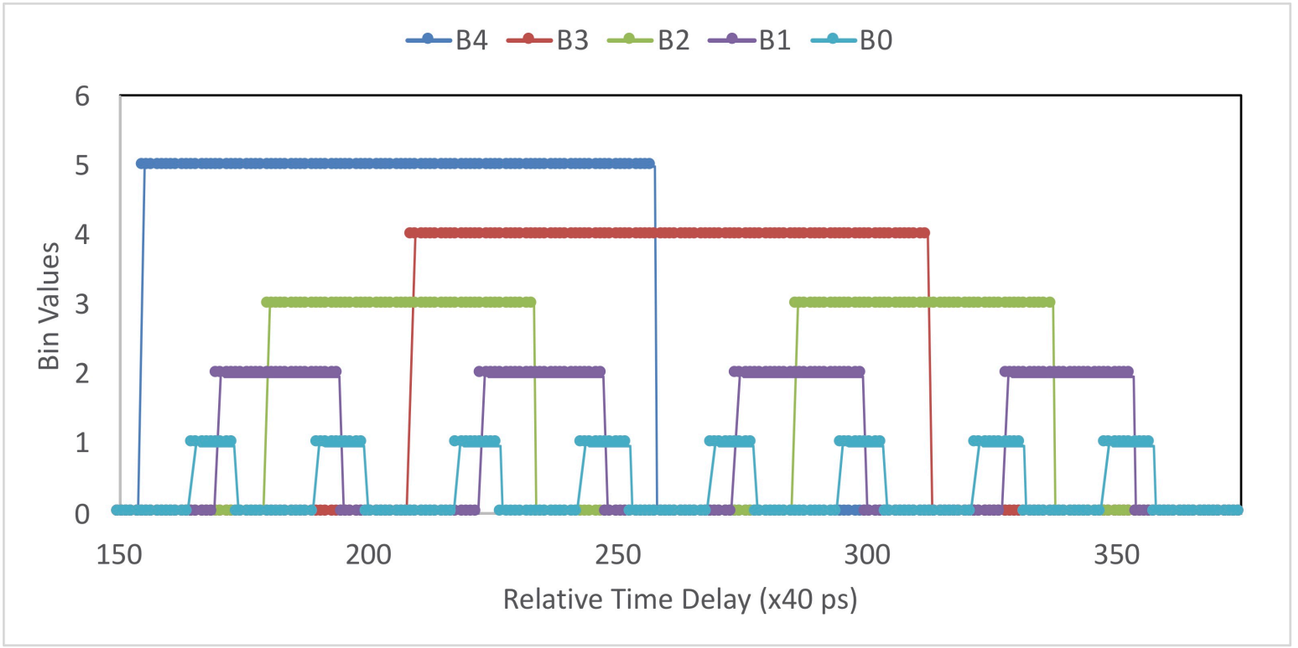
- The Gray code oscillator runs after IN signal arrives.
- The code is captured at clock edges.
- Multiple measurements are possible.





Two-Step Ring Oscillator





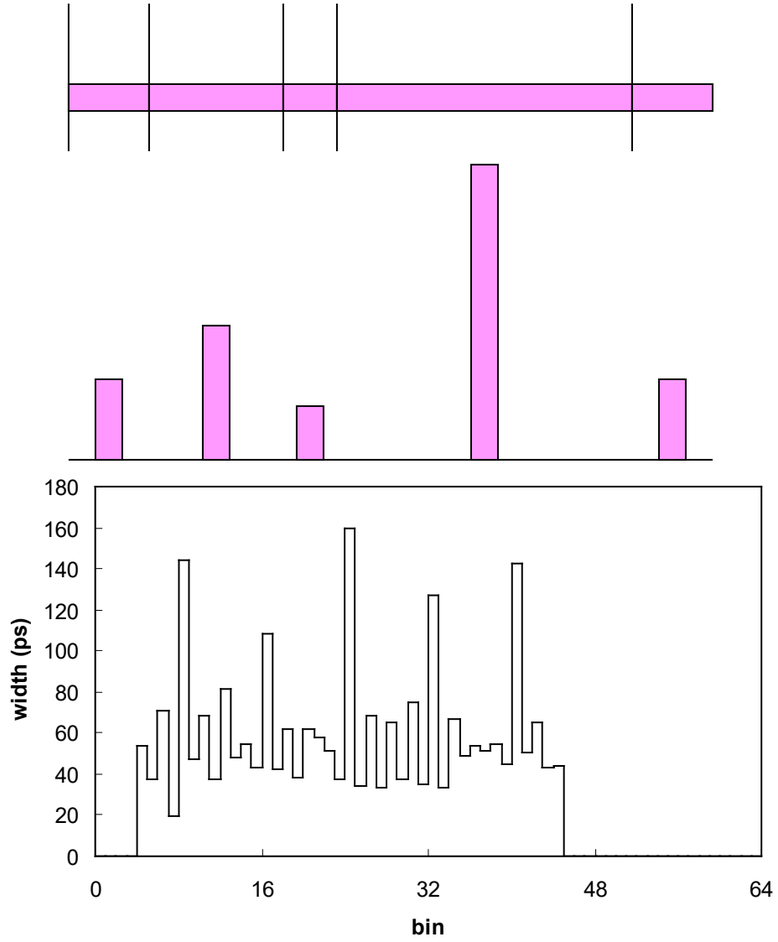
In	B0	B1
0	1	1
1	0	1
1	0	0
1	1	0
1	1	1

- The first two bits of a ring oscillator can be viewed as part of a Gray code oscillator.
- The propagation delay of the delay cell is in general shorter than one in Gray code oscillator bits.
- Consider RO + counter scheme?

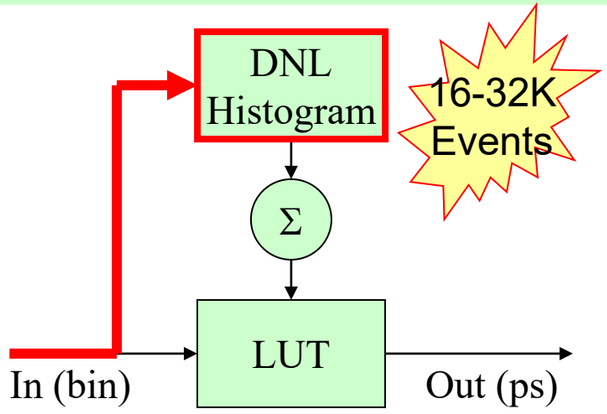
Random Hits for Calibration?

Bin-by-Bin Code Density Calibration

- TDC digitize hits with evenly spread arrival times.
- A histogram is booked.
- Number of counts in each bin is proportional to the width of the bin.

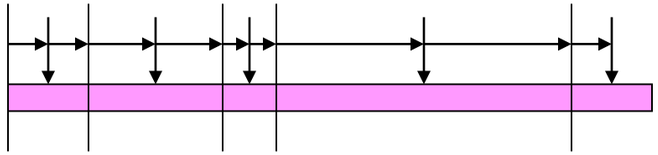


- In the auto calibration process, a bin width histogram (DNL histogram) is first booked.
- More counts are accumulated in wider bins.

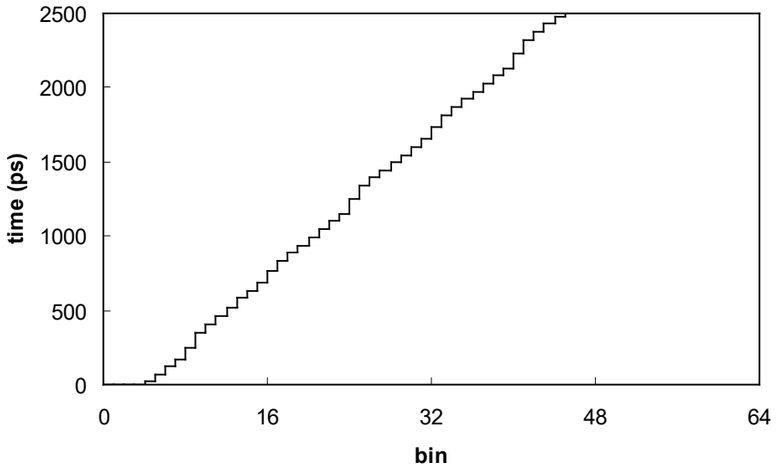


Generating Lookup Table

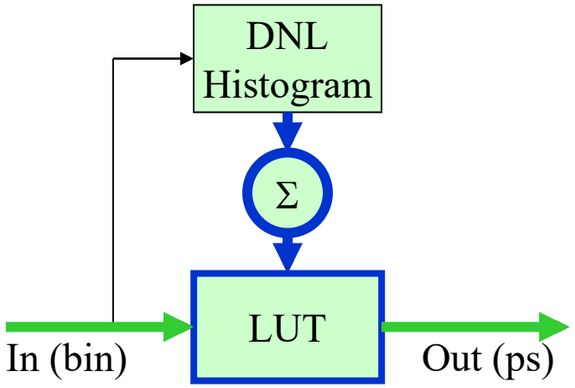
- The widths of the bins are accumulated to form a lookup table.
- Do not forget the half-width of the current bin. (calibrating to the center of the bin)



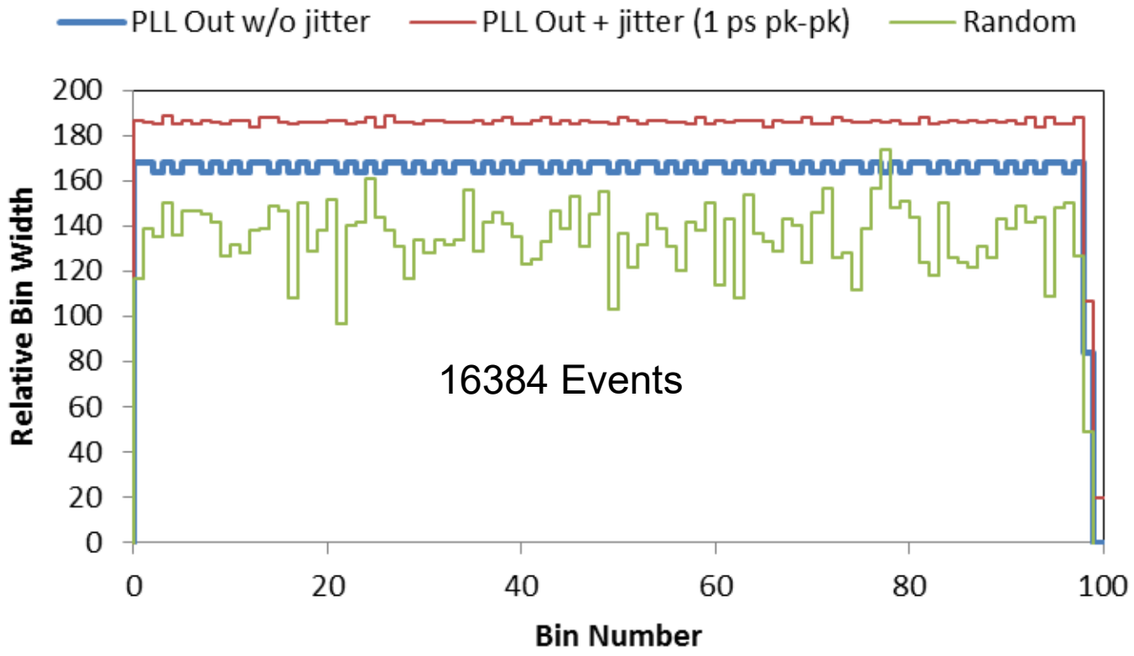
$$t_n = \frac{w_n}{2} + \sum_{k=0}^{n-1} w_k$$

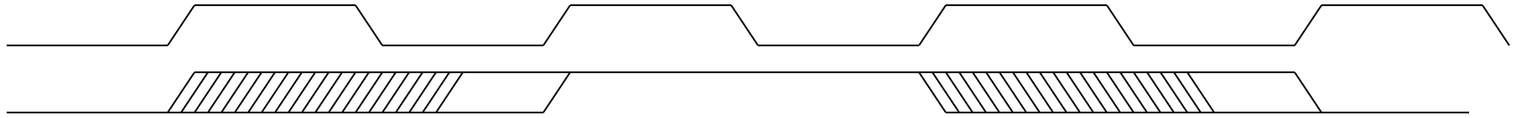


- Bin widths are summed up into the calibration lookup table.
- Note that the values represent times of the centers of the bins.



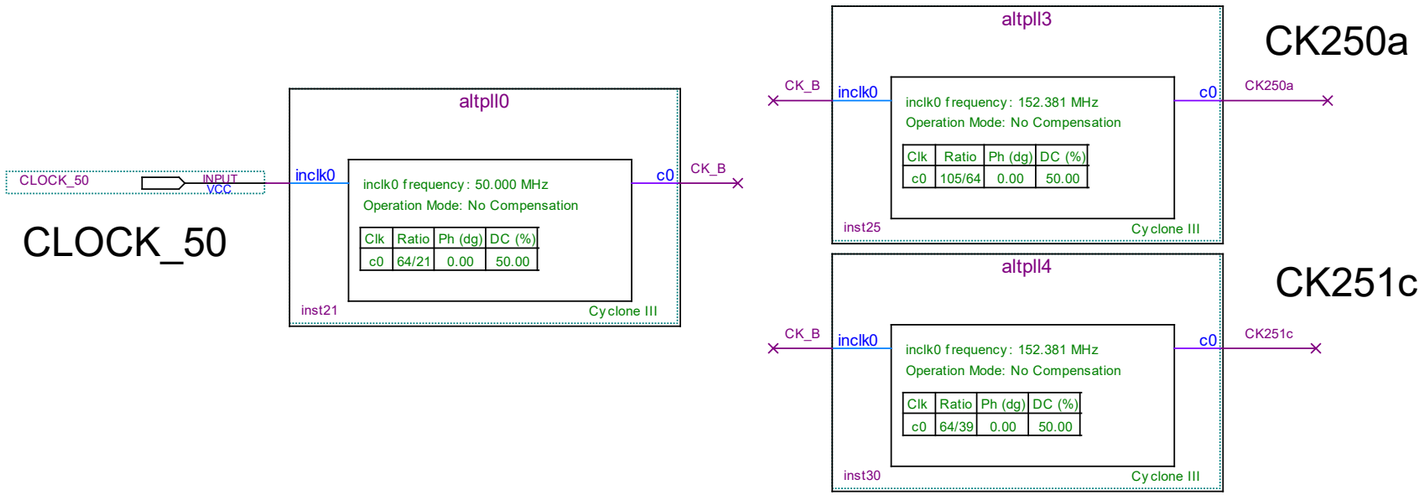
Random != Evenly Spread





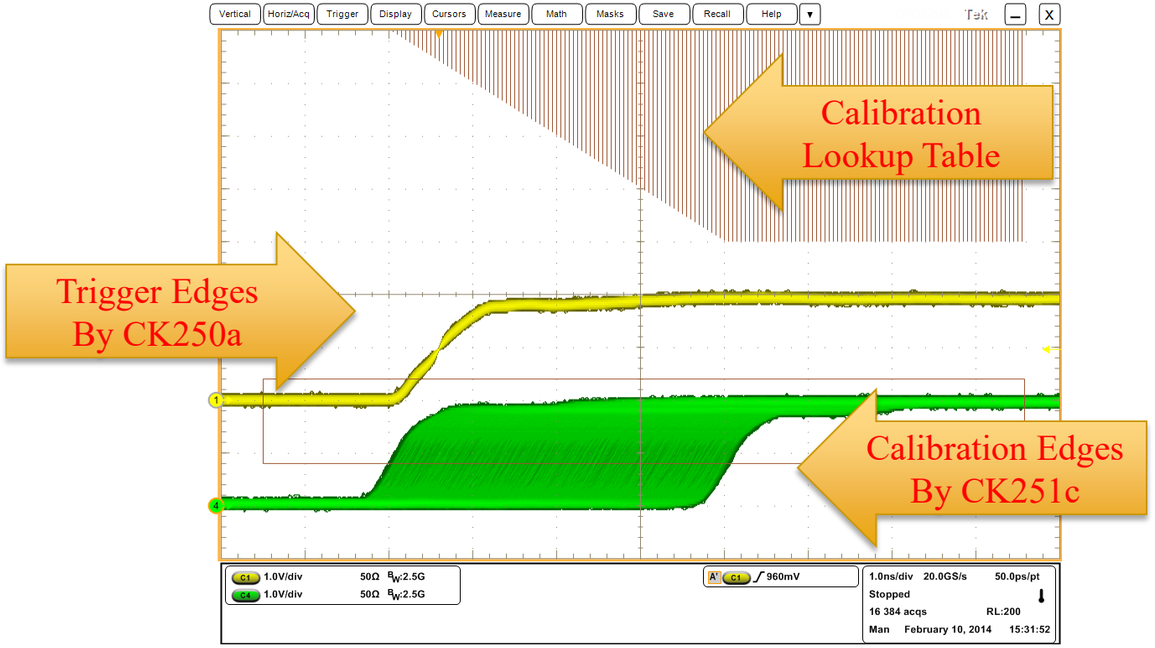
- The random hits have statistical fluctuation, and the variation is large with limited calibration events.
- Hits with evenly spread arrival times are more desirable for calibration.

Generating Clocks with Smooth Phase Drift Using Cascaded PLL



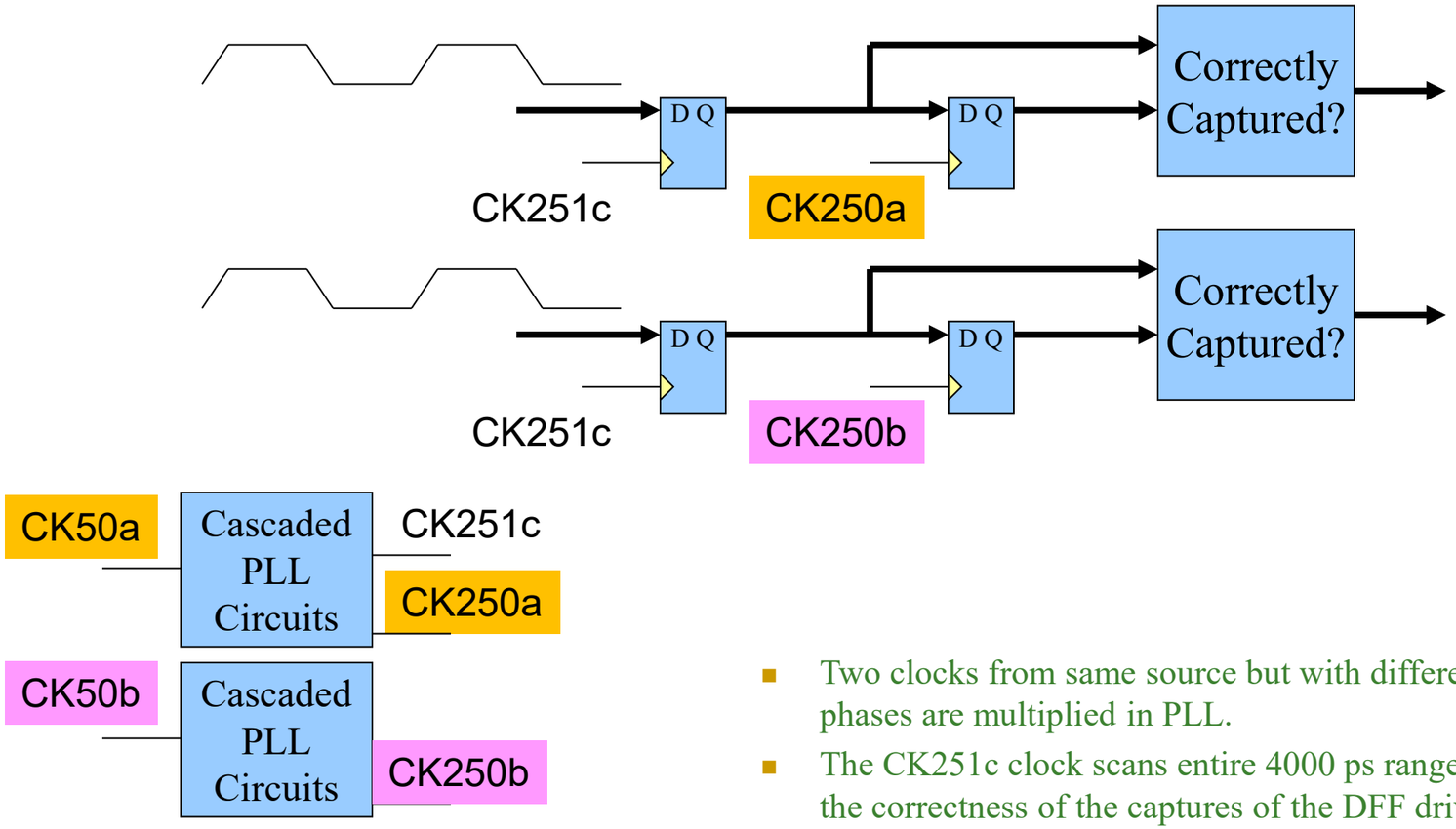
- Two stages of PLL circuits are cascaded together.
  - f(CK250a) = 250 MHz
  - f(CK251c) = 250.06 MHz
  - f(CK251c) = (4096/4095)*f(CK250a)
  - T(CK250a) - T(CK251c) = 0.97 ps.

Test Result in an Oscilloscope Screen Captur



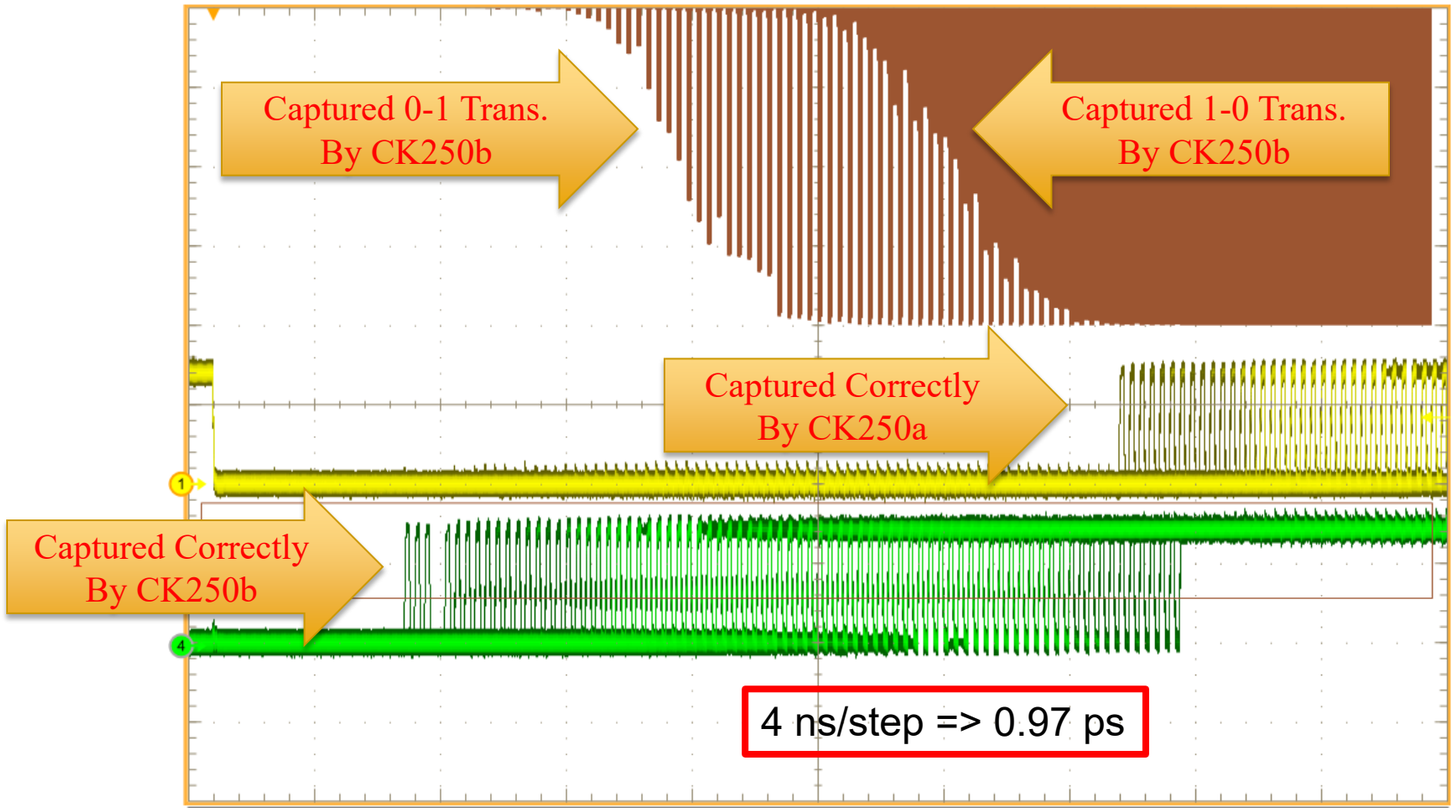
- A total of 16384 Calibration edges are collected.
- Entire 4000 ps range are scanned 4 times (4*4096 = 16384).
- The histogram (with 50 ps/bin) serves as a demonstration of calibration lookup table.

Clock Phase Measurement, Another Application



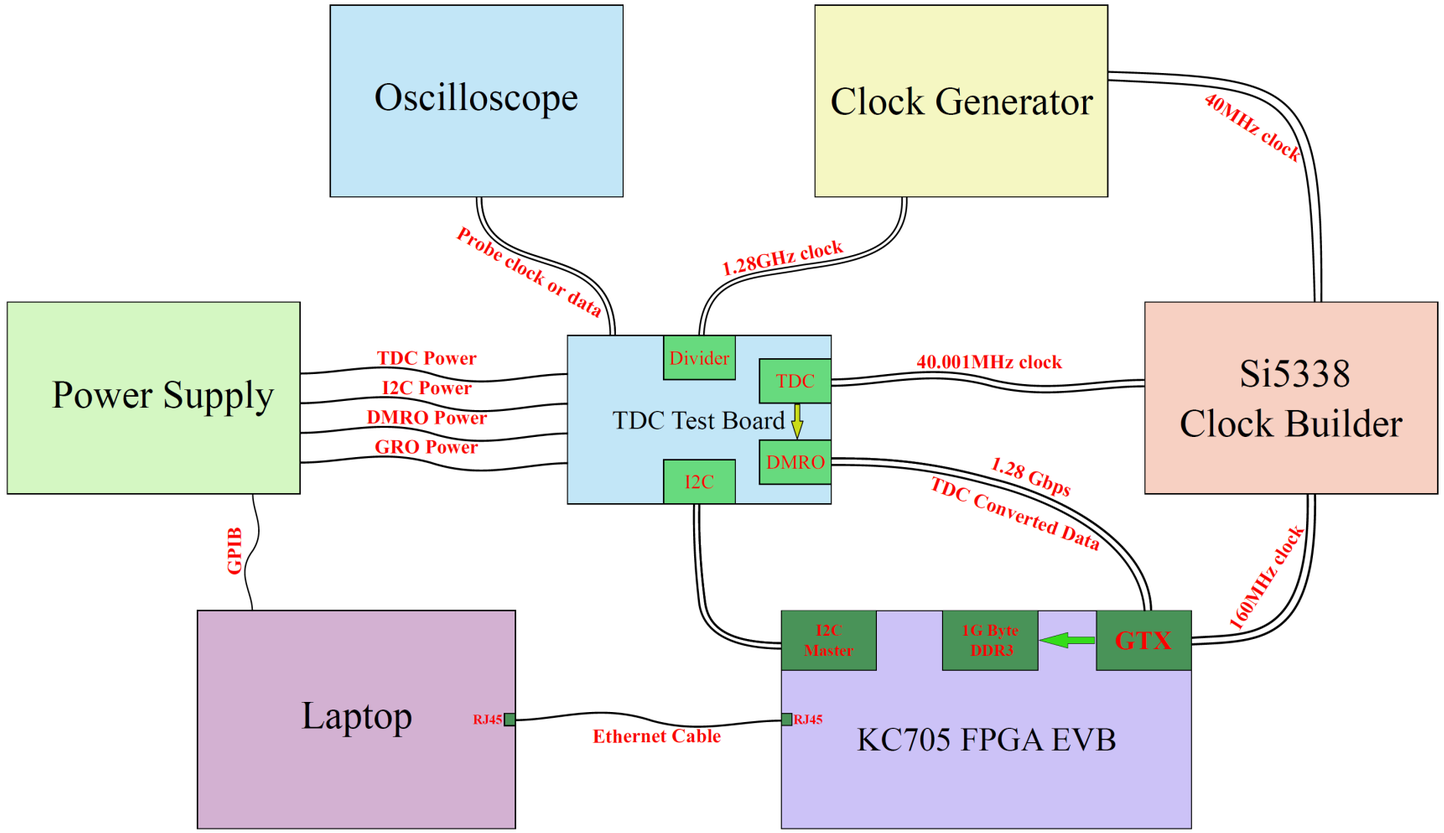
- Two clocks from same source but with different phases are multiplied in PLL.
- The CK251c clock scans entire 4000 ps range and the correctness of the captures of the DFF driven by two clocks are checked.

Screen Capture



- The phase difference of CK250a and CK250b can be measured after CK251c scans through.
- The 0-1 and 1-0 transitions have different setup time.

Generating Clocks with Smooth Phase Drift Using External PLL



- The TDC in the test setup uses 40 MHz to drive system.
- The Si5338 device generates 40.001 MHz to create input hits.
- The smooth phase drift provides good calibration.

The “Any-Frequency” Clock Generator

SILICON LABS

Si5338

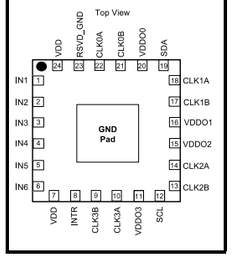
I²C-Programmable Any-Frequency, Any-Output Quad Clock Generator

Features

- Low power MultiSynth™ technology enables independent, any-frequency synthesis on four differential output drivers
- PCIe Gen 1/2/3/4 Common Clock and Gen 3 SRNS compliant
- Highly-configurable output drivers with up to four differential outputs, eight single-ended clock outputs, or a combination of both
- Low phase jitter of 0.7 ps RMS typ
- High precision synthesis allows true zero ppm frequency accuracy on all outputs
- Flexible input reference:
  - External crystal: 8 to 30 MHz
  - CMOS input: 5 to 200 MHz
  - SSTL/HSTL input: 5 to 350 MHz
  - Differential input: 5 to 710 MHz
- Independently configurable outputs support any frequency or format:
  - LVPECL/LVDS: 0.16 to 710 MHz
  - HCSL: 0.16 to 250 MHz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
- Independent output voltage per driver: 1.5, 1.8, 2.5, or 3.3 V
- Single supply core with excellent PSRR: 1.8, 2.5, 3.3 V
- Independent frequency increment/decrement feature enables glitchless frequency adjustments in 1 ppm steps
- Independent phase adjustment on each of the output drivers with an accuracy of ≤20 ps steps
- Highly configurable spread spectrum (SSC) on any output:
  - Any frequency from 5 to 350 MHz
  - Any spread from 0.5 to 5.0%
  - Any modulation rate from 33 to 63 kHz
- External feedback mode allows zero-delay mode
- Loss of lock and loss of signal alarms
- I²C/SMBus compatible interface
- Easy to use programming software
- Small size: 4 x 4 mm, 24-QFN
- Low power: 45 mA core supply typ
- Wide temperature range: –40 to +85 °C

Ordering Information:
See page 42.

Pin Assignments

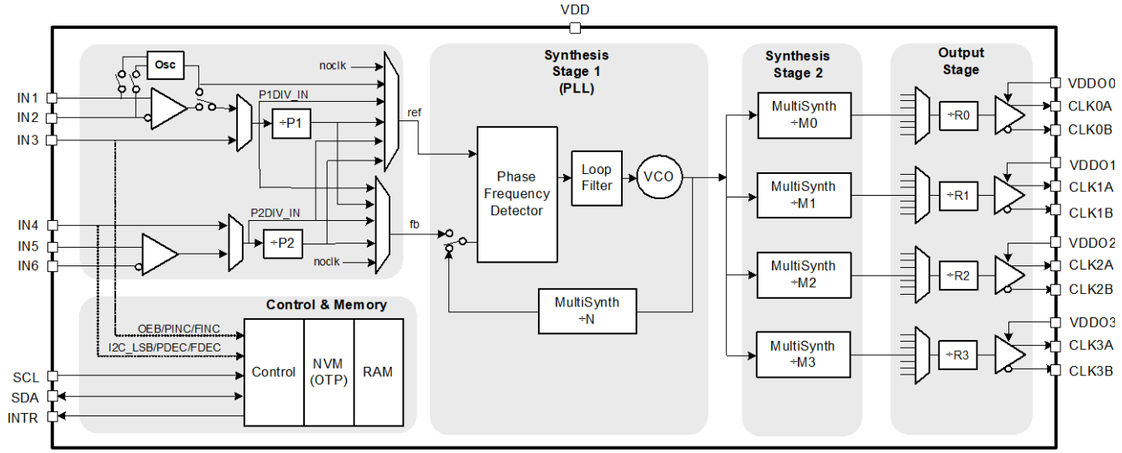


Applications

- Ethernet switch/router
- PCIe Gen1/2/3/4
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

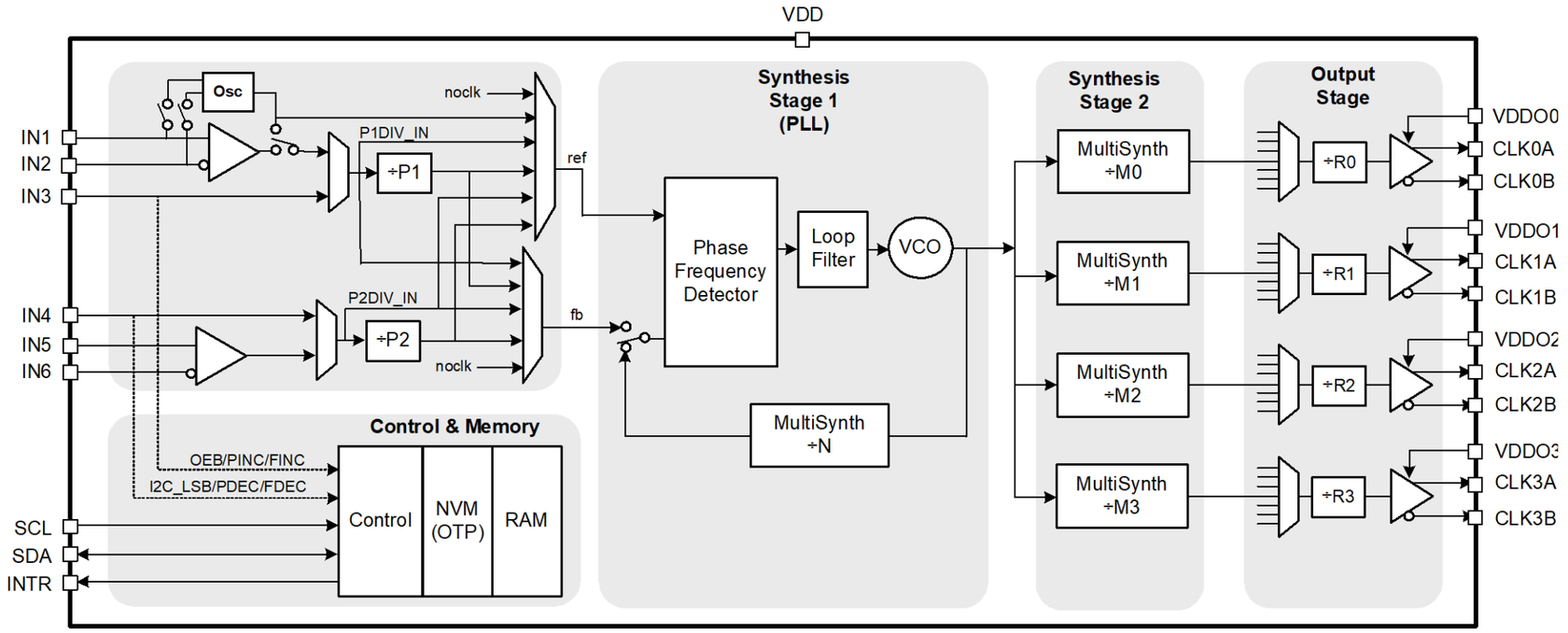
Description

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four output drivers. This timing IC is capable of replacing up to four different frequency crystal oscillators or operating as a frequency translator. Using its patented MultiSynth™ technology, the Si5338 allows generation of four independent clocks with 0 ppm precision. Each output clock is independently configurable to support various signal formats and supply voltages. The Si5338 provides low-jitter frequency synthesis in a space-saving 4 x 4 mm QFN package. The device is programmable via an I²C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply. I²C device programming is made easy with the ClockBuilder™ Desktop software available at www.silabs.com/ClockBuilder. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

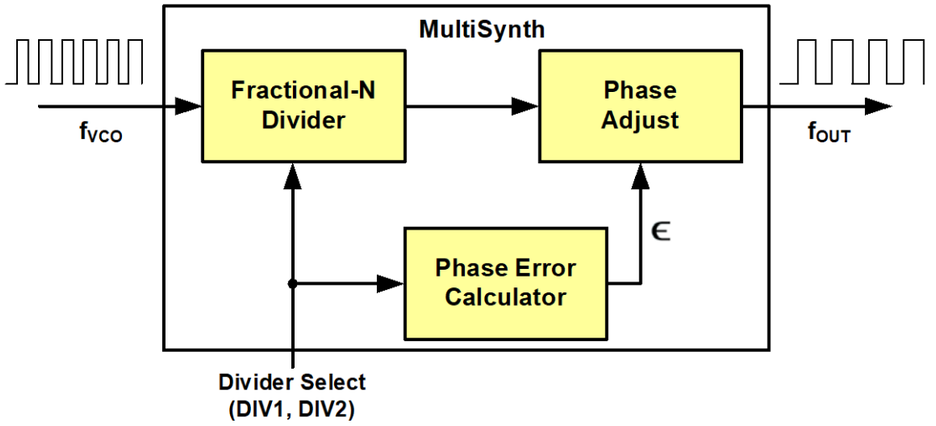


- The Si5338 device is capable to generate several clocks with different frequencies without integer ratio.
- Similar devices are useful in design of systems.

The “MultiSynth”



- The “MultiSynth” approach allows generating fractional ratio of frequencies.



Summary

- We don't want to "reinventing wheels" in general. But sometimes, it is useful and beneficial to rethink some "well-known" concepts in our fields and often a better understanding on these concepts may yield schemes and designs with better performance.
- START/STOP => IN/CLK
  - Multiple measurements, calibration, wave union TDC
- Exact Bin Width => Arbitrary Bin Width
  - TDC in more platform, new scheme, faster, lower power consumption etc.
- Gray Code Counter => Gray Code Oscillator
  - Low resource usage
- Random Hits => Hits with Evenly Spread Arrival Time
  - Better calibration performance


The End
Thanks