A 10 Gbps Driver/Receiver ASIC and Optical Modules for Particle Physics Experiments

Xing Huang, Datao Gong, Suen Hou, Guangming Huang, Chonghan Liu, Tiankuan Liu, Ming Qi, Hanhan Sun, Quan Sun, Li Zhang, Wei Zhang, Xiandong Zhao, and Jingbo Ye

***Abstract*— We present the design and test results of a Drivers and Limiting AmplifierS ASIC operating at 10 Gbps (DLAS10) and three Miniature Optical Transmitter/Receiver/Transceiver modules (MTx+, MRx+, and MTRx+) based on DLAS10. DLAS10 can drive two Transmitter Optical Sub-Assemblies (TOSAs) of Vertical Cavity Surface Emitting Lasers (VCSELs), receive the signals from two Receiver Optical Sub-Assemblies (ROSAs) that have no embedded limiting amplifiers, or drive a VCSEL TOSA and receive the signal from a ROSA, respectively. Each channel of DLAS10 consists of an input Continuous Time Linear Equalizer (CTLE), a four-stage limiting amplifier (LA), and an output driver. The LA amplifies the signals of variable levels to a saturation amplitude of 800 mV (peak-peak). The output driver drives VCSELs or impedance-controlled traces. DLAS10 is fabricated in a 65 nm CMOS technology. The die is 1 mm × 1 mm. DLAS10 is packaged in a 4 mm × 4 mm 24-pin quad-flat no-leads (QFN) package. DLAS10 has been tested in MTx+, MRx+, and MTRx+ modules. Both measured optical and electrical eye diagrams pass the 10 Gbps eye mask test. The input electrical sensitivity is 40 mVp-p, while the input optical sensitivity is -12 dBm. The total jitter of MRx+ is 29 ps (P-P) with a random jitter of 1.6 ps (RMS) and a deterministic jitter of 9.9 ps. Each MTx+/MRx+ module consumes 82.6 mW/ch and 174.4 mW/ch, respectively.**

***Index Terms*— Analog integrated circuits, High energy physics instrumentation, Optical transceivers.**

I. Introduction

HIGH-speed optical data transmission between on-detector and off-detector electronics is of particular interest due to the increasing data volume in particle physics experiments [1]. The generic optical link in particle physics experiments, including the transmitting link and the receiving link with the same structure and opposite directions, is shown in Fig. 1. The on-detector optical transmitter converts the electrical signals from the serializer to optical signals transmitted through fibers. The on-detector optical receiver converts the optical signals from the off-detector to the electrical signals, which will be provided for the deserializer. Through common projects, CERN has demonstrated the lpGBT [2] serializer-deserializer (SerDes) and VTRx+ [3] optical transceiver can be operated up to 10.24 Gbps per fiber. The serializer in lpGBT operates at 5.12 or 10.24 Gbps, while its deserializer at 2.56 Gbps. VTRx+ has four transmitters and one receiver with fibers terminated at a Mechanically Transferable (MT) connector [4] . VTRx+ is only board-mount with a dedicated electric connector. Both the lpGBT ASIC and the VTRx+ optical module have an small footprint and are qualified to be radiation tolerant for applications in the inner trackers of experiments on the LHC. Compared with the inner trackers, on-detector electronics for calorimeters and muon systems have much less stringent requirements in component size and radiation tolerance [5] [6] . The PCBs are also usually larger to house more functions such as the hardware trigger and high precision ADCs. The data channels and the PCB layout are more spread out, making it more natural for the optical transceiver and lpGBT to have an equal number of channels, and collect the digital data through fibers over such a large PCB to the front panel. The size and complexity of the PCB call for an optical transceiver with more robust connectors. Based on the development of the Miniature optical Transmitter /Transceiver MTx/MTRx [7] and Vertical Cavity Surface Emitting Laser (VCSEL) driver LOCld [8] for the ATLAS Liquid Argon Calorimeter (LAr) trigger upgrade [9] , we develop the Drivers and Limiting AmplifierS ASIC, operating at 10 Gbps (DLAS10), in a 65 nm CMOS technology and the corresponding three Miniature optical Transmitter /Receiver/Transceiver (MTx+, MRx+, and MTRx+). Comparing with its previous prototype of a dual-channel VCSEL driver [10] , DLAS10 has two channels with higher gain to sense smaller amplitude of the input signal, and each can be operated up to 10.24 Gbps and can be configured to be two VCSEL drivers, or two receiver limiting amplifiers, or one driver and one receiver. Matching DLAS10 with a TOSA and a ROSA with only Trans-Impedance Amplifier (TIA), and with a custom optical coupler, MTx+/MRx+/MTRx+ offer an economical option with a robust electrical connector and receives fibers with the LC connectors [11] . The height of the three variants MTRx+, MTx+, and MRx+ is below 6 mm. The modules can be both board and panel mountable. The modules provide the combination of an optical transceiver, dual-channel optical transmitters, and dual-channel optical receivers for on-detector readout electronics outside the inner trackers.

This work was supported by SMU's Dedman Dean's Research Council Grant.

Xing Huang, Hanhan Sun, Li Zhang, and Wei Zhang are PhD candidates of Central China Normal University, Wuhan, Hubei 430079, China. They are visiting scholars at Southern Methodist University, Dallas, TX 75205, USA for this work.

Datao Gong (corresponding author, e-mail: dgong@mail.smu.edu), Chonghan Liu, Tiankuan Liu, and Jingbo Ye are with Southern Methodist University, Dallas, TX 75205, USA.

Suen Hou is with Academia Sinica, Nangang, Taipei 11529, Taiwan.

Guangming Huang is with Central China Normal University, Wuhan, Hubei 430079, P.R. China.

Ming Qi is with Nanjing University, Nanjing, Jiangsu 210008, China.

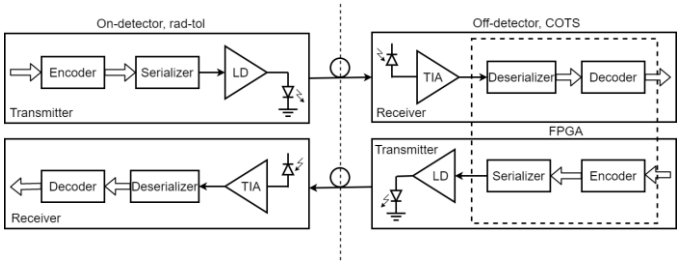


Fig. 1. Optical link in particle physics experiments.

II. Design of DLAS10

A. Structure of DLAS10

Each channel of DLAS10 consists of an input equalizer (EQ), a four-stage Limiting Amplifier (LA), and an output driver. Two channels share an Inter-Integrated Circuit (I^2C) block. Fig. 2 shows that the block diagram of DLAS10 driving two TOSAs, receiving the signal from a ROSAs with only TIA, and connecting to a TOSA and a ROSA. DLAS10 is powered by a single 1.2 V power supply, whereas TOSAs and ROSAs are powered by a 3.3 V power supply. DLAS10 is AC coupled to TOSAs and ROSAs.

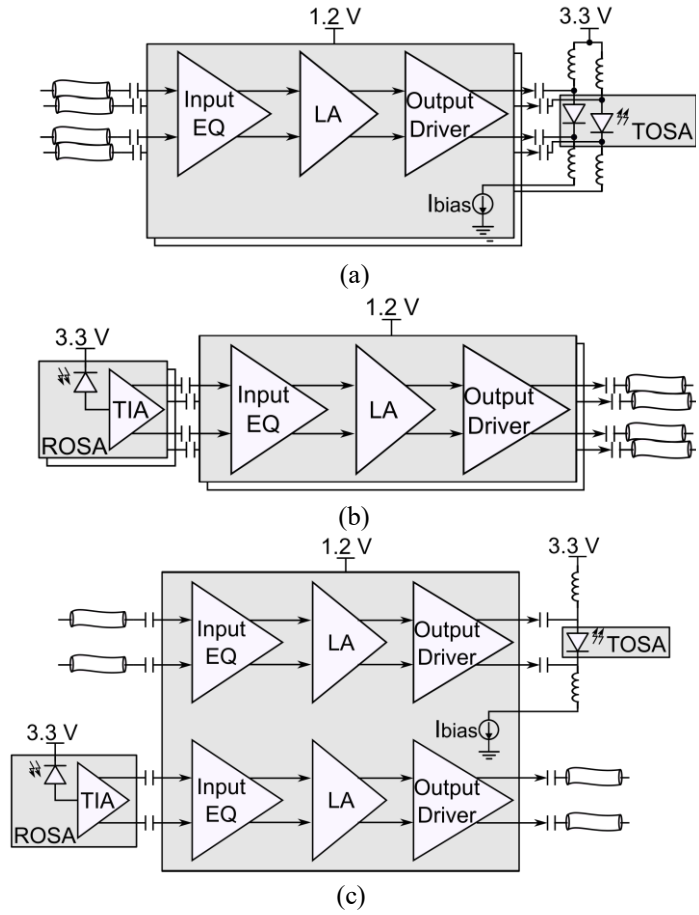


Fig. 2. Block diagrams of DLAS10 in the use case of MTx+ (a), MRx+ (b), and MTRx+ (c).

B. Input equalizer

The schematic of the input EQ is shown in Fig. 3. The termination of the differential input was implemented with two 50 Ω resistors R_3 and R_4 connected in series. The input common-mode voltage (VCM) is 800 mV or 2/3 of Vdd. The conventional Continuous-Time Linear Equalization (CTLE) [12] with source degeneration using a combination of a capacitor and a variable resistor is implemented to adjust the locations of the zero and poles in the frequency response to compensate for the high-frequency degradation of the input signal due to long transmission lines. The tunable resistor (R_7) is implemented by 6 paralleled NMOS transistors. The CTLE structure adds a programmable zero and pole to compensate the high frequency signal loss of input signal and the inductor L1 introduces another fixed zero to further extend the bandwidth of the input EQ [13] . The minimum input signal level is specified to correspond to the output of a typical TIA from a ROSA. The EQ is programmable with the tuning range from 0.38 GHz to 1.56 GHz and can compensate for signal loss at 5 GHz up to 9.8 dB. The maximum signal amplitude that the equalizer can cope with is 0.8 V.

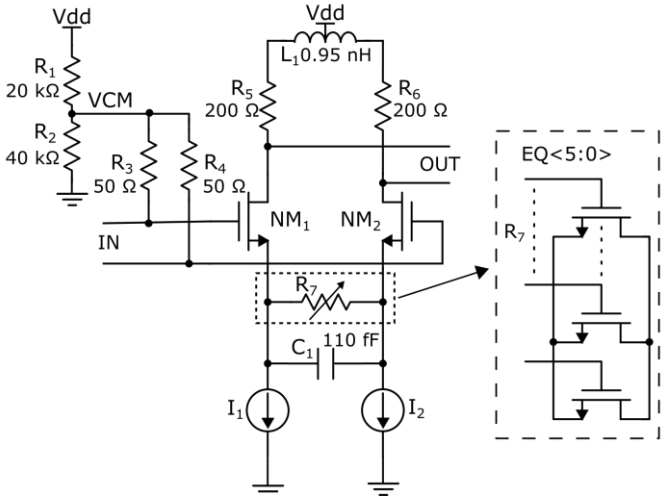


Fig. 3. Schematics of the input EQ with inductive peaking and CTLE.

C. Limiting Amplifier

The LA aims at amplifying a wide range of input signals to the saturation level to drive the output driver, and thereby the output modulation current is independent of the amplitude of the input signal. The schematic of the LA is shown in Fig. 4. To obtain the overall sensitivity, a gain of 24 dB is required. The overall bandwidth of the LA should be larger than 10 GHz [14] . In addition to achieving the gain, maintaining a wide bandwidth at all stages is also a key feature to avoid Inter-Symbol Interference (ISI). A multiple-stage LA with an inductance-peaking technique is adopted [15] . Center-tapped inductors, shared between adjacent amplifier stages [15] , are

Quan Sun is with Fermi National Accelerator Laboratory, Batavia, IL 60510, USA.

Xiandong Zhao was with Southern Methodist University, Dallas, TX 75205, USA. He is now with Washington University in St. Louis, 1 Brookings Dr, St. Louis, MO 63130, USA.

used to save layout area. To accommodate the Process, Voltage, and Temperature (PVT) variations, active feedback is used [16] . The active feedback current (I_{FB}) can be tuned by the I^2C block to obtain a reasonable combination of bandwidth and gain. The simulated bandwidth and gain for LA are 10.5 GHz and 28.4 dB.

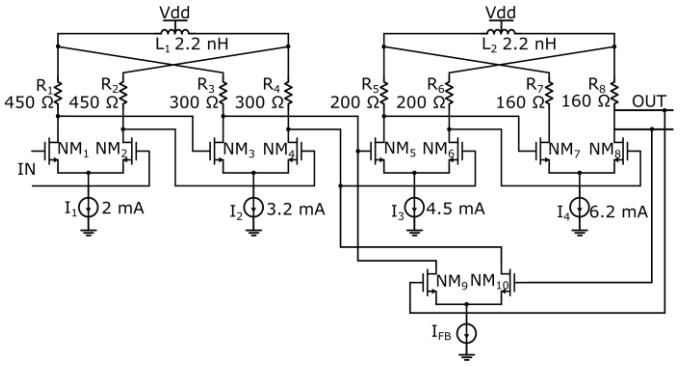


Fig. 4. Schematic of the four-stage LA.

D. Output driver

The schematic of the output driver is shown in Fig. 5. NM_1 and NM_2 are the amplifying transistors that convert voltages to currents. NM_3 and NM_4 form a current mirror. The current source I_{mod} indicates the modulation current generated by a digital-to-analog converter (DAC) and is configured via the I^2C block to adjust the output modulation amplitude for applications as a cable driver or a VCSEL driver. The bias current (I_{bias}) shown in Fig.2 is also generated by a DAC and controlled by the I^2C block. The tuning ranges of the I_{mod} and I_{bias} are both from 0 mA to 10.0 mA with a step of 0.16 mA. The output driver is based on the Current-Mode Logic (CML) structure and has 50 Ω load resistors to match the transmission-line impedance on the Printed Circuit Board (PCB). A large current capability is required to achieve a sufficient output swing.

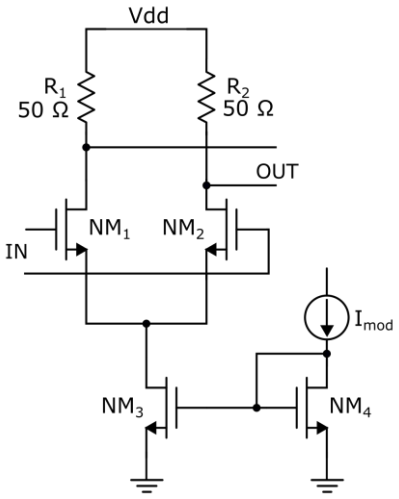


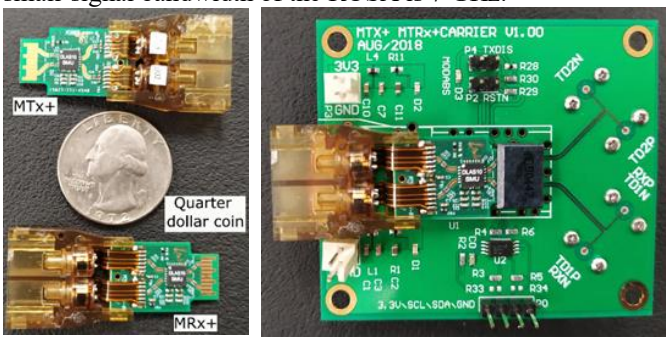
Fig. 5. Schematics of the output driver.

E. Dimension and package

The die of DLAS10 is 1 mm × 1 mm and is packaged in a 4 mm × 4 mm 24-pin Quad-Flat No-leads (QFN) chip.

III. Design of Optical Modules

DLAS10 has been tested in the optical transmitter/receiver (MTx+, MRx+, and MTRx+) modules. These modules are assembled with the custom mechanical latch that couples the module and optical fibers with LC connectors. Fig. 6(a) shows the MTx+ and MRx+ modules compared with a quarter dollar coin. Fig. 6(b) shows the test board with MRx+ mounted. The electrical connector is that for the SFP+ modules. The latch can be anchored to the motherboard when the module is board mounted. It also has an EMI shield that doubles as a plug-in guide when the module is used at a front-panel. The part numbers of the TOSAs and the ROSAs used in the test are Truelight TTF-1F59-427 and TRF-8F59-732, respectively. The typical forward voltage of the TOSA is 2.0 V. The typical small-signal bandwidth of the ROSA is 7 GHz.



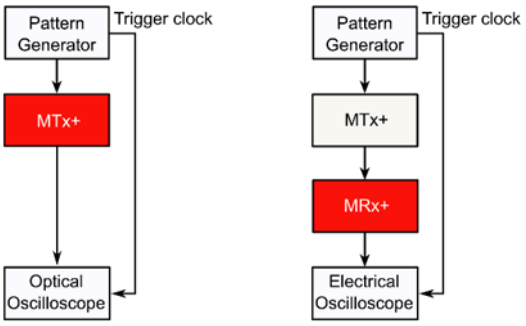
(a) (b)

Fig. 6. (a) Photos of MTx+ and MRx+ compared with a quarter dollar coin; (b) the carrier board with an MRx+ mounted.

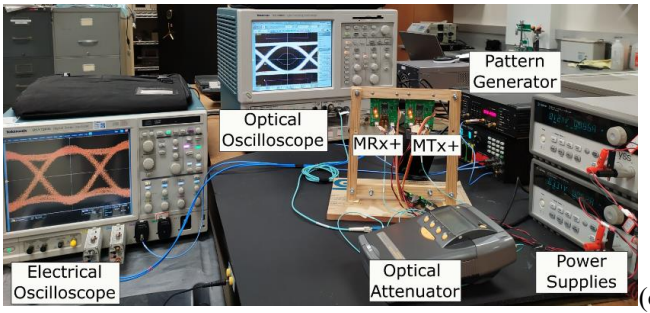
IV. Test Results

A. Test setup

Fig. 7(a) and Fig. 7(b) show the test block diagrams of MTx+ and MRx+, respectively. Fig. 7(c) shows the picture of the test setup. Two DC power supplies (Agilent E3641A) provide 1.2 V and 3.3 V power. A pattern generator (CENTELLAX TG1C1-A with a clock module CENTELLAX PCB12500) provides 10 Gbps Pseudo-Random Binary Sequence (PRBS) signals with various amplitudes and the trigger clock. An optical oscilloscope (Tektronix TDS8000B) captures the optical eye diagrams of MTx+. An electrical oscilloscope (Tektronix DSA72004) measures the electrical eye diagrams of MRx+. For the MRx+ test, MTx+ is the optical source.



(a) (b)

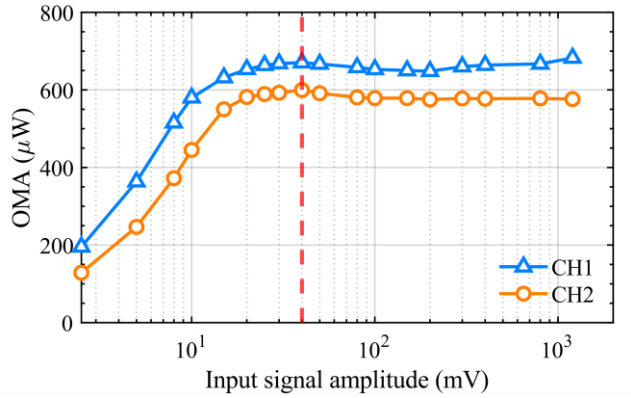


(c)

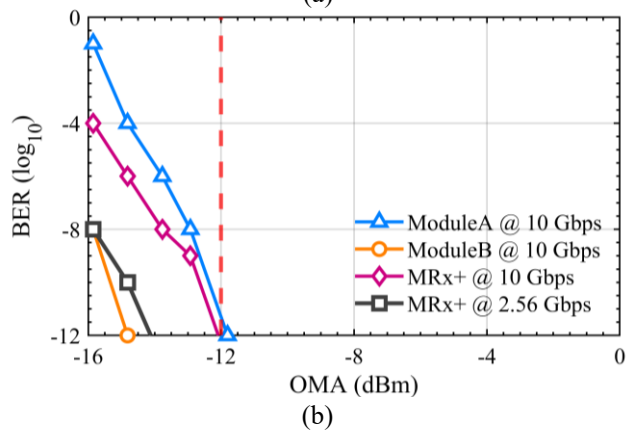
Fig. 7. (a) and (b) Test block diagrams of MTx+ and MRx+, (c) photo of the test setup.

B. Input sensitivity

The input sensitivities of MTx+ and MRx+ were tested by scanning the input signal amplitude. Fig. 8 shows the input sensitivities of MTx+ and MRx+. As can be seen in Fig. 8(a), when the input amplitude exceeds 40 mV, the Optical Modulation Amplitude (OMA) of MTx+ is stable. The input sensitivity of 40 mV is low enough to receive the signal from the ROSA that has no LA. As can be seen in Fig. 8(b), when MRx is operated at 10 Gbps, the input sensitivity of MRx+ is -12 dBm. When the operating rate drops to 2.56 Gbps, the input sensitivity of MRx+ is increased to -14 dBm. The optical input sensitivities of DLAS10 are comparable with those of two commercial optical transceiver modules (marked as A and B in Fig. 8(b)). The measurement difference between Channels 1 and 2 could be introduced by the TOSA's slope efficiency, which varies from 0.09 mW/mA to 0.17 mW/mA.



(a)

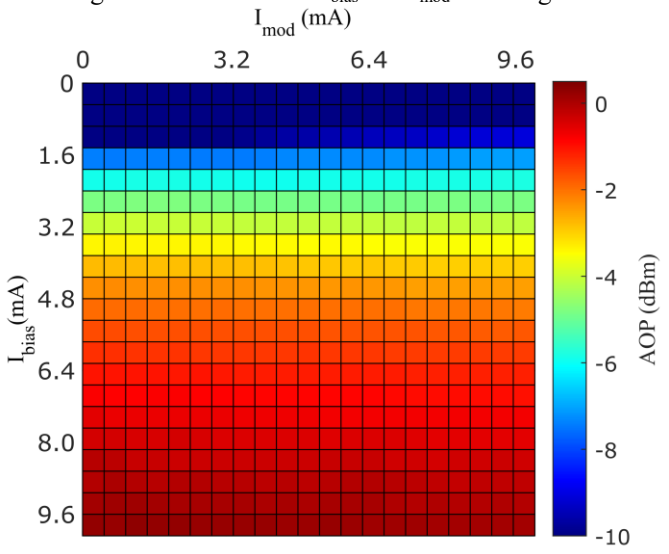


(b)

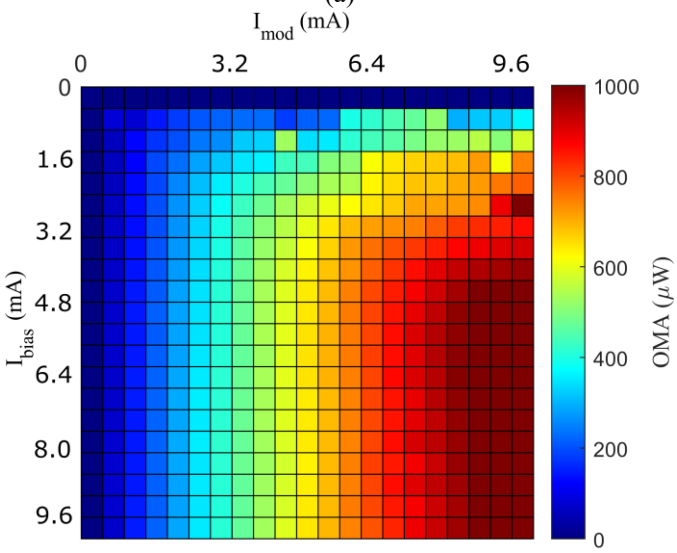
Fig. 8. (a) OMA versus the amplitude of the input electrical signal of an MTx+; (b) BER versus the OMA of MRx+ operating at 10 Gbps and 2.56 Gbps, compared with two commercial modules.

C. I_{mod} and I_{bias} scanning of MTx+

The I_{mod} and I_{bias} of MTx+ were scanned for the optimal operational parameters. The Average Output Power (AOP) and OMA of the test were recorded in the 2-dimension plots shown in Fig. 9(a) and Fig. 9(b), respectively. The AOP is strongly correlated to the I_{bias} but not the I_{mod}. When the I_{bias} is small, the correlation between OMA and Imod is not obvious. When the I_{bias} reaches a certain level, OMA is positively correlated with the I_{mod}. The typical configuration of I_{bias} of 7.7 mA and the I_{mod} of 5.1 mA were selected for the following test of MTx+, according to the results of the I_{bias} and I_{mod} scanning.



(a)



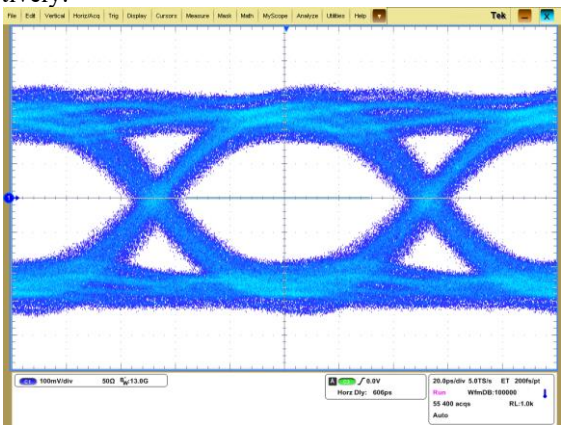
(b)

Fig. 9. (a) AOP versus I_{mod} and I_{bias} joint scanning; (b) OMA versus I_{mod} and I_{bias} joint scanning.

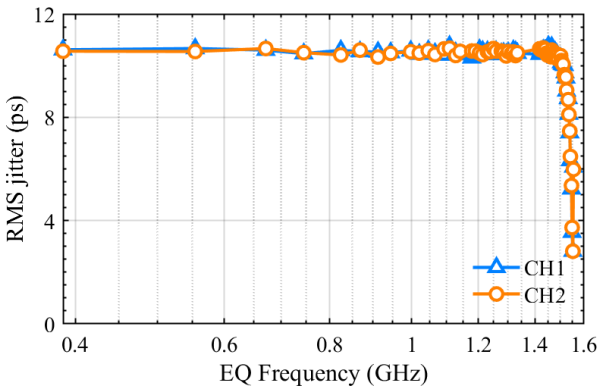
D. Input equalization of MTx+

The effect of the input equalization was tested by scanning the input equalization using two 2 m long coaxial cables (RG316, part number: Amphenol RF 135101-01-M2.00) with Sub-Miniature version A (SMA) connectors. The eye diagram attenuated by the long cables is shown in Fig. 10(a) with the x scale of 20 ps/div and the y scale of 100 mV/div. The results are shown in Fig. 10(b). The RMS jitter can be reduced by adjusting

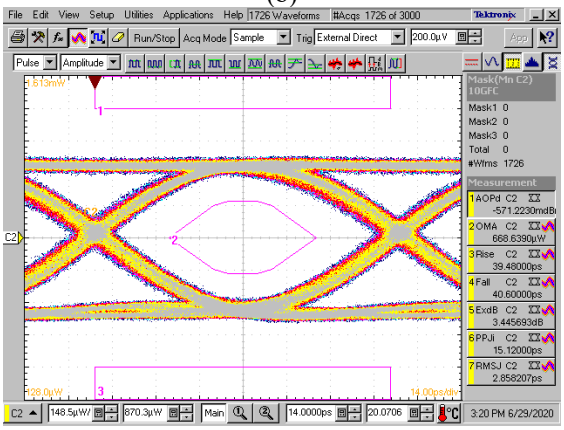
the input equalization. When the frequency of the input equalization is 1.54 GHz, the RMS jitter is 2.8 ps, which alleviates the high-frequency attenuation caused by the long input transmission line. The optimal eye diagram at the input EQ frequency of 1.54 GHz is shown in Fig. 10(c). The AOP and the OMA in Fig. 10(c) are -0.571 dBm and 669 µW, respectively.



(a)



(b)



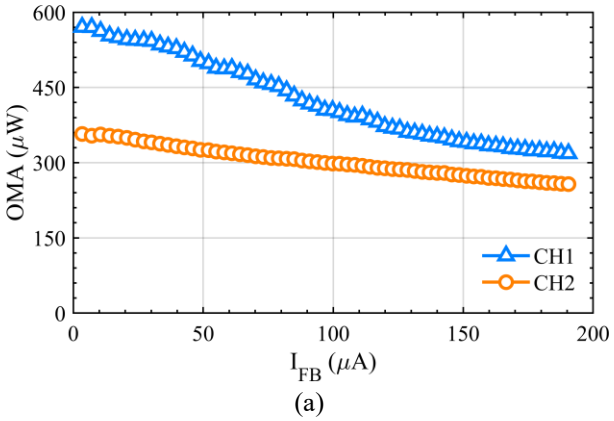
(c)

Fig. 10. (a) Eye diagram from 2 m long coaxial cables; (b) effects of the input equalization; (c) eye diagram when the input EQ frequency is 1.54 GHz.

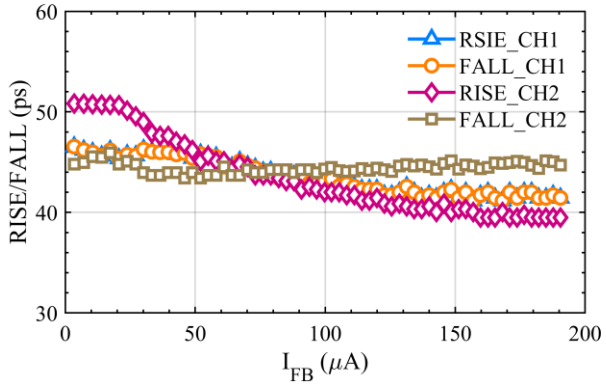
E. Feedback of LA

The goal of the LA feedback is to adjust the balance between the gain and bandwidth of the LA. When I_{FB} is large, the LA has high bandwidth and low gain, and vice versa. When the output of the LA reaches saturation, the feedback effect is not significant. A relatively small input can make sure that the LA works at a linear region and shows the relationship between the feedback and the gain. 10 mV is selected as the input amplitude for testing the feedback of LA.

Fig. 11 shows the effects of I_{FB}. OMA decreases when I_{FB} increases because the gain of LA decreases. In the meantime, the bandwidth of LA increases, reflecting the decrease in rise and fall times. The measurement differences between Channels 1 and 2 could be from the mismatch and the TOSAs.



(a)

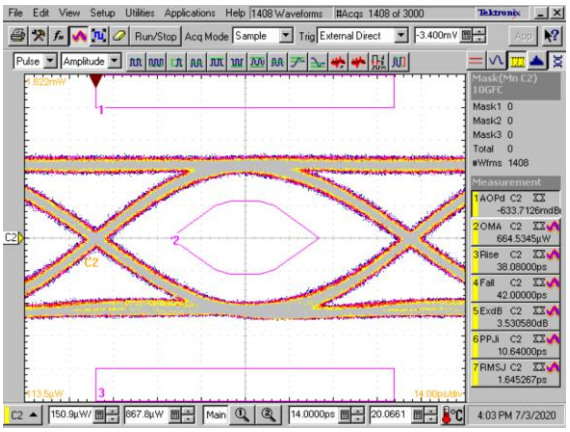


(b)

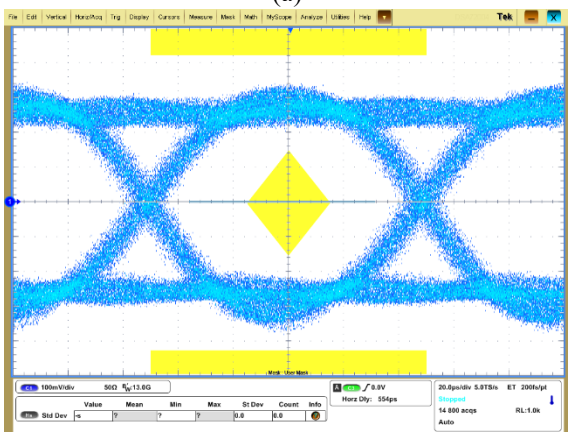
Fig. 11. (a) Dependence of the OMA and (b) the transition times on the I_{FB}.

F. Eye diagrams

The eye diagrams of MTx+ and MRx+ are shown in Fig. *12*(a) and Fig. 12(b), respectively. In Fig. 12(a), the AOP and the OMA are -0.633 dBm and 664.5 µW, respectively. The x scale and the y scale are 20 ps/div and 100 mV/div, respectively. Both eye diagrams passed the 10 Gbps eye mask compliance [17] **Error! Reference source not found.**testing.



(a)



(b)

Fig. 12. (a) Eye diagrams of MTx+ and (b) MRx+.

G. Jitter measurements

Although no decomposition of random jitter and deterministic jitter of MTx+ is performed by the optical scope, the measured peak-to-peak jitter is 10.6 ps and the RMS jitter 1.6 ps. The jitter of MRx+ is analyzed by an electrical oscilloscope with an embedded jitter analysis package TDSJIT3. The total jitter of MRx+ is 29 ps (P-P) with a random jitter of 1.6 ps (RMS) and a deterministic jitter of 9.9 ps (P-P). This should be understood as the parameter taken with MTx+ as the source input.

H. Power consumption

The measured power consumption of each part operating at 10 Gbps is shown in Table 1. Each channel of the MTx+/MRx+ module consumes 82.6 mW and 174.4 mW, respectively. The power consumption of MTRx+ is 257.0 mW.

Table 1. Power consumption of each part

Part	Power consumption (mW)
Single channel of DLAS10	37.5
Single TOSA	45.1
Single ROSA	136.9
MTx+	165.2
MRx+	348.8
MTRx+	257.0

I. Radiation tolerance

The radiation tolerance of DLAS10 and the ROSAs used in the MRx+/MTRx+ modules will be tested in the future. The previous prototype of DLAS10 and the TOSAs that are used in MTx+/MTRx+ have been verified to be radiation tolerant for applications in certain particle physics experiments [10] ,[19] .

J. Comparison

Table 2 gives the performance comparison among MTRx+ and the reported optical modules in this literature.

Table 2. Performance comparison among MTRx+ and the reported modules in this literature

Specification	Module A	Module B	VTRx [20]	MTRx [7]	MTRx+	Unit
Tx data rate	10	25	5	5	10	Gbps
Rx data rate	10	25	5	5	10	Gbps
Tx sensitivity	180	75	100	100	40	mV
Rx sensitivity	-15	-12	-13.1	-13.1	-12	dBm
Size (L×W×H)	48.7 × 14.5 × 9.7	56.55 x 13.4 x 8.5	45 × 14.5 × 10	45 × 15 × 6	43 × 19 × 5.9	mm
Electrical interface	SFP+	SFP28	SFP+	custom	SFP+	-
Optical interface	LC	LC	LC	ferrule	LC	-
Technology	-	-	130	250	65	nm
Power consumption	825	990	500 - 625	320	257	mW

V. Conclusion

We have designed and tested a 10 Gbps driver/receiver ASIC DLAS10 and Optical Transmitter/Receiver/Transceiver modules MTx+, MRx+, and MTRx+ that are based on DLAS10. DLAS10 can drive TOSAs and receive signals from ROSAs with only a TIA. DLAS10 is fabricated in a 65 nm CMOS process. The die of DLAS10 is 1 mm × 1 mm. The electrical input sensitivity of MTx+ is 40 mVpp. The optical input sensitivity of MRx+ is -12 dBm at 10 Gbps and -14 dBm at 2.56 Gbps, respectively. The power consumptions of MTx+ and MRx+ are 82.6 mW/ch and 174.4 mW/ch, respectively. The power consumption of MTRx+ is 257.0 mW.

Acknowledgment

We thank Szymon Kulis and Paulo Moreira at CERN for sharing the I²C block design. We also thank the financial support from the SMU University Research Council Grant, the Dedman College Dean's Research Council Grant, and the Institute of Physics, Academia Sinica.

References

[1] J. Troska et al., The VTRx+, an Optical Link Module for Data Transmission at HL-LHC, PoS (TWEPP-17) 048, doi: 10.22323/1.313.0048.

[2] P. Moreira et al., The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, presented at TWEPP 2019

Topical Workshop on Electronics for Particle Physics, Santiago de Compostela, Spain, September 3, 2019.
[3] J. Troska, Versatile Link Plus Specification, part 2.1, CERN Tech. Rept., EDMS-1719329 (2020).
[4] Takaya, Masaaki, Shinji Nagasawa, and Yasuji Murakami. "Single-mode multifiber connector using an injection molded MT type ferrule and a quick assembly technique." Optical Engineering 39, no. 4 (2000): 1025-1031. doi: 10.1117/1.602457.
[5] ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS LAr Calorimeter, CERN-LHCC-2017-018, CERN, Geneva, 2017.
[6] ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer, CERN-LHCC-2017-017, CERN, Geneva, 2017.
[7] X. Zhao, C. Liu, D. Gong, J. Chen, D. Guo, H. He et al, "Mid-board miniature dual channel optical transmitter MTx and transceiver MTRx." J. Instrum., vol. 11, p. C03054, Mar. 24, 2016, doi: 10.1088/1748-0221/11/03/C03054.
[8] X. Li et al, 8-Gbps-per-channel radiation-tolerant VCSEL drivers for the LHC detector upgrade, 2015 JINST 10 C02017. doi: 10.1088/1748-0221/10/02/C02017.
[9] D. Besin et al., "Design and Evaluation of the LAr Trigger Digitizer Board in the ATLAS Phase-I Upgrade", IEEE Trans. Nucl. Sci. 66 (2019) 2011. doi: 10.1109/TNS.2019.2924795.
[10] W. Zhou et al., "LOCld65, a Dual-Channel VCSEL Driver ASIC for Detector Front-End Readout," in IEEE Transactions on Nuclear Science, vol. 66, no. 7, pp. 1115-1122, July 2019, doi: 10.1109/TNS.2019.2915357.
[11] B. Deng et al., MTRx+ A TOSA/ROSA-based optical transmitter (MTx+)/transceiver (MTRx+) for high-energy physics experiments, 2019 *JINST* 14 C05021, doi: 10.1088/1748-0221/14/05/C05021.
[12] S. Gondi and B. Razavi, "Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers," in IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1999-2011, Sept. 2007, doi: 10.1109/JSSC.2007.903076.
[13] Cai, Chen, Jian-zhong Zhao, and Yu-mei Zhou. "A 1.25–12.5 Gbps adaptive CTLE with asynchronous statistic eye-opening monitor." Journal of Electrical and Computer Engineering 2018 (2018). doi: 10.1155/2018/3095950.
[14] S. Galal and B. Razavi, "10Gb/s limiting amplifier and laser/modulator driver in 0.18/spl mu/m CMOS technology," 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., San Francisco, CA, USA, 2003, pp. 188-487 vol.1, doi: 10.1109/ISSCC.2003.1234261.
[15] T.-C. Huang, et al., "8.4 A 28Gb/s 1pJ/b shared-inductor optical receiver with 56% chip-area reduction in 28nm CMOS," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb. 2014. doi: 10.1109/isscc.2014.6757374.
[16] H.Y. Huang, et al., "A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback." IEEE Journal of Solid-State Circuits. 2007 Apr 23;42(5):1111-20. doi: 10.1109/jssc.2007.894819.
[17] Std, E. E. E. "Std 802.3-2005, "IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications," The Institute of Electrical and Electronics Engineers." Inc., Sections: 1-5. doi: 10.1109/IEEESTD.2005.7297898.
[18] SFF Committee. "SFF-8431 specifications for enhanced small form factor pluggable module SFP+." Revision 4.1 (2009): 132.
[19] F.X. Chang et al., "Aging and environmental tolerance of an optical transmitter for the ATLAS Phase-I upgrade at the LHC," Nucl. Instrum. Meth. A 831 (2016) 349-354. doi: 10.1016/j.nima.2016.04.033.
[20] J. Troska, Versatile Link Specification Part 2.1, EDMS-1140665 (2017).