WEPV033

Architecture of a Multi-Channel Data Streaming Device with an FPGA as a Coprocessor

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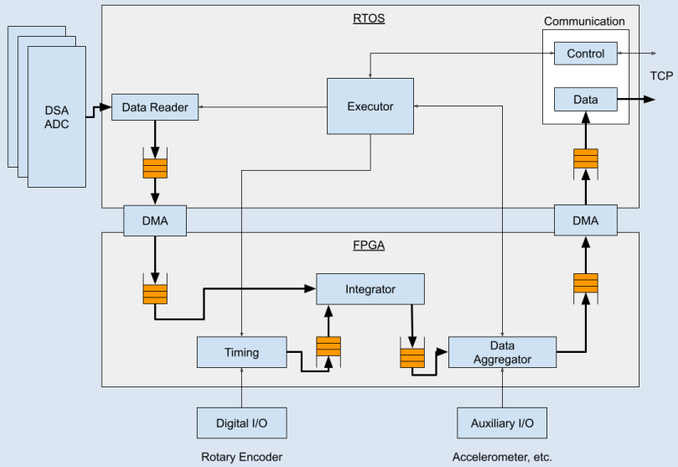
FERMILAB-POSTER-21-119-TD

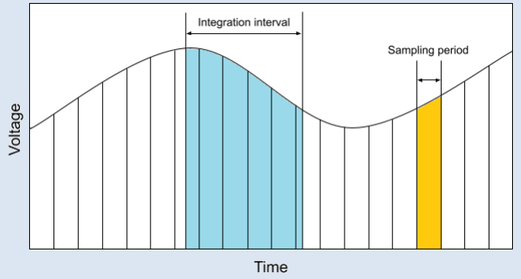
ICALEPCS 2021

Extensible Digital Integrator (EDI)



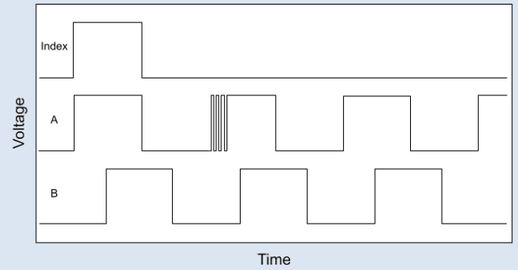
- The EDI is structured as a set of interconnected modules that communicate using data queues.
- After receiving a start command from a TCP connection, the system will begin acquiring data and reading triggers from the angular encoder.
- Integrated ADC samples and timing data are aggregated and are sent back to the real-time OS, where they are transmitted to the consumer.
- No data is stored on disk in the EDI but is instead continuously streamed over the TCP connection for further processing.

Signal Integration



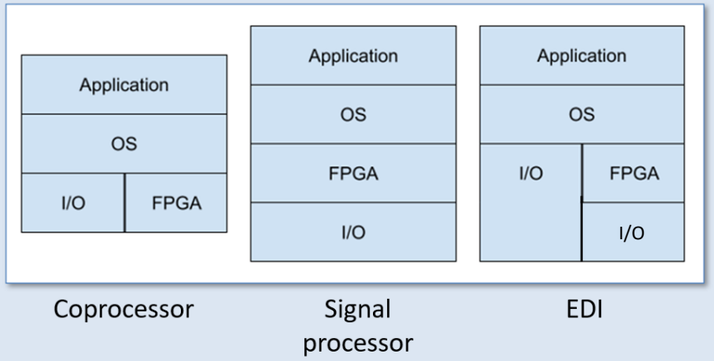
- Triggers do not necessarily arrive at the same time as ADC samples, therefore partial samples must be accounted for.
- Fractions of a sample are tracked in the sample queue.
- This integration operation occurs in parallel on all ADC channels.

Triggering



- An angular encoder is used to generate external triggers.
- With the potential for electrical noise on these trigger lines, the FPGA introduces a debouncing delay to validate triggers before their timing is accepted into the queue.

Architectures with FPGAs



- FPGAs are frequently used as coprocessors whenever parallelized or computationally intensive tasks need to be offloaded from the CPU.
- In many cases when FPGAs are used in DAQ hardware, they are implemented as signal processors that perform operations on raw samples.
- The EDI combines both of these hierarchies into a single architecture, in order to both integrate and aggregate signals.

COTS Hardware

- NI PXIe-4464 ADCs are members of the DSA family of modules with delta-sigma converters. They offer high resolution (24 bits) with high sampling rates (up to 204.8kS/s), 6 gains, and 4 simultaneously sampled input channels.
- NI PXIe-7856 Multifunction Reconfigurable modules feature high-performance FPGAs that add fast signal processing capability to PXI systems. They offer 8 16-bit SAR ADCs, 8 16 bits DACs, 48 digital I/O channels and a Kintex-7 160T FPGA.

Interface - Operations

Operation	Description
set properties	Sets the ADC gains and number of triggers to take data for.
run	Begins the measurement.
abort	Stops data acquisition, regardless of status.
read temperature	Reads ADC temperatures for offline correction.
read accelerometer	Reads probe orientation.

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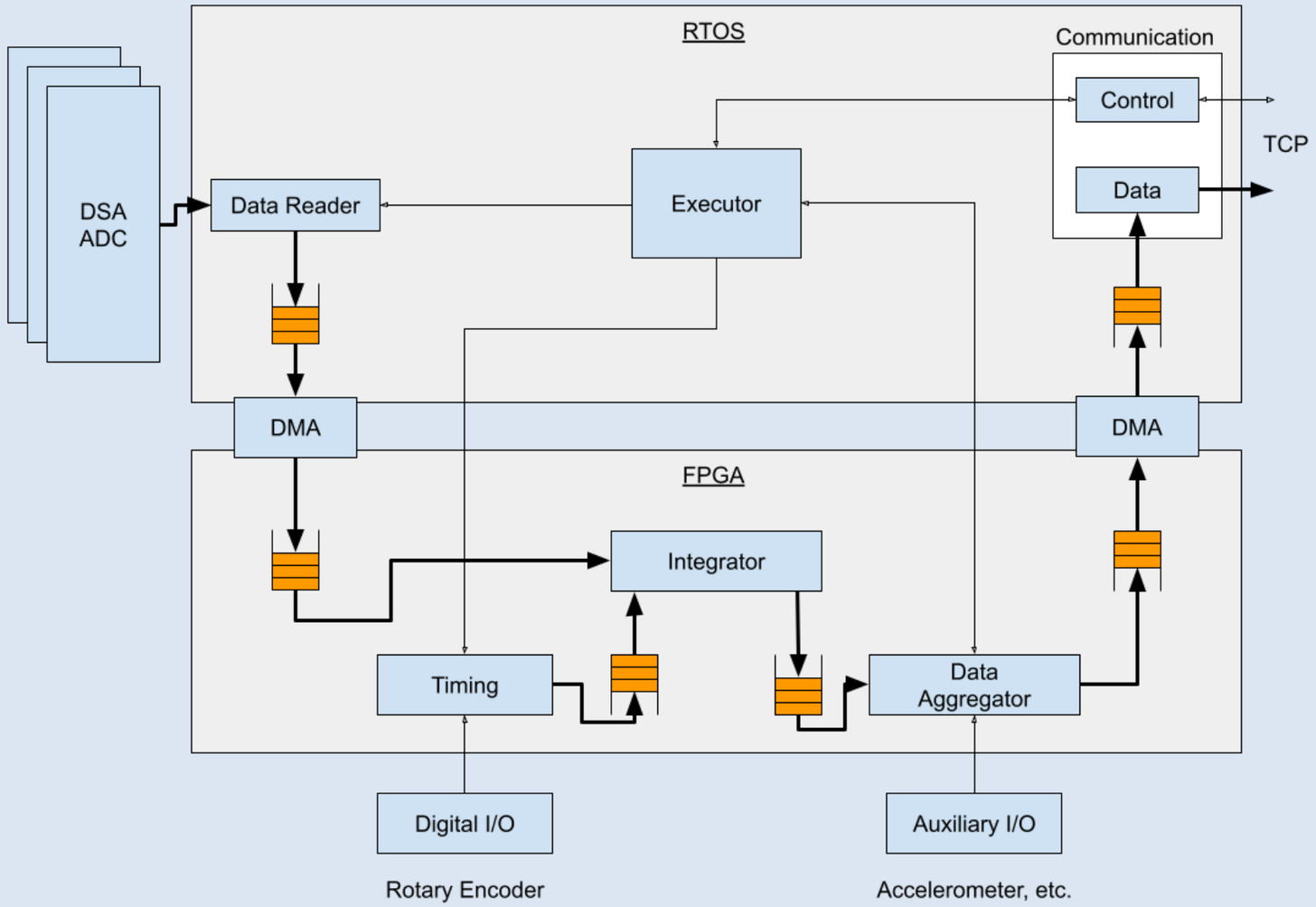

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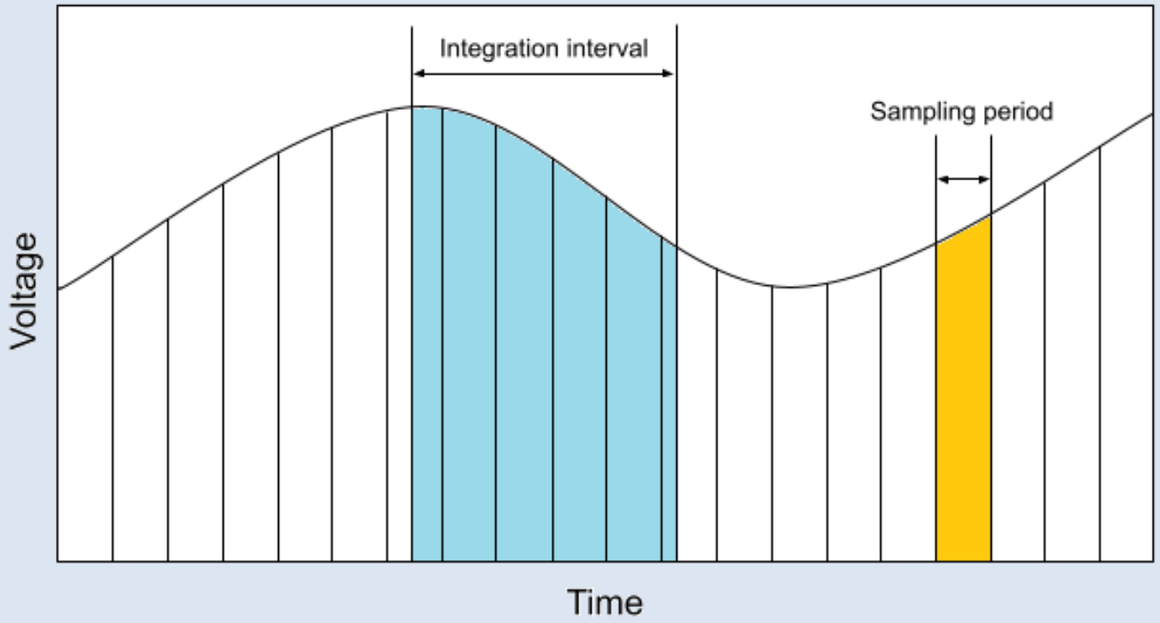

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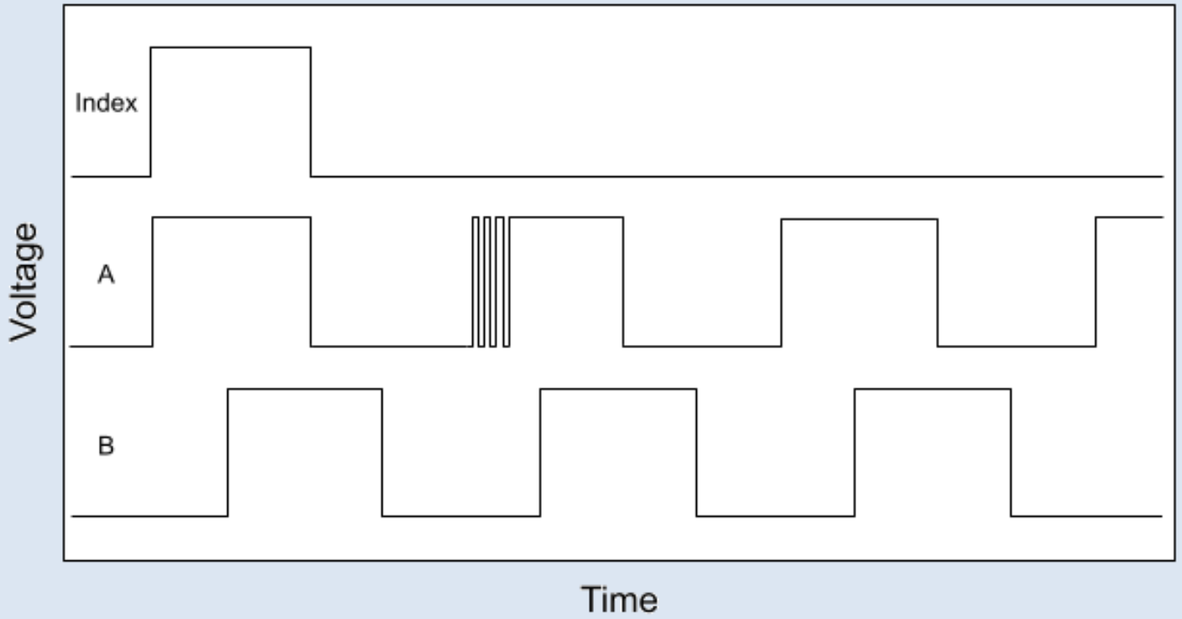

- Typically, an angular encoder is used to generate external triggers.
- With the potential for electrical and/or mechanical noise on these trigger lines, the FPGA introduces a debouncing delay to validate triggers before their timing is accepted into the queue.

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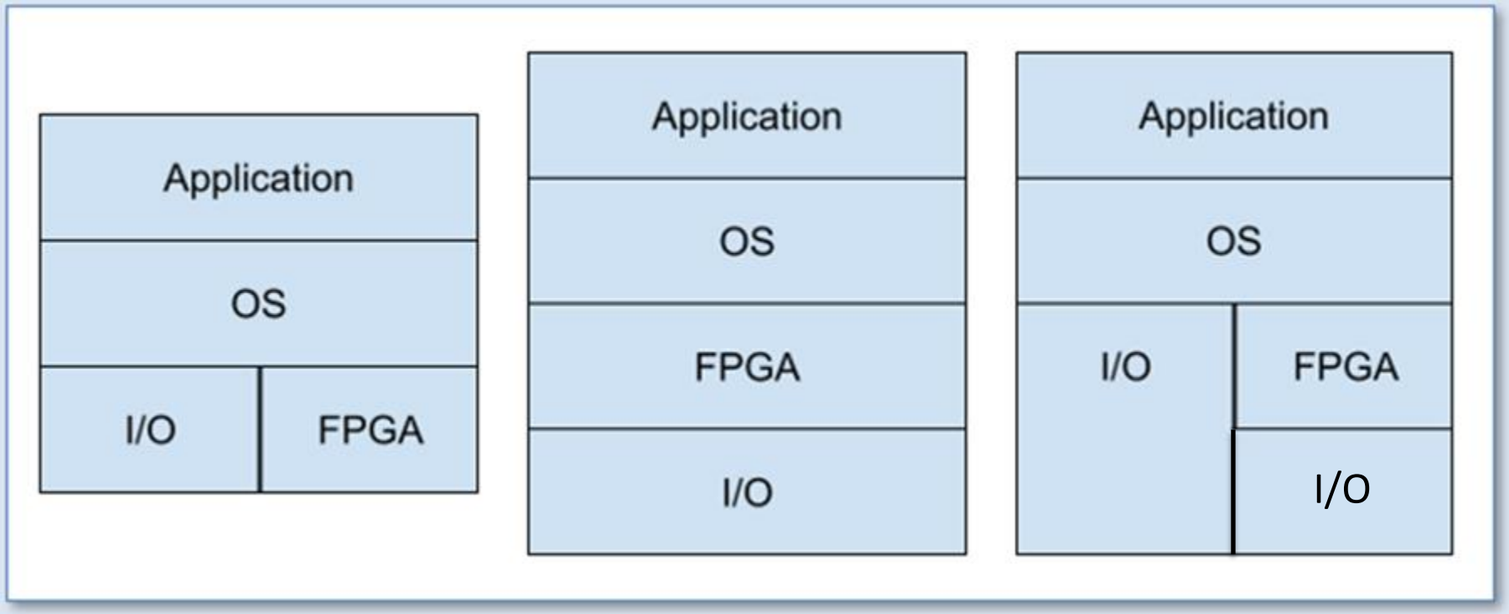
Architectures with FPGAs



Coprocessor | Signal processor | EDI

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