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# Developing conduction-cooled SRF cavities and first test results

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(with contributions from Fermilab AD/ME and APS-TD/SRF teams)

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# Motivation: develop SRF accelerators for industrial applications

## Electron beam radiation processing



- Requirements: high power electron beams 0.5-10 MeV, with very high beam power > 100 kW
- Applications:
  - Water/sludge decontamination
  - Flue gas cleanup
  - Environmental remediation
  - Medical waste sterilization

[http://accelconf.web.cern.ch/AccelConf/napac2016/talks/thb3io02\\_talk.pdf](http://accelconf.web.cern.ch/AccelConf/napac2016/talks/thb3io02_talk.pdf)

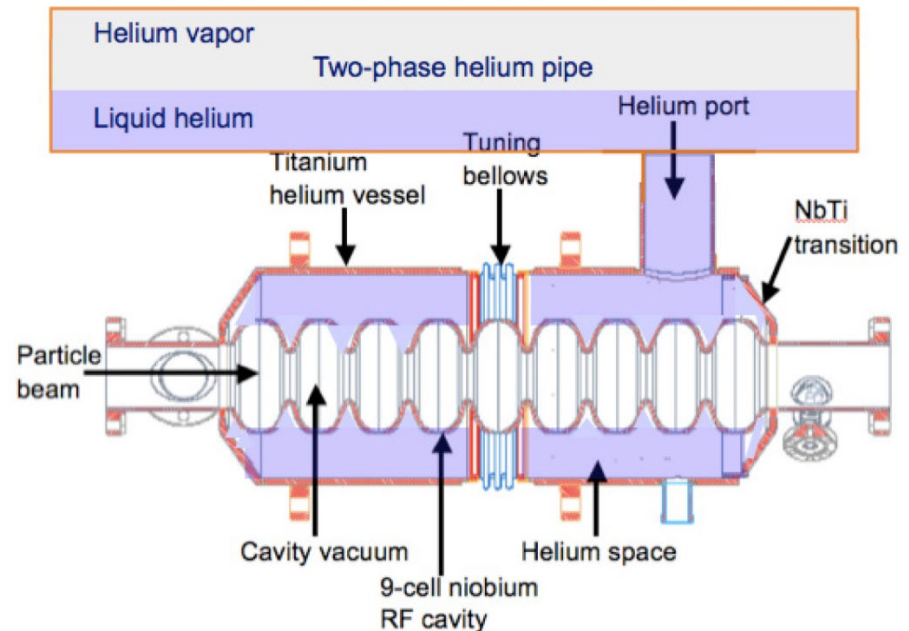
## A meter long SRF linac

- $E_{acc}$  10 MV/m
- cw for high beam power

Industrial settings require:

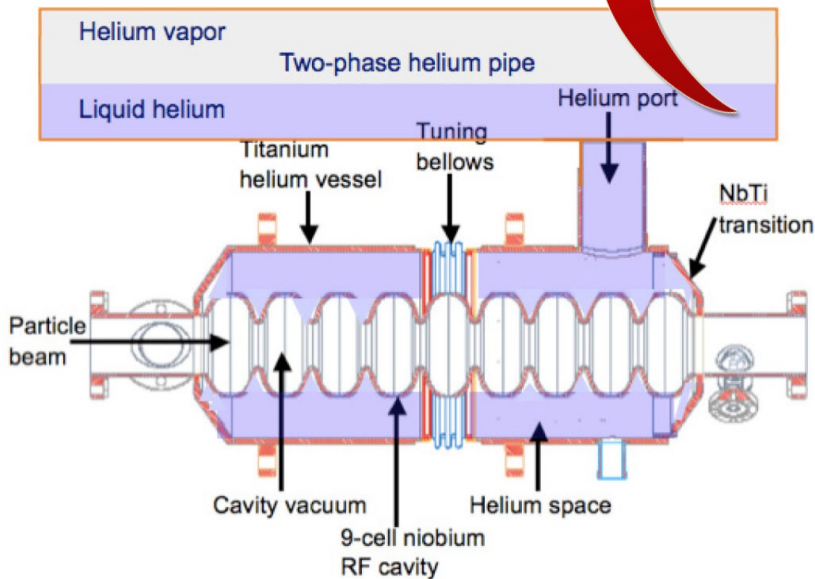
- Low capital and operating cost
- Robust, reliable, turn-key operation

SRF accelerators rely on LHe, which makes them complex machines

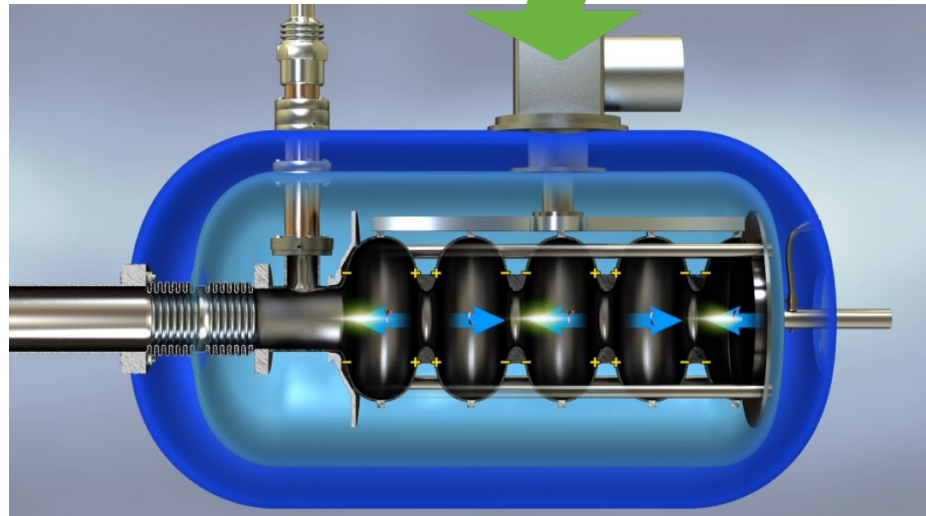


# Need: simplify SRF accelerator cryogenics

Take out liquid helium  
(and its complexities)



Cool SRF cavities conductively with  
4 K cryocoolers



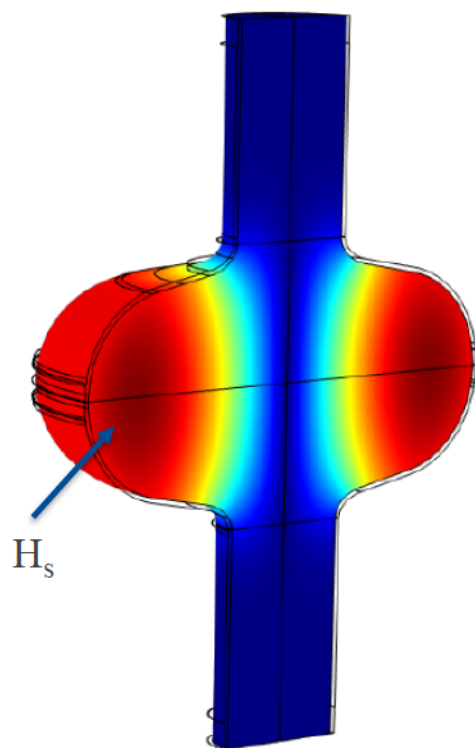
## Goals:

- Practical design of a thermal conduction link
- Demonstration of 10 MV/m cw gradient

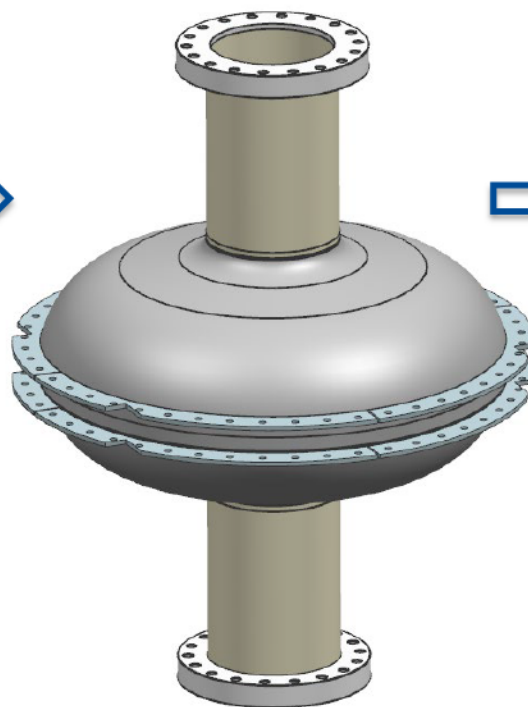
# Conduction cooling for SRF cavities: Design approach

Dissipation is prominent near the equator

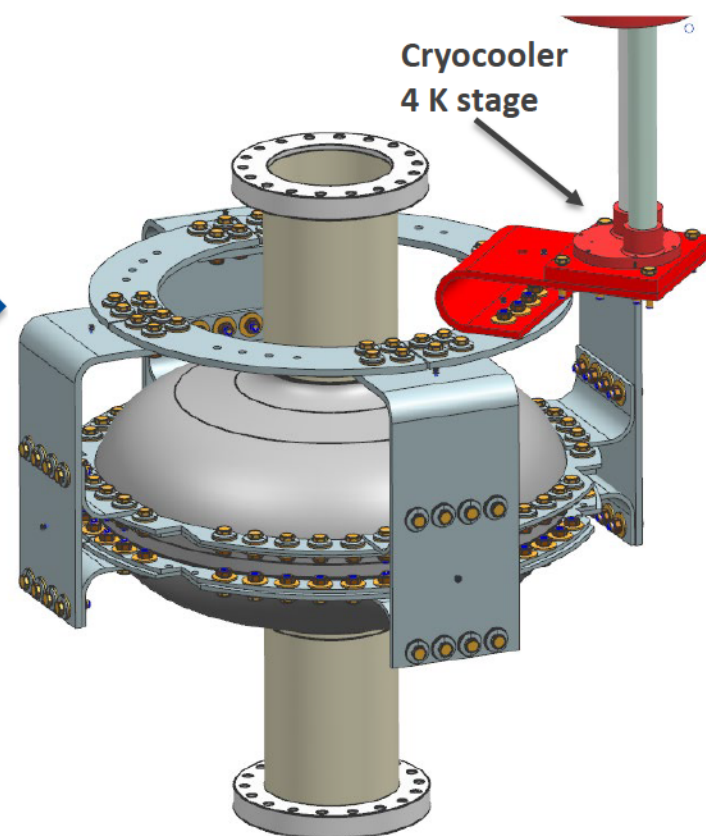
$$P_{diss} = \frac{1}{2} R_s \oint |H_s|^2 ds$$



Weld niobium rings around the equator to extract dissipation



Connect cavity to cryocooler with a thermal conduction link

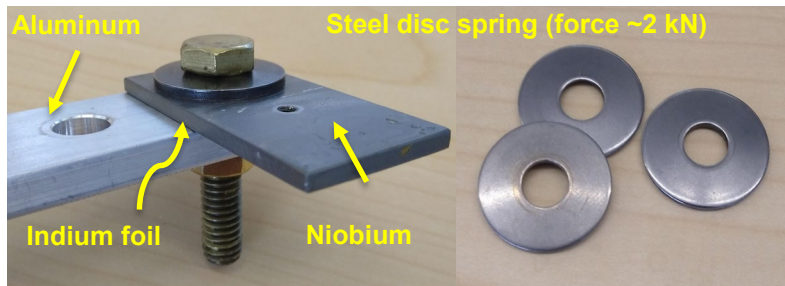


# Design of thermal link

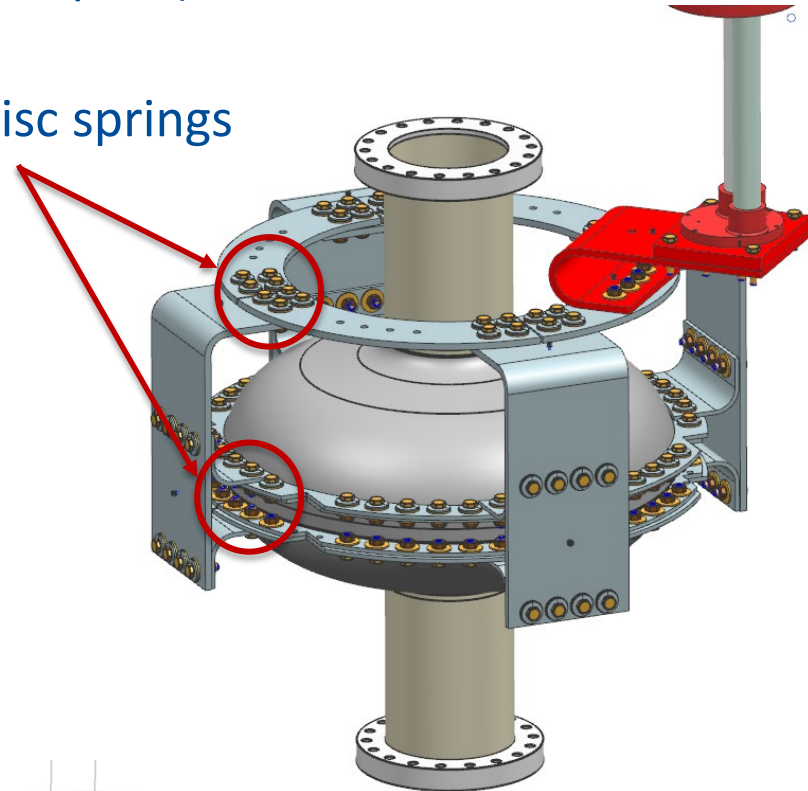
**Material:** High purity aluminum (5N or 99.999% pure)

**Connection method:** bolting, pressed using disc springs

Thermal design of pressed contacts established via contact resistance measurements on small samples

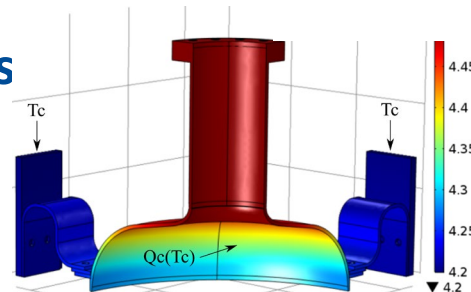


R.C. Dhuley, M.I. Geelhoed, J.C.T. Thangaraj, *Cryogenics* 93, 86-93, 2018



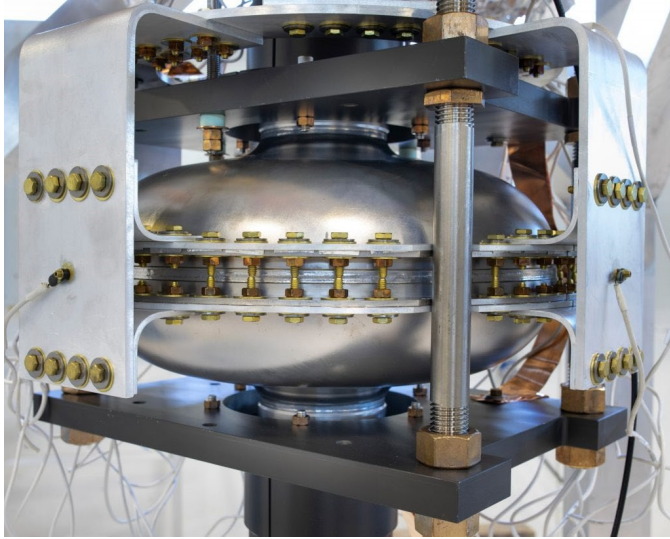
## Physical design via thermal simulations

R. Dhuley, R. Kostin, S. Posen *et al.*, *IEEE TAS* 29(5), 0500205, 2019





# New test cryostat

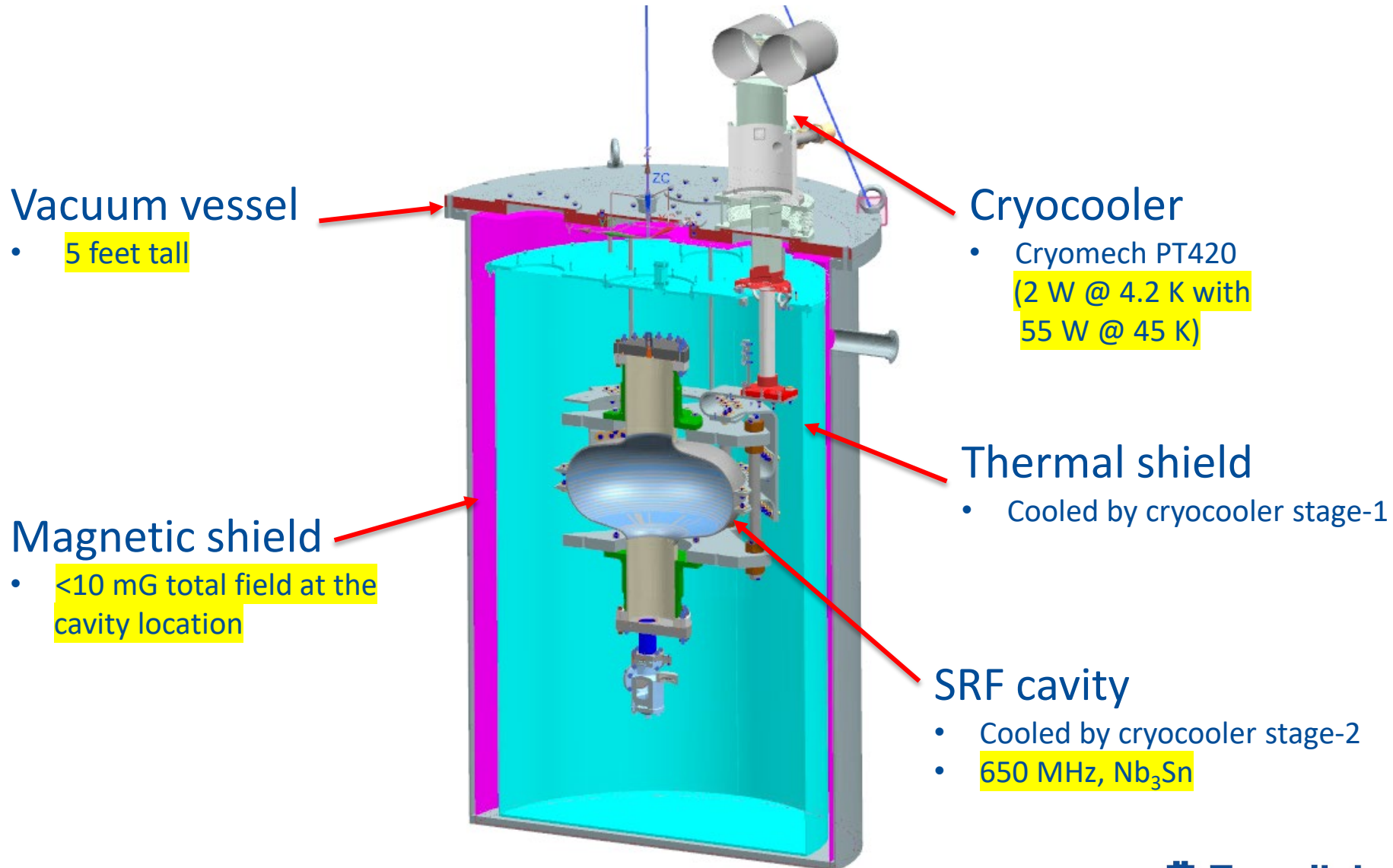


Cavity bolted with thermal conduction links



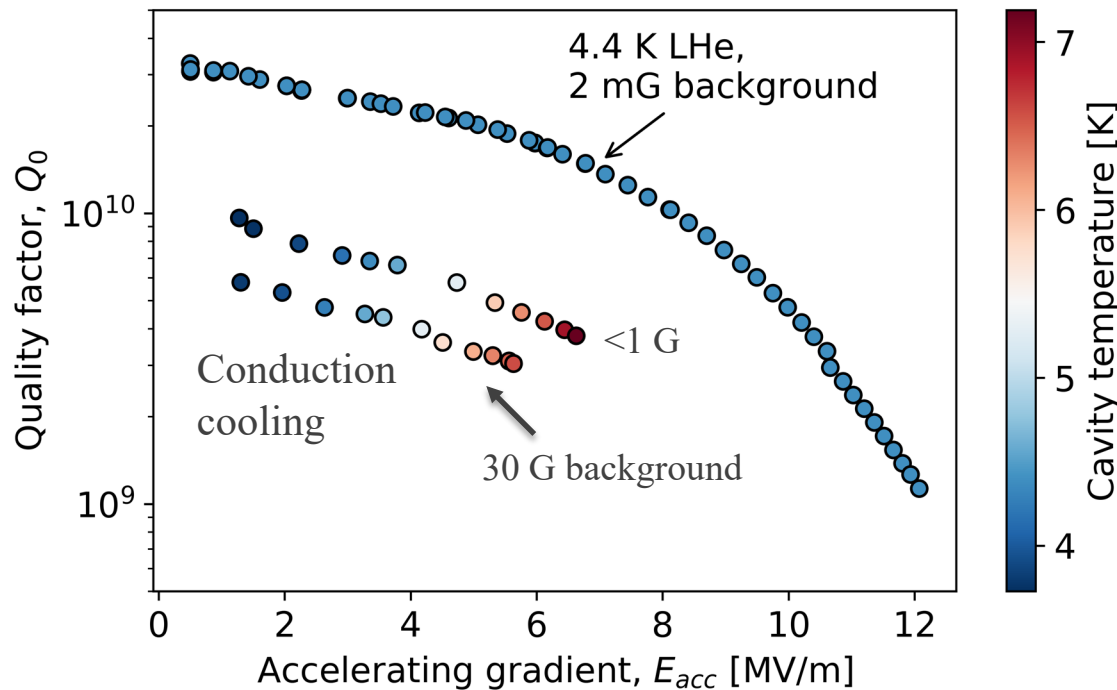
Test setup

# New test cryostat



# First results

## $Q_0$ vs. $E_{acc}$ for 650 MHz Nb<sub>3</sub>Sn cavity

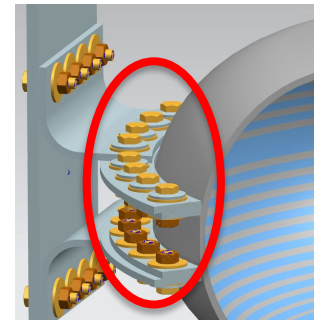


## VTS baseline

- $Q_0$   $3 \times 10^{10}$  at  $E_{acc}$  1 MV/m
- $E_{acc}$  12 MV/m (power limit)

## Conduction cooling

- $Q_0$   $5 \times 10^9$  at  $E_{acc}$  1 MV/m
- $E_{acc}$  5.5 MV/m (power limit)



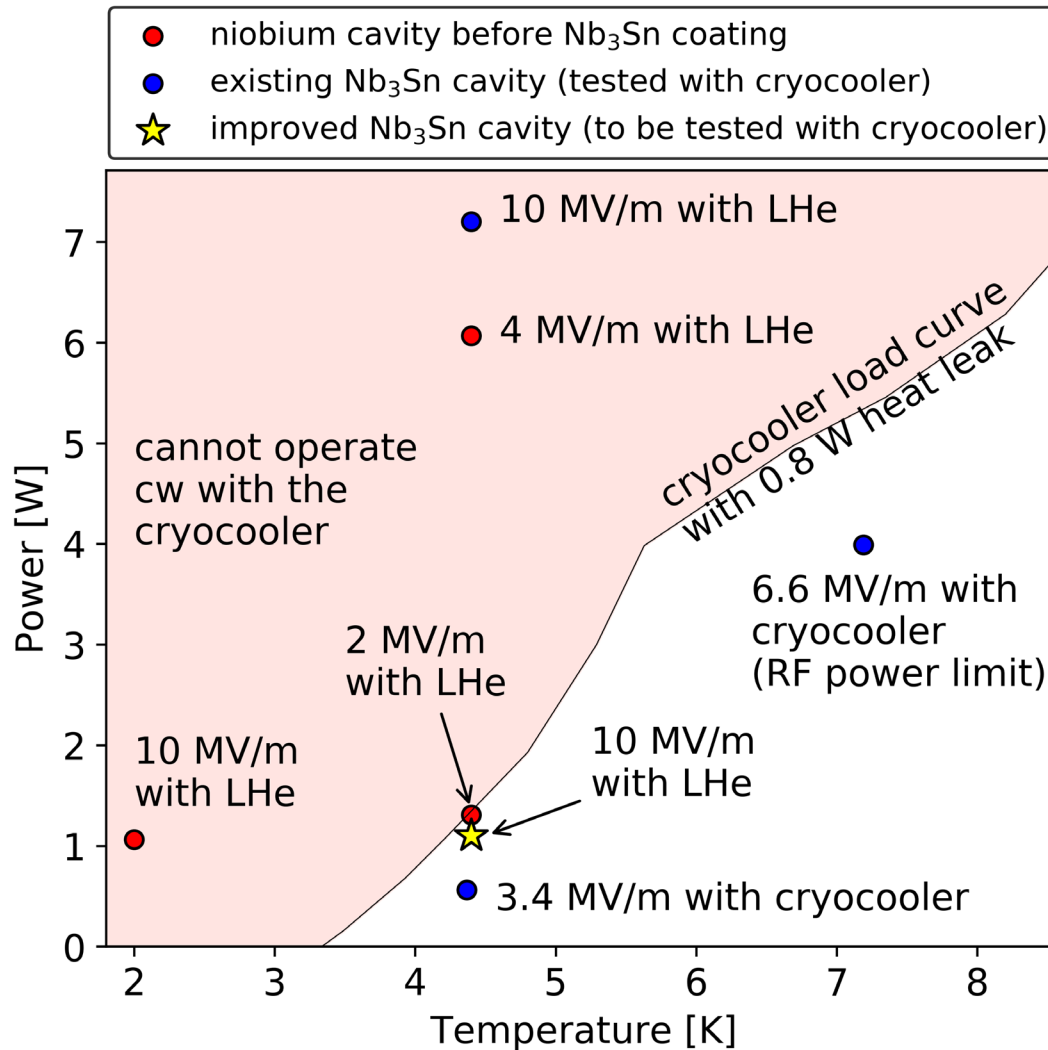
disc springs  
~30 G

## with <1 G disc springs

- $Q_0$   $1 \times 10^{10}$  at  $E_{acc}$  1 MV/m
- $E_{acc}$  6.6 MV/m (power limit)



# Progress, lessons so far...



## ● Niobium cavity

- limited in performance with 4 K cryocoolers

## ● Nb<sub>3</sub>Sn cavity

- Performance not limited by cryocooler capacity at 4.2 K.  $E_{acc}$  can be pushed up by letting the cryocooler operate warmer than 4.2 K.
- Better coating and magnetic hygiene is needed to reach 10 MV/m cw.

## ★ Improved Nb<sub>3</sub>Sn coating

- New coating has produced 10 MV/m in VTS with dissipation manageable with the cryocooler at 4.4 K.

# Summary and future work

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## Development of conduction cooling for SRF

- Practical thermal link design
- Experimental setup ready
- First results are promising
  - 6.6 MV/m cw recorded on a single cell 650 MHz Nb<sub>3</sub>Sn cavity

## Activities: ongoing and planned

- Improve magnetic hygiene of our cryostat
- Test with improved Nb<sub>3</sub>Sn coating
- Identify and mitigate potential microphonics due to cryocooler vibrations

# Acknowledgement

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Conduction cooled SRF demonstration

- Fermilab LDRD
- Accelerator Stewardship award from US DOE/SC/HEP

Infrastructure for Nb<sub>3</sub>Sn coating at Fermilab

- Fermilab LDRD
- DOE Early Career Award (S. Posen)

# Thank you

The diagram illustrates the RF driver with feedback for PLL system. It includes the following components and connections:

- Control computer**: Connected to the **PXIe Crate**.
- PXIe Crate**: Houses the **NI PXI A/D** and **NI PXIe FPGA**.
- OCXO PLL Freq. Source**: Provides a **10MHz Ref** to the **NI PXIe FPGA** and a **630MHz Carrier** to the **I/Q demod** block.
- 20MHz DDS IF**: Connected to the **NI PXIe FPGA**, which outputs **I** and **Q** signals to the **I/Q mod** block.
- I/Q mod**: A multiplier block that combines the **I** and **Q** signals with the **630MHz Carrier** to generate the **650MHz 10W Class A** signal.
- 650MHz 10W Class A**: A power amplifier that drives the **650MHz SRF cavity**.
- 650MHz SRF cavity**: The resonant circuit being driven.
- Feedback Monitors**:
  - FWD RF Monitor**: A detector that monitors the forward signal from the amplifier.
  - RFL RF Monitor**: A detector that monitors the reflected signal from the cavity.
  - Cavity Field monitor**: A monitor that provides feedback from the cavity to the **I/Q demod** block.
- I/Q demod**: A multiplier block that demodulates the signal from the **Cavity Field monitor** and provides feedback to the **NI PXIe FPGA**.
- NI PXI A/D**: Receives signals from the **FWD RF Monitor** and **RFL RF Monitor** and sends data to the **Control computer**.

The system is labeled **Euclid** in green text.