Digital Application Specific Integrated Circuit Design

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Triple Modular Redundancy Tool for System Verilog

Background: TMR

Single radiation effects can be transient and static. The charge collected from radiation has a prompt (drift) and a slow (diffusion) component. This current spike causes disparate results: SEU, SET, SEB, MBU, and more. A system level SEE mitigation technique, used to overcome, is the triple module redundancy (TMR).

TMR for system Verilog (TMR4SV), written in Python, is the first step towards design IP triplication. It allows various triplication methods for flip flops, clocks, and logic.

Technology

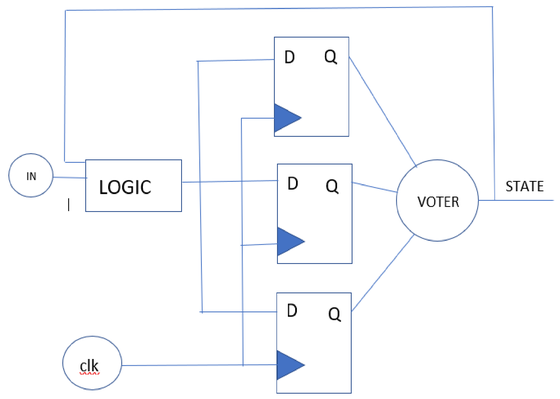
PyCharm, Linux, HSpice

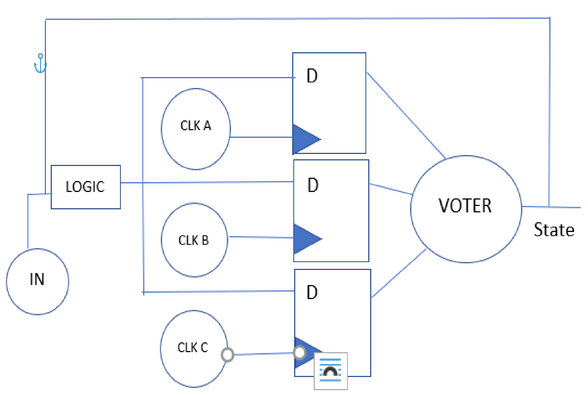
Objectives and characteristics

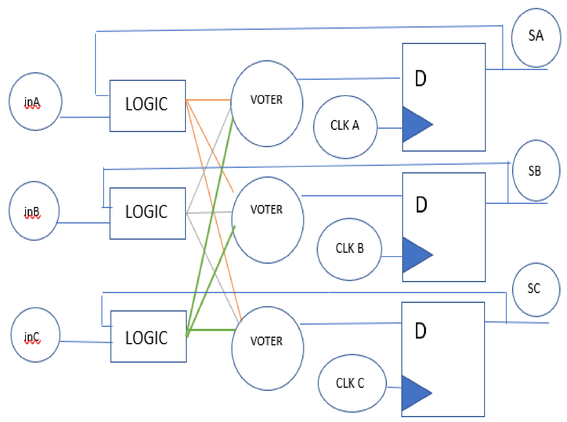
1. User interface to choose methodology.
2. Constraint file is modified if clocks or logic are triplicated.
3. Clock and reset pins are re-named to user's preference.
4. All components are triplicated as chosen by the user. The designated folder should have a new file named module_TMR.sv.
5. Input file's name is modified to have modules name: module.sv.

Overall, the use of the triplication alleviates the radiation's effect and prevents upsets within a state's transition.

Visuals of various Triplication Methods



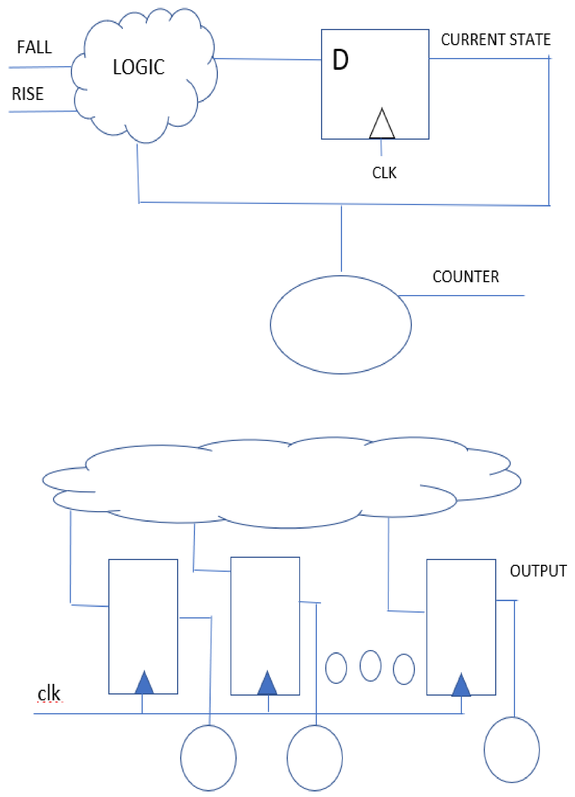




Acknowledgments: Thank you to Farah Fahim, Troy England, Leandro Stefanazzi, Manuel Blanco Valentin, SIST Committee, and LSMRCE Committee.

VHDL for Pile Up Control

Flowchart for Pile Up Control



Technology

ModelSim, Linux

Background for Pile Up Control

The asic analog memory can hold up to 16 values of signals per channel, and the pile up control logic allows to serialize read and write from it.

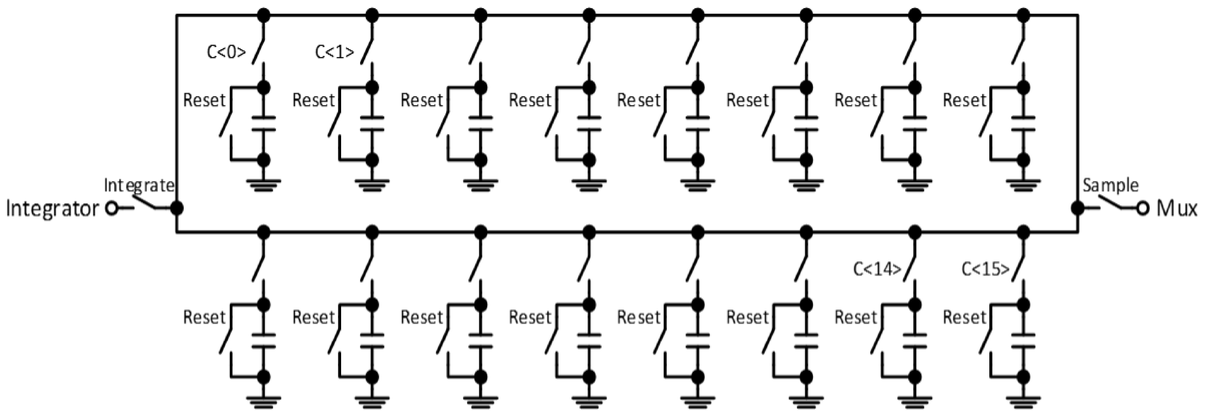
The pile up control written in VHSIC Hardware Description Language (VHDL) Code enables the use of 16 capacitors. This is done by reading 3 input signals: integrate, readint, rst.

The input integrate generates two pulses. For every two pulses, a capacitor (C) goes high for C<i+1>.

- Logic: Identify integrate's rise and fall.
- FSM: Determines state based on logic.
- The FSM's output, current state, is then included into the logic.
- Counter: Counts up until the signal readint goes high.
- Flip Flops: They represent the capacitors C<i>.

The VHDL Code includes an Entity, Architecture, 3 Processes, and a Case Statement.

Schematic for Pile Up Control



Triple Module Redundancy and Pile Up Control

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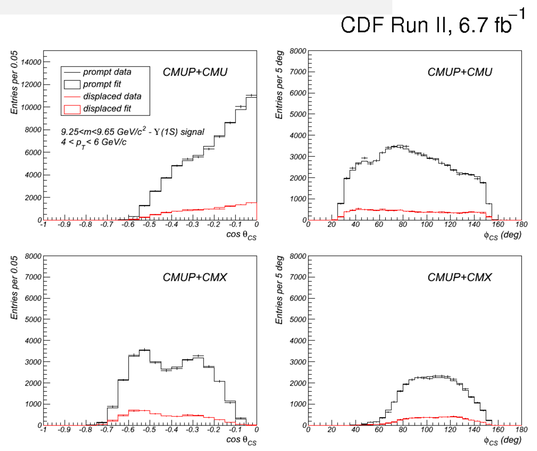

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