A New Scheme of Redundant Timing Crosschecking for Frontend Systems

Jingjing Xu, Jinyuan Wu, Ted Liu, Jamieson T Olsen and Quan Sun

***Abstract*— In high energy physics experiments, frontend digitization modules are usually driven by a common clock. At the frontend electronics and digitization modules of the detector, a precise timing reference must establish in order to make a useful timing measurement. It would be very useful for the frontend digitization system to include a feature of redundant timing crosschecking. The inspiration for the timing crosschecking scheme came from the long-abandoned analog mean-timer schemes. In this scheme, several Front-end modules are connected together through a cable set with taps connected to the digitization modules. Pulses are driven from every FE modules alternately without overlapping. The arrival times of pulses sent from FE modules are digitized at the timing crosschecking module. The mean times will change as temperature changes, but their difference between two FE modules are cancelled mathematically. This feature enables easy achievement of good timing precision without the need for complex hardware.**

***Index Terms*— Time to Digital Convertor, Timing Reference Distribution, Mean Time**

I. Introduction

In high energy physics experiments, frontend digitization modules are usually driven by a common clock. At the frontend electronics and digitization modules of the detector, a precise timing reference must establish in order to make a useful timing measurement.

Typically, frontend and digitization modules inside the detector are connected to outside through optical fibers, with local clock signals derived from the serial link. The paths for clock distribution could be about 100 meters in large detectors so temperature effect must be taken into account.

While there exist various solutions for temperature variation compensation in the vertical clock distribution paths, it would be very useful to build a horizontal connection to provide a redundant timing crosschecking as shown in Fig. 1.

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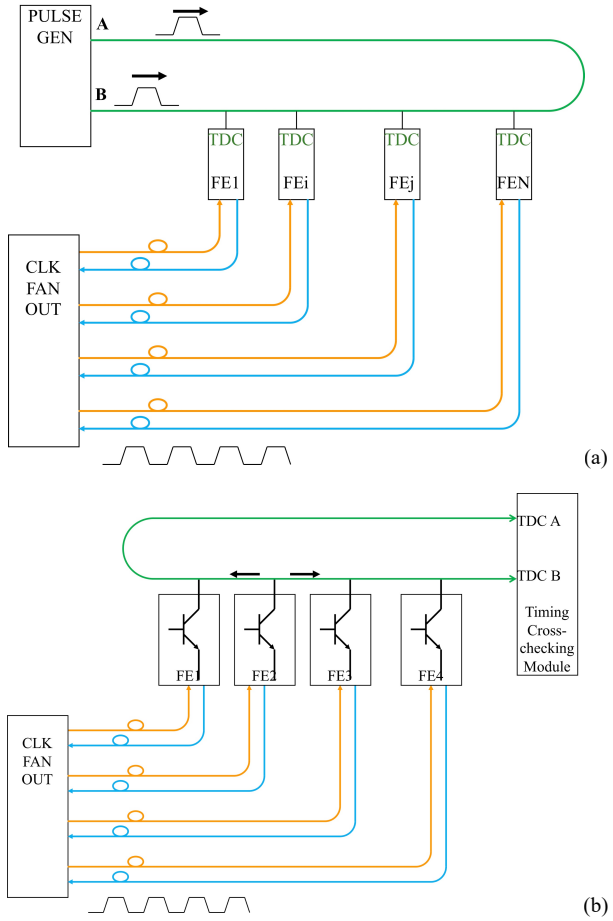

Fig. 1. Possible timing crosschecking schemes

The inspiration for the timing crosschecking scheme came from the long-abandoned analog mean-timer schemes [1-4]. Some brief study of the authors can be found in References [5] and [6]. Consider a detector subsystem containing N frontend electronics, marked as FE1, FE2, etc. and frontend modules are interconnected through a cable. In the scheme shown in Fig. 1(a), pulses are sent to the cable from left and right alternately without overlapping. The time-to-digital converter (TDC) at each module digitizes arrival times of both pulses. The mean of the both arrival times is used as a timing reference and the performance of this scheme has been reported in our previous work [7].

If a TDC channel is not conveniently available in a frontend module, a new scheme shown in Fig. 1(b) becomes more suitable, which is the main topic of this paper. In this case, each

frontend module sends pulses alternately to both ends without overlapping. The only extra hardware implemented in the frontend module is an open collector or other tri-state driver that can drive a pulse to both directions of the cable and can maintain the cable tap high impedance while not driving. Each module drives the cable with a predefined sequence while the pulse edges are aligned to its local clock. For example, in a system with 40 MHz global clock, one may choose to drive the cable in a 200 ns pace. In this case, module 0 drives the cable at clock cycle 0 and 8 clock cycles later, the module 1 drives the cable at clock cycle 8, etc.

The arrival times of the pulses from each frontend module are digitized by the TDC channels A and B at the Timing Cross-checking Module. The arrival times of a pulse measured by two TDC channels are average as the mean time of the pulse. The mean times from different modules reflect driving times on these modules which are aligned to their local clocks.

Clearly there are propagation delays between modules when the pulses travel in the cable and the propagation delays may change as temperature changes. However, as we will show later, the differences of the mean times between any two module remains a constant regardless the variations of the cable delays. The timing relationship between local clocks can be monitored with this scheme, taking advantage of the mathematical cancelation of the cable delays.

In this paper, we will discuss the principal of this scheme in Section II. Preliminary test results will be described in the remaining sections.

II. Property of the Mean Times

Consider one pulses from a frontend module traveling in opposite directions to TDC A and TDC B. The arrival times of two pulses from any two modules FE_i and FE_j are measured by the TDC channels as shown in Fig. 2.

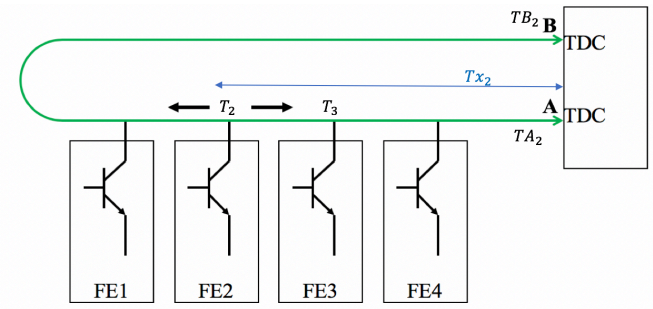

Fig. 2. The arrival times of the pulses

For simplicity, let's define the arrival times for only one edge, for example, the leading edges of the pulses, although the following calculations apply to both edges. The time of the pulse edge sent from module FE_i is T_i. If the arrival time of pulse at TDC A from module FE_i is TA_i and the arrival time of pulse at TDC B from module FE_i is TB_i. We define the propagation delay from module FE_i to TDC A as $T(x_{i,A})$ and similarly from module FE_j to TDC B as $T(x_{j,B})$. We further define the propagation delay from module FE_i to FE_j as $T(x_{i,j})$. The arrival times for pulse at TDC A can be written:

$$TA_i = T_i + T(x_{i,A}) \qquad (1)$$

The arrival times for pulse at TDC B have similar relation.

$$TB_i = T_i + T(x_{i,j}) + T(x_{j,B}) \qquad (2)$$

Now we calculate the time difference $\delta T_{i,j}$ between pulses sent from two FE modules. Here, we assumed that the propagation delays for pulses traveling in opposite directions are the same, or $T(x_{i,j}) = T(x_{j,i})$, which is true for most cables with acceptable quality.

The mean times of the arrival times of the pulses at two digitize modules can be simply calculated.

$$\frac{TA_i+TB_i}{2} = \frac{2T_i+T(x_{i,A})+T(x_{i,j})+T(x_{j,B})}{2} \qquad (3)$$

$$\frac{TA_j+TB_j}{2} = \frac{2T_j+T(x_{j,B})+T(x_{j,i})+T(x_{i,A})}{2} \qquad (4)$$

$$\delta T_{i,j} = \frac{TA_j+TB_j}{2} - \frac{TA_i+TB_i}{2} = T_j - T_i + \frac{T(x_{j,i})-T(x_{i,j})}{2} \qquad (5)$$

It can be seen that the difference of these two mean time values equals to the time difference between pulses sent from these two frontend modules as long as the propagation delays for the pulses traveling in both directions are the same. This difference should have the same interval as the pulse sent from frontend modules. If the temperature variation causes the propagation delay to change, the mean times measured and calculated at both modules will change, but by the same amount.

This property of the mean times can be applied for all frontend modules connected to the same cable. As pointed out early, the arrival times are not limited to the leading edges of the pulses. Also, there is no restriction on how many pulses can be sent out from each frontend module. For example, the FEi module can send out a burst of pulses and then FEj can send out a burst with same number of transitions. This produces more time measurements in unit time period that helps to improve measurement precision.

III. The Evaluation Test Results

In practical implementation as shown in Fig. 3, 8 printed circuit boards emulating the frontend modules are interconnected together using short cable segments. A very short trace on the board is used to connect two SMA connectors to maintain the signal path and the collector of a BJT transistor is attached to the trace as the signal driver with open collector non-saturate current source topology.

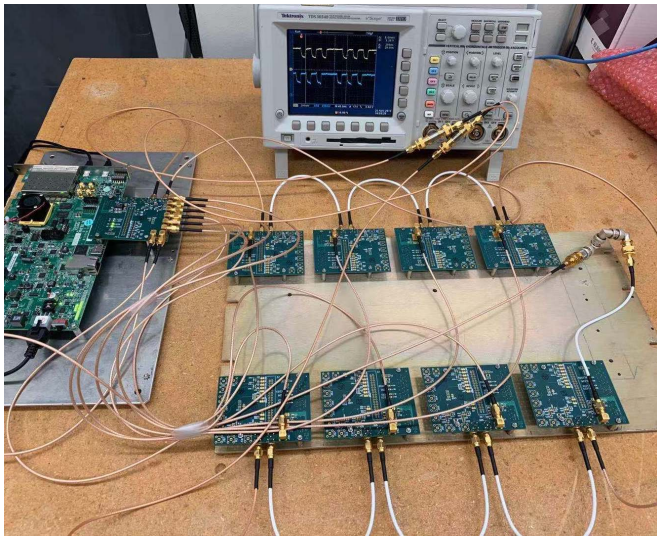

Fig. 3. The practical implementation of frontend modules Systems

An evaluation board with Xilinx Ultrascale+ FPGA (Field-Programmable Gate Array, xcku5p-ffvb676-2-e) is used both to drive the FE modules and to digitize the pulse arrival times at the cable ends with two channels of TDC implemented in the FPGA with a nominal measurement precision of 30 ps (resource utilization: LUT:1470; FF:3208;). The clock frequency of the FPGA TDC is 553.3784 MHz (generated from 300 MHz using cascaded phase lock-loops with integer factors 13*63/(3*2*37*2)), which is chosen to avoid artificial alignment between the test period of 200 ns.

Three pulses, which we call a common burst, are generated in the FPGA every 200 ns and are sent to frontend modules alternately. Each frontend module receives the pulses in a 200 ns interval, driving the shared cable. The pulses are detected by the two TDC channels connected to the end of the cable. The waveforms seen at both ends of the cable are shown in Fig. 4.

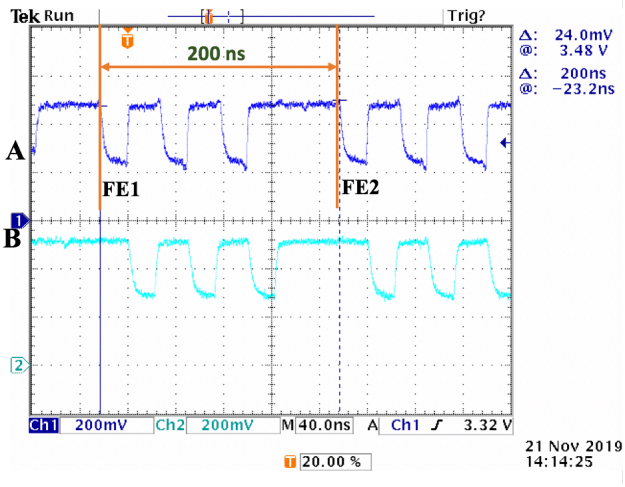

Fig. 4. The waveforms seen at both ends of the cable.

The oscilloscope screen shot can be used as a simple demonstration of the mean timing cross-checking scheme.

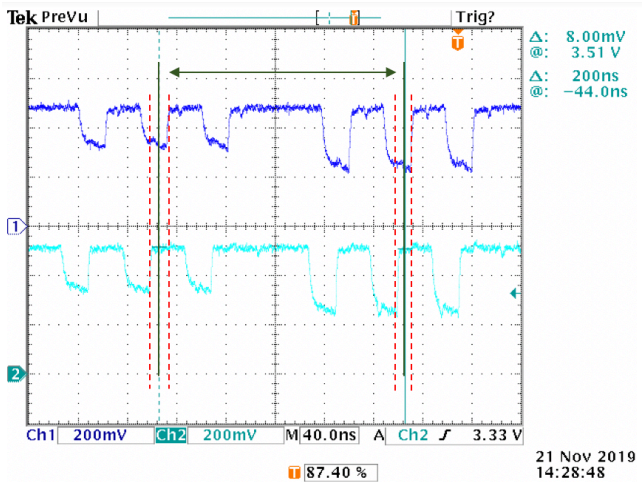

Fig. 5. Mean time difference of pulse at TDC A and B for two frontend modules

As shown in Fig. 5, the arrival times at TDC A (CH1) and TDC B (CH2) for an edge of the pulses driven by two neighboring modules are marked by the four vertical red dashed lines. The centers, or the mean times of the edges are marked with the dark green solid lines (and also the vertical cursors of the oscilloscope). It can be seen that despite cable delays between two modules, the difference between the two mean times from two frontend modules equals to 200 ns, which is the same time interval as the pulses was sent.

In practical analysis, a total of 12 arrival time measurements, meaning both edges of 3 pulses at TDC A and B, are used to calculate the mean time of a common burst to improve measurement precision. Several hundreds of measurements of the bursts are repeated to study of the timing cross-checking scheme. A typical performance is shown in Fig. 5.

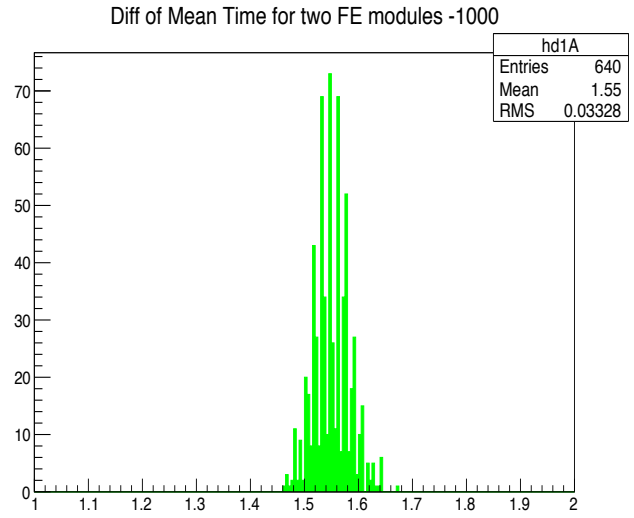

Fig. 6. The difference of mean times for two frontend modules

In the histogram shown above, the differences of mean times of the bursts created by two FE modules are plotted. The two FE modules are 5 cable segments apart and in our sequence their bursts are nominally 1000 ns apart. It can be seen from the histogram that the difference between two frontend modules

are approximately the same, even though the arrival times of the pulse edges at TDC A and TDC B are significantly different due to cable propagation delays.

The differences of the mean times between any two frontend modules are constants and the variations reflect the clocking skews and jitters between frontend modules. The standard deviations of the mean time differences shown above are in the order of about 33 ps, which are essentially due to the noise, timing jitter from the comparators in our test setup and frontend module itself.

Our monitoring sequence repeats every 3200 ns, serving up to 16 FE modules and since it repeats so often, it is possible to use average of subsequent measurements to improve monitoring precision. As an example, we have studied sliding averages of adjacent 4 and 16 measurements and the results are plotted in Fig. 7, along with the one without average.

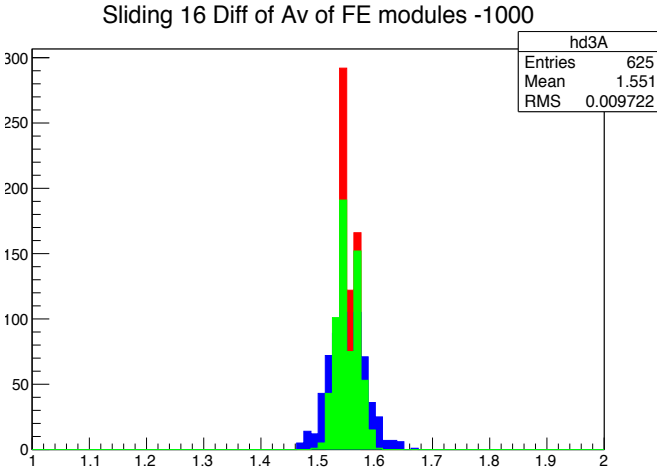

Fig. 7. The differences of the mean times

The histogram plotted in blue above reflects the raw differences of the mean times for two frontend modules with standard deviation of about 33 ps as discussed previously. The green histogram is the distribution of the sliding average of 4 measurements. It can be seen that the width is clearly narrower due to averaging.

When more averages are utilized, the measurement precision is further improved. The red histogram reflects a sliding average of 16 measurements. In this case, the RMS timing measurement precision is better than 10 ps, which is sufficient for timing crosschecking in most detector systems.

IV. The Effects of Delay Variations

To emulate cable delay variations due to temperature, we have studied effects by adding some artificial delays. The BNC connector unions marked x0/x1/x2/x3 as shown in Fig. 8 were added between the cable connecting the evaluation board output and one of the FE to exaggerate variations for observation. Measurements are taken in all these conditions. Clock skews were measured with x0/x1/x2/x3 connector union(s).

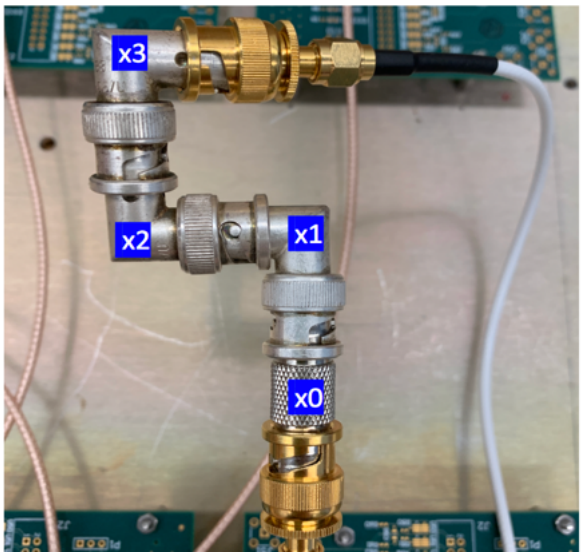

Fig. 8. Photo of added BNC connector unions delays

The histograms for these tests are shown in Fig. 9.

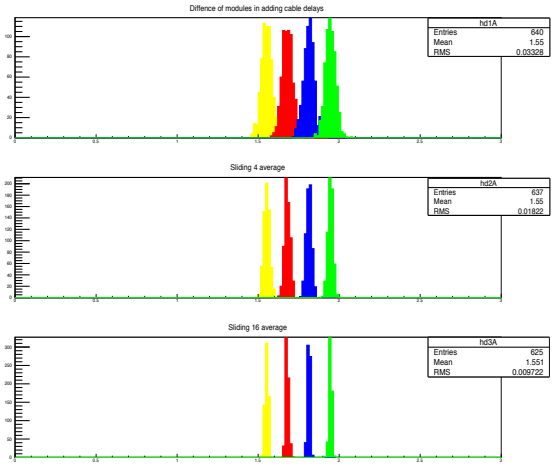

Fig. 9. The histogram for added BNC connector unions delays

These histograms show the clocking skews for two FE modules with x0/x1/x2/x3 cable delays. It can be seen that the difference of mean times between two frontend modules changes for different artificial delays of the clock input to one module. The differences between peaks show that timing delays are around 130-140 ps for each connector added. Clearly, as more sliding average of measurements used, measurement precision of clock skews with added delay between two FE modules is improved.

V. Summary

The cable delay self-cancellation is the key to the effectiveness and simplicity of this type of timing crosschecking scheme. The results of the simple evaluation tests show that a satisfactory timing precision is achievable, even with moderate quality interconnection and far from optimal digitization hardware.

The scheme discussed in this paper requires essentially passive components such as cable and connector at the frontend

module with only a driver having the silicon temperature sensitivity. The TDC on the Timing Cross-checking module can be placed outside detector so that non-radiation tolerant components are needed. Since the timing precision can be improved with averaging of multiple measurements, it is unnecessary to push the TDC and related hardware to the maximum performance.

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