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Assembly of Edgeless Four Side Tileable ROICs for a Wafer Scale, Deadzone-less Camera

Farah Fahim

Abstract– **Deadzone-less, large area camera systems can benefit from the assembly of a wafer scale sensor connected to an array of almost reticule size, 4-side tileable, edgeless readout integrated circuits (ROIC). The design of truly edgeless ROICs, with active area extending to their edges, has been made possible with the advent of 3D integration technologies with high-density interconnects, which enable new routing and I/O paradigms. The design methodology used for two large area, edgeless ROICs, is presented: a single tier, as well as a 3D integrated two tier ROIC. The "SISRO" approach of Segmenting Independent Subchips for Resource Optimization was developed for creating edgeless ROICs. It makes it possible to virtually absorb all the peripheral functionality, including I/O pads, within an area shared by a grouping of pixels. The segmentation into subchips is an unprecedented but effective step to reduce complexity, from over 100 million transistors to less than 500K gates in the examples provided. It greatly improves the ease of integration, particularly because the diverse functional blocks of the subchip require a wide range of assembly techniques from full custom layout to automatic place and route.**

Index Terms—**Edgeless ROICs, subchips, tileable, pixel detector, deadzone-less**

I. Introduction

LARGE area camera systems without dead zones are desirable for several applications ranging from high energy physics, astronomy, medical imaging and photon science.

X-ray diffraction experiments, for example, provide a good illustration of the need for both large area and gapless detectors. Large area detectors in this case allow large wavenumbers for high spatial resolution of the reconstructed image. In these experiments, a given crystal orientation appears as a ring. In pure powder diffraction the intensity of the ring is uniform, hence dead areas can be tolerated [1, 2]. Polycrystals, on the other hand, have scattering centers in the object, which when reconstructed appear as bright spots. In time-dependent studies, the moving of these spots, their blurring out and re-establishment as a material re-crystalizes is the measurement of interest. Gaps in the detector can therefore become a limiting source of inaccuracy when they interfere with the tracking of the temporal and spatial evolution of key spots which represents different phases [3]. Moreover, classic powder diffraction analyses typically perform an angular average around the Ewald sphere intersected by the detector. Gaps in the detector are not a problem when plotting a 1-D radial distribution function. However, for 3D [4] reconstructions, gaps in the Fourier space on the detector lead to image distortion.

Historically, detectors used for fast frame based imaging did not typically require large areas. However, the construction of brighter light sources [5], and the requirement for larger *imaging figure-of-merit* (iFOM), which is field-of-view divided by spatial resolution, have driven the development of X-Ray photon detection systems from detectors with dead regions between read out integrated circuits (ROICs) of a few millimeters [6, 7] to a few hundred microns [8].

The goal of this work is to present a way to further minimize dead zones, by creating four-side tileable ROICs using the back of the ROIC for distributing input/output (I/O) pads instead of the periphery. The "Segmenting Independent Subchips for Resource Optimization" (SISRO) approach is presented, which is a method for absorbing all peripheral functions and I/Os within the pixelated area to create truly edgeless ROICs.

Section II reviews the state of the art towards the implementation of a gapless detector, along with the challenges associated with creating edgeless ROICs. In Section III, the SISRO design approach of subdividing the ROIC into subchips based on optimizing resources is proposed. Section IV describes an example of a 3D integrated ROIC and an equivalent 2D ROIC to which the SISRO approach is applied. In Section V the main challenges of creating a subchip in context of the example are presented, followed by conclusions in Section VI. For clarity and pedagogical value, several of the considerations and steps implemented in the proposed design approach are itemized and listed.

II. Current State of the Art Towards Four Side Tileable ROICs

Before introducing the proposed approach, a survey of the common techniques for detector assembly and the corresponding limitations towards the implementation of gapless detectors is presented. Large area detectors of a few hundred cm^2 consist of an array of either monolithic or hybrid pixel modules. Hybrid modules involve an assembly of pixelated sensors bump bonded to ROICs, where the size of the ROIC is restricted by the integrated circuit fabrication process to a few cm^2. Typically, there is a 1:1 correspondence between

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F. Fahim is with the ASIC Development Group of the Electrical Engineering Department of the Particle Physics Division at the Fermi National Accelerator Laboratory, BP 500, MS 222, Batavia, IL 60510, USA, (telephone: +1 630 840 8423, fax: +1 630 840 2950 farah@fnal.gov

F. Fahim is also a student member of the Bio inspired opto-electronics laboratory in the Department of Electrical and Computer Engineering, Northwestern University, 2145 Sheridan Road, Evanston, IL 60208.

the sensor's and ROIC's pixel geometry, hence the pixelated areas of the ROIC constitute active regions. Conversely, inactive areas include all areas not connected to the sensor, which are primarily designated to peripheral functionality such as bias generators and data transmitters, as well as I/O pads. Dead zones in the detector are primarily the result of either gaps between adjoining ROICs, or the inactive peripheral areas of the ROIC.

The wire bonding of ROICs creates gaps between their assembly, leading to sensing dead zones. ROICs that have active edges extending to three sides, such that the I/O pads and peripheral functionality are only on one side of the device, are 3-side abuttable. Large area pixel detectors consisting of an array of modules with two adjacent rows and multiple columns of 3-side abuttable ROICs have been demonstrated [9, 10, 11]. Such ROICs can also be assembled in a shingled or a roof-tile geometry [12] to provide full coverage by overlapping modules, but the ensuing uneven surface can result in image distortion. Stitching technologies [13] allow increasing the ROIC area by seamlessly integrating multiple dies, as demonstrated in [14, 15, 16]. More elaborate stitching techniques such as the one proposed in [17] allow integration of heterogeneous multi-die in a small footprint with high-performance interconnects.

Large area, gapless detectors can be created, by bonding edgeless ROICs with active areas extending to all edges to wafer scale sensors. Such edgeless ROICs must be designed by absorbing the peripheral functionality into the pixelated area. To minimize gaps between ROICs, through-silicon vias (TSVs) can be used to distribute I/O pads across the backside of the ROIC instead of the periphery.

The advent and increased reliability of 3D integration technologies [18] with high-density interconnects has made new routing and I/O paradigms available to designers. Large diameter TSVs at the periphery have led to "almost edgeless" ROICs, to enable 4-side abuttability and reduced gaps in the detector through the elimination of wirebonds. As shown in **Error! Reference source not found.**a, TSVs are inserted in the periphery, followed by deposition of back metal pads for bump-bonding to the PCB. The TSVs used in this approach are approximately ~ 50 µm wide with a depth of ~ 100 µm, and have high capacitance. They are generally used to carry I/Os from one side to the other. The redistribution layer can then be used to fan out signals to create a backside ball grid array for bonding to the PCB [19]. Despite being 4-side abuttable, these ROICs retain relatively large peripheral dead zones [20, 21].

The "truly edgeless" approach as shown in **Error! Reference source not found.**b, on the other hand, utilizes small diameter, shallow TSVs, approximately ~1 µm wide and ~10 µm deep, with a dense pitch of ~2 µm. The ROICs need to be thinned to approximately 10 µm for insertion of these TSVs. Thinning wafers to 10 µm necessitates either temporary bonding to a handle wafer or 3D bonding to another wafer. Low-temperature direct-bond interconnect (LTD) [22, 23] can be used to create 3D integrated ROICs composed of multiple tiers with dense signal exchange through short, low-capacitance, inter-tier bonding interfaces such as used in [24]. This assembly is thinned, the backside TSVs (B-TSVs) are inserted and the back metal pads are deposited. The processed single tier ROICs with handle wafer or two tier 3D integrated ROICs undergo further processing on the opposite side and after determining the known good dies are singulated and LTD bonded to a wafer scale sensor. These ROICs can be designed to be edgeless with no peripheral functionality, allowing the creation of large area camera systems with minimal sensing dead zones of less than one-pixel width. This gap of less than one pixel can be completely eliminated by a minor fanout of a slightly larger sensor pixel to create systems with no dead zones. Table 1 shows the comparison between leading ROICs designed to reduce sensing gaps.

Table 1. Performance metric comparison between pixel ROICs utilizing TSVs for minimizing dead zones. The approach presented in this work allows for no sensing gap for up to a wafer scale sensor.

	Medipix3 [19]	UFXC32k [21]	Timepix4 [25]	This work : VIPIC_L (2-tiers)
4-side abuttable	No	No	Yes	Yes
ROIC assembly	Super pixels with peripheral logic	Super pixels with peripheral logic	Super pixels with peripheral logic	Independent subchips no peripheral logic
Pixel pitch	55 µm	75 µm	52 µm	65 µm
RDL between sensor & ROIC I/P	No	No	Yes, sensor pitch 55 µm	Minimal, sensor pitch 65.34 µm
TSV size	Large diameter (60 µm / 40 µm)	Large diameter (20 µm)	N/A	Small diameter (1.2 µm)
TSV placement	One edge at periphery to eliminate wire bonding; backside surface redistribution using RDL		Top edge, bottom edge and center row	across the ROIC substrate at ~500 µm pitch
Thinning	120 µm / 50 µm	100 µm	N/A	~ 10 µm
Chip size	1.98 cm^2	2 cm^2	6.94 cm^2	1.56 cm^2
Chip periphery	2130 µm	900 µm	800 µm (analog periphery) + 400 µm (digital periphery)	14 µm
Sensing gap between dies	> 2 mm	~1 mm (edge with periphery) 6 µm lateral active edge	RDL to compensate for 400 µm; increases I/P capacitance by 30-50 fF	None, up to wafer scale sensor

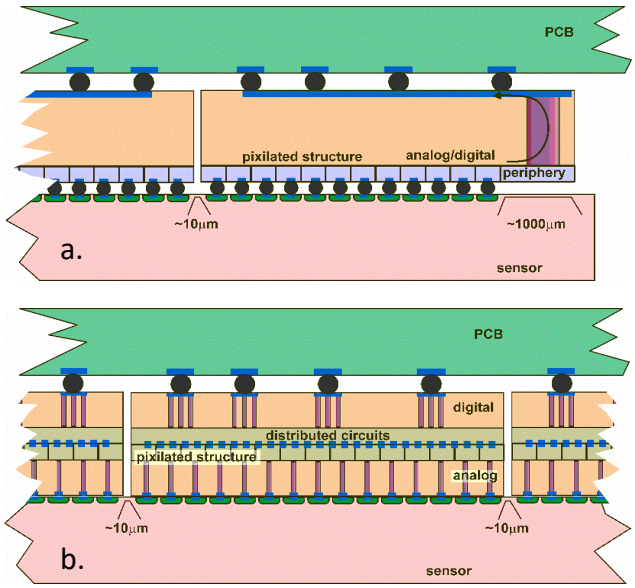

Fig. 1 a. "Almost Edgeless" detector system with peripheries greater than 1000 μm. b. "Edgeless 3D" with gaps less than 10 μm between ROICs [26].

Challenges in the creation of edgeless ROICs

Despite their obvious potential, the realization and widespread development of truly edgeless ROICs has faced several obstacles. In this section we present some of the distinctive technological and design challenges that must be confronted for this particular application. Where appropriate a mitigation strategy is also proposed.

– *Manufacturing processes related to 3D integration* – LTD bonding [**Error! Bookmark not defined.**, **Error! Bookmark not defined.**], B-TSV insertion, back metal deposition are currently not part of the standard CMOS fabrication process. These additional steps are performed by third party vendors, which can impact the yield of the camera in addition to increasing processing times. Recently however, major foundries such as Taiwan Semiconductor (TSMC) and Global Foundry (GF) have started offering 3D integration on advanced process nodes for large volume applications, and this trend is expected to become mainstream [27].

– *Complexity of readout board* - Arrays of ROICs with sizes greater than 1 cm^2 with backside I/O pitches of 400 – 800 μm containing almost a thousand I/O pads each, require advanced substrate designs (e.g. printed circuit board, ceramic board etc.) utilizing blind, buried and micro vias with tens of layers. This further increases the risks associated with the development.

– *Lack of a sealring* - A sealring, composed of one or more interconnected metal layers, typically encapsulates the IC and isolates the silicon from the external environment. It is especially required during the die-sawing stage as it minimizes the impact of tensile stress, prevents degradation due to moisture and protects against ionic contamination [28]. To mitigate this risk, a ~5 μm ring of dummy metal layers from metal 1 to metal top can be placed along the edge of the ROIC. Like the traditional sealring, it may also be electrically connected to ground. However, even when the mechanical, wet die-sawing stage is replaced by dry reactive ion etch (RIE) process to precisely singulate the dies, the lack of a sealring might still degrade the lifetime of the ROIC.

– *Distributed ESD structures across the ROIC* - Electrostatic discharge (ESD) protection circuits with guard rings are required for all I/O pads. However, these structures are not a part of a continuous I/O ring with well-defined isolation, but are distributed across the subchip in close proximity to analog and digital circuits. The impact of such structures on neighboring functionality has not been studied.

– *Pixel-to-pixel variations* - The analog sections in a single tier and the analog tier in a two tier ROIC are pixelated, while the associated digital logic is not physically constrained within a pixel. The non-uniformity of the digital circuits can lead to pixel-to-pixel variations: for example, analog pixels in close proximity to high-speed I/Os can exhibit higher noise due to substrate coupling. These areas can be identified by dynamic power hotspot maps of the layout, which can be generated by standard digital flow EDA tools. The separation of analog and digital functions in two tiers reduces the coupling by isolating and shielding the functionality. However, it is conceivable that, by grouping a large number of pixels, the SISRO approach might exacerbate pixel-to-pixel variations in a single tier ROIC.

III. Segmenting Independent Subchips for Resource Optimization ("SISRO") Approach

To assemble a large edgeless ROIC, we propose that it be sub-divided into several smaller edgeless subchips, each containing an array of pixels as shown in Fig. 2. Each subchip becomes an indivisible unit for further assembly. This is an essential, unprecedented implementation step, for the deadzone-less floorplan of the detector. The key feature of 3D integration technology being exploited for this approach is backside through silicon vias (B-TSVs), which enable the use of the backside of the chip for data transfer instead of its periphery. Bump-bond I/O pads are distributed across the back to create a ball grid array, for connection to the readout board. This approach of segmenting into independent subchips is based on optimized sharing of both spatial and functional resources. The subchip is functionally independent, however at the next hierarchical level when it is tiled to create a chip, certain layers abut to create continuity of the power supply and bias grid and other shared signals (if necessary), in a manner similar to the traditional pixel assembly. The choice for the optimum number of pixels in a sub-chip, which can lead to an independent unit is influenced by several factors such as:

- *The ratio of area required for peripheral logic vs. in-pixel logic within a subchip* - A low ratio (1-5%) ensures that the peripheral functionality can easily be absorbed within the active area, without increasing the size of the pixel, through improved area utilization by the EDA (Electronic Design Automation) Place and Route (P&R) tool. As an example, when a pixel has 1% extra area, merging it across 1000 pixels accounts for an area equivalent to ten pixels. This area could be optimally utilized to absorb the peripheral functionality, which otherwise could not be distributed piece-wise across 1000 pixels.

- *Size of the subchip* - Layout area and number of transistors in a subchip, influence the ease of integration and verification. A design with total number of gates between 300K – 500K can be easily handled by standard EDA tools for synthesis, P&R and verification. Much larger designs not only require

additional resources (such as multiple processors and licenses) but also take longer to complete a full iterative design cycle.

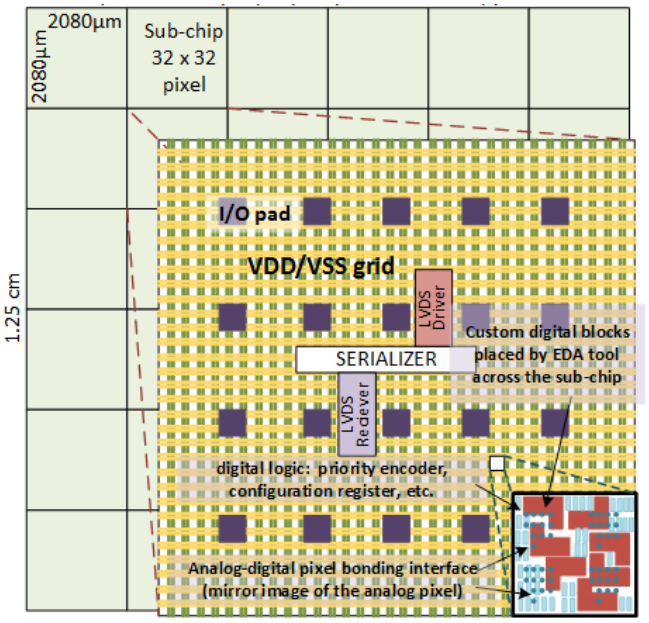

Fig. 2 An Array of 6 × 6 subchips assembled to create a large area edgeless ROIC. Each subchip contains the logic of 1024 pixels with 20 I/O pads and other peripheral functionality. The pixel logic is not confined to a repeatable placement pattern to accommodate the placement of peripheral logic in strategic locations.

- *System readout requirements* – The number of parallel data outputs defines the full frame readout rate. If every subchip has its own data output, the full system frame rate is the same as the frame rate of the subchip, which is a function of the number of bits in the data packet, the number of pixels and the readout speed. In systems with zero-suppressed frame readout, the data packet includes both the number of bits of data (e.g. number of photons counted by the pixel) and the length of pixel address. The pixel address is determined by the number of pixels within a subchip.
- *Number of I/O's* - Global I/O's such as biases and clock signals can typically be shared across subchips. The number of dedicated I/O's required per subchip determines the minimum number of pads required and consequently the minimum area of the subchip.
- *Backside bonding* - The horizontal and vertical pitch of the backside distributed I/O pads will determine the area of the subchip. It also impacts the complexity of the readout board.

Advantages of the SISRO approach

The SISRO approach effectively exploits the repetitive nature of large pixel detectors, by identifying a self-contained, independent design building block. It is applicable to both 3D and 2D ROICs. This hierarchical structure has several advantages, such as:

- Mitigate risk in the assembly of large, reticule size chips by focusing on the design of smaller subchips for efficient usage of time and effectiveness of EDA tools for both iterative assembly as well as verification.
- Ease of scaling and assembly of reticule size chip. The final assembly step is as simple as creating arrays of subchips and ensuring no design rule violations occur from abutting several subchips.
- Allows massively parallel readout for orders of magnitude higher full frame rates by allocating one or more low capacitance readout I/O's per subchip to increase the number of parallel output ports [29]
- The readout architecture is optimized for small subchip areas (few mm^2), hence higher speeds can be achieved, as it does not have the constraints associated with moving data from one end of the ROIC to the opposite end (~ cm) required for data transfer through the periphery [30].
- By not having a single uniform pixel, but rather a larger subchip, functional resources such as memory blocks, data converters, etc. can be shared across a group of pixels and be dynamically allocated based on usage.
- Allows for multiple reconfigurable regions of interest. Since each subchip is independent, different subchips can operate in different modes. For example, when one subchip is operating in full frame imaging mode with a photon collection window of a few milliseconds, another subchip could be operating in zero suppressed mode with a window of a few hundred nanoseconds [31].

IV. Example Application to Edgeless 3D and 2D ROICs

In this section, we present an example of the application of the SISRO method to the design of a single tier and of a two tier photon counting ROICs. They contain the same functionality but differ in pixel sizes. The two tier ROIC was manufactured in a 130 nm CMOS process. The single tier ROIC was designed in the same process for demonstration purposes but was not manufactured. The spatial and functional properties of the two photon imaging ROICs, along with the information required to determine the size of the subchip, have been listed in

Table 2. The pixel size is defined by the application, or otherwise limited by the smallest achievable size compatible with the required in-pixel functionality. In this instance a pixel size of 65 × 65 μm^2 was achieved by optimizing the layout of a previous test structure [**Error! Bookmark not defined.**], which allowed a 30% area reduction while simultaneously expanding the analog and digital functionalities to meet the requirements set by the beamline instrumentation application.

For the two tier IC, the pixel size is mainly constrained by the minimum analog pixel size. In the case of the single tier ROIC, the pixel size of 100 × 100 μm^2 represents an increase of 18% with respect to the combined pixel area of the two layer ROIC. The additional area is required to accommodate for the separation between the analog and digital sections in independent deep nwell (DNW), as well as to compensate for the 50% reduction in the number of metal layers available.

- When grouping pixels together and determining the size of the subchip, we can first start with calculating the total number of pixels based on the size of the full chip. Then depending on the desired system frame rate, the total number of parallel outputs required can be computed based on the output line driver speed. This gives an initial approximation of the number of pixels that can be grouped together (total no. of pixels / total no. of parallel readout ports).
- Each subchip needs both dedicated I/Os (e.g. data outputs), as well as global I/Os (e.g. power supplies and biases)

which can be shared between subchips. The minimum number of pads within one subchips is therefore the number of dedicated I/Os, plus one or more global I/Os depending on the extent of sharing. The area of the subchip should be compatible with the area required for I/Os (No. of I/Os × I/O distribution pitch).

- The length of the data packet which includes the pixel address is dependent on the size of the subchip array. Also, for a given readout bandwidth for zero-suppressed readout, the larger the subchip, the larger the losses for a given pixel occupancy.

- The number of transistors and gates in the design is an important factor when considering efficient P&R tool usage. An approximate number of subchips can be calculated based on (Total no. of gates/ 300K - 500K).

- Finally, checking that the ratio of the total area of the peripheral functionality to the total in-pixel area of the subchip is low, is a good way to ensure that the pixel size can accommodate the additional functionality without expanding significantly.

The application needs should be given priority when balancing different factors in this decision making process. Based on the data from

Table 2, a minimum subchip size of approximately 1000 pixels with one output, or a maximum subchip size of 4000 pixels with at least four parallel outputs, meet the specifications. Hence a subchip size of 32 × 32 pixels was chosen.

Table 2. Spatial and functional properties of the 3D and 2D photon imaging ROIC with a subchip size of 32 × 32 pixels

	Vertically Integrated Photon Imaging Chip : **VIPIC_L** [29, 32]	Edgeless Photon Imaging Chip : **Edgeless_2D_PIC**
Pixel size	Two tiers of 65 μm × 65 μm Total area : 8450 μm^2	100 μm × 100 μm Total area : 10000 μm^2
No. of routing layers	8 × 2 = 16	8
Size of ROIC	1.25 cm × 1.25 cm [192 × 192]	1.28 cm × 1.28 cm [128 × 128]
Backside I/O pad pitch	~ 400 μm – 800 μm	
Total number of transistors in design	~ 120 million	~ 80 million
In-pixel functions	Preamplifier, Shaper, window discriminator, hit processor, two counters (7 bit), configuration register (21 bit), priority encoder logic	
Digital functional area before routing (per pixel)	~ 7180 μm^2 (Approximation from synthesis tool, or custom digital block size)	
Peripheral functions	I/O pads with ESD protection, high speed output serializer, analog bias block, LVDS driver and receiver.	
Peripheral functional area	~ 100,000 μm^2 [approximately 20 I/O pads per subchip]	
Global I/O	Analog, Digital Power and Ground, LVDS Power and bias, Analog Biases (6), control of test injection switches, digital reset [~Total = 15]	
Dedicated I/O	Configuration register clock, input, output and reset, LVDS Data output, LVDS clock input, frame clock [~Total = 10]	
Readout architecture	Reconfigurable : Imaging and Zero-suppressed with user programmable window of exposure and data length (no. of output data bits)	
Full-frame imaging rate with one data output per subchip (output clock = 400 MHz)	> 50 kfps : [For a pixel with 7 bit data packet and output serializer operating at 400 MHz, with one data output, aggregating 1024 pixels yields ~ 55 kfps]	
Zero suppressed readout	< 0.4% occupancy for a time window of 150 ns [output serializer operating at 400 MHz, with one data output per subchip; 4 out of 1024 pixels can be read out within 150 ns with 2 bit data + 10 bit address]	
SUBCHIP		
Size of subchip	32 × 32 = 1024 pixels	
No. of subchips	6 × 6 = 36	4 × 4 = 16
Area of subchip	2 mm × 2 mm	3.2 mm × 3.2 mm
No. of gates for digital-on-top assembly per subchip	400 K	
Ratio of peripheral function to total in-pixel function	100000/ (7180 * 1024) ~ 1.5%	
Total area available for routing, clock tree distribution, etc. per subchip	13%	21% [Note : also includes area for placing the analog and digital sections in independent triple wells]

A. Example of 3D Integrated Edgeless two tier ROIC

A gapless, large area 3-layer detector system as shown in Fig. 3 with one sensor layer and 3D integrated edgeless ROIC with one analog and one digital tier. A micro photograph of the two tiers before 3D integration is shown in Fig. 4. Such edgeless ROICs can be precisely diced using reactive ion etching, and can be placed just 10 – 20 µm apart, which is less than the size of a single pixel. A minor fanout to a sensor with slightly larger pixel pitch can then be used to create a gapless detector. The Vertically Integrated Photon Imaging Chip - Large (VIPIC-L) is a large area, edgeless, small pixel (65 µm pitch for the ROIC, 65.34 µm for the sensor), 3D integrated ROIC designed for X-ray correlation spectroscopy. The analog and digital tiers of VIPIC-L contain 192 × 192 pixel array. The ROIC size is 1.25 × 1.25 cm^2 with only a 7 µm periphery [32]. In this instance the ROIC was chosen based on the available reticule for a multiproject wafer. The SISRO approach is equally applicable to other sizes, and is particularly suited for large reticule size chips.

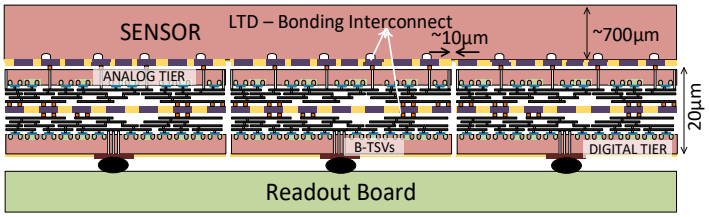

Fig. 3 Vertically integrated, gapless, large area 3-layer 3D detector system with one wafer scale sensor layer connected to an array of 3D ROICs containing one analog and one digital tier.

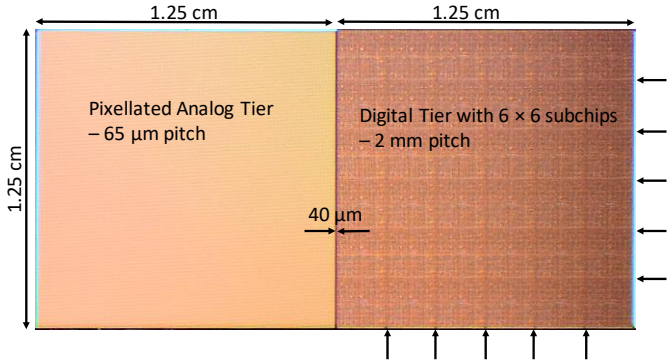

Fig. 4 Microphotograph of the manufactured VIPIC-L analog and digital tiers. The active edge extends to the edge of the reticle, with no peripheral I/O pads. The two chips are placed 40 µm apart on the same reticle in the wafer, the gap is used as a dicing street to precisely singulate dies after 3D assembly of the wafers. The 6 × 6 array of subchips in the digital tier can be discerned, with boundaries indicated by the arrows.

It contains about 120 million transistors, with approximately 100 million transistors in the digital tier and the remaining in the analog tier. An array of 30 × 24 I/O bond pads are distributed across the back of the die, at a pitch of approximately 500 µm, which corresponds to 720 bond pads in a 1.6 cm^2 area connected to the readout board. A deadzone-less, wafer scale, megapixel camera system can be created by tiling an array of 6 × 6 VIPIC-L ROICs to a 6 inch sensor wafer [33]. The 1.3 M pixel system can achieve a full frame rate of 56 kfps or a zero-suppressed data rate of 1.44 G packet/s.

i. Edgeless Analog Tier

To create the edgeless analog ROIC tier, the analog bias block (Fig. 5a), which in this instance is the only peripheral block, must be absorbed within a single pixel boundary. This is achieved by creating a few different flavors of analog pixels by distributing the biasing transistors across the various flavors as shown in Fig. 5b, and subsequently tiling their layouts to create a biasing grid. Small transistors distributed in parallel across multiple pixels can thus be used in place of large ones with multiple fingers, typically favored for bias generation. In the 3D integrated ROIC structure the analog tier does not contain any I/O pads, all power and biasing signals to this tier are provided through the digital tier. A grid of top metal layers, as shown in Fig. 6 for global power, ground and bias signals, connects at specific locations through the bonding interface to the digital tier.

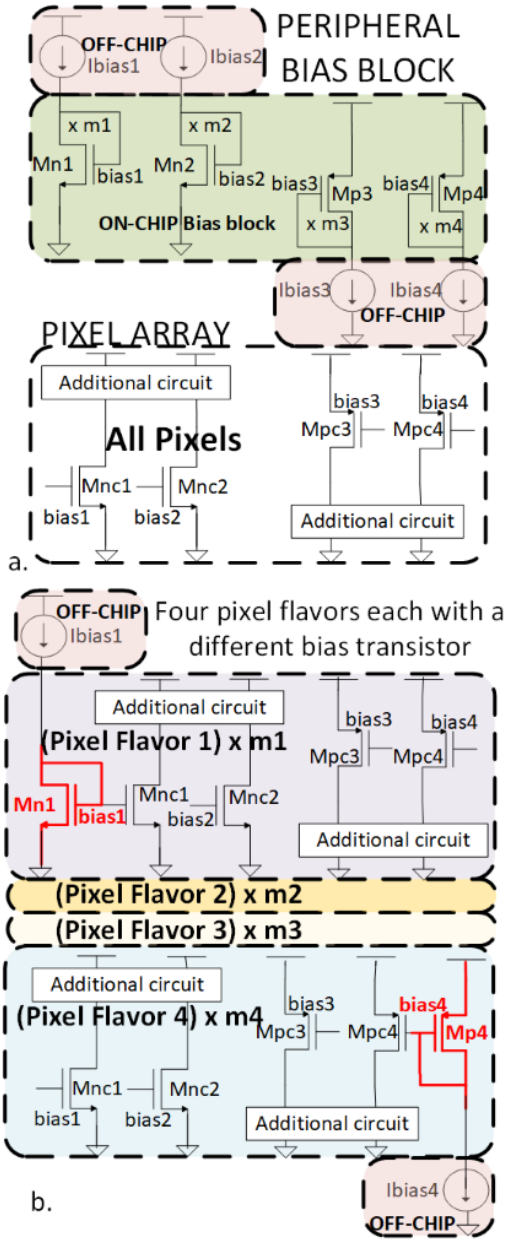

Fig. 5. a. Peripheral bias block as traditionally connected to an array of identical pixels. b. Schematic of different pixel flavors each with a different bias transistor.

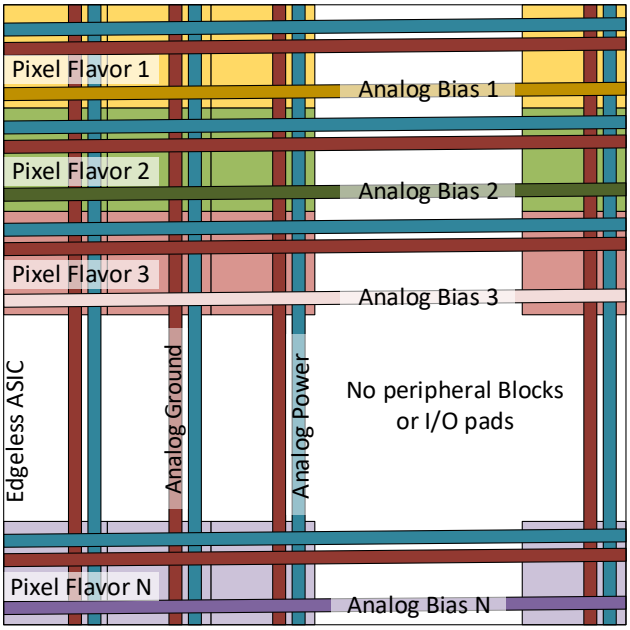

Fig. 6 Edgeless analog ROIC tier assembled using a few different flavors of Analog Pixel, each incorporating a different bias transistor. Power, ground and bias signals are supplied via the digital tier through the bonding interface to the analog tier. For clarity, the vertical distribution of biases across all pixels is not shown.

In addition to global signals, several pixel level signals need to be interconnected between the analog pixel and the digital pixel logic. Examples include the output of discriminators from the analog pixel and configuration lines for the analog pixel. The analog and digital tiers are face-to-face bonded through their respective top metals via a fusion bonding interface. Hence the digital tier needs to mirror the bonding interface of the analog tier. The bonding interface provides both electrical interconnection and mechanical support. Fig. 7 shows the bonding interface for VIPIC-L, which consists of an array of 13 × 13 octagonal bond posts, each 2.5 µm in diameter, arranged at a 5 µm pitch. The posts which are used for signal exchange connect through multiple vias to the top routing metal layer (last foundry metal layer), which are then routed to the relevant circuitry. Approximately 25% of the posts are used for electrical connectivity, with the remaining posts providing mechanical support. At the chip level, this translates to more than 1.5M electrical interconnections. Global analog I/O such as power supply, ground and biases are also distributed via the bonding interface, however they are not repeated at the pixel pitch, but rather confined to specific locations recurring at a subchip pitch. Some of the extra posts for mechanical connectivity in the pixel are used for this purpose.

i. Edgeless Digital Tier

A similarly uniform and repeatable digital pixel cannot be created, as the peripheral functional blocks such as the output data transmitter, line drivers and receivers are large, need to be strategically located, and cannot be distributed piecewise within pixels. In VIPIC-L, the 1.25 × 1.25 cm^2 edgeless digital tier consists of approximately 100 million transistors, more that 1.5 million front-side electrical interconnections between tiers, and nearly one thousand back side I/O pads to the readout board. To deal with the constraints imposed by the single pixels on one hand, and the complexity of the large chip on the other, the SISRO approach prescribes the instantiation of independent modular subchips. The subchip in VIPIC-L corresponds to 32 × 32 analog pixels. This not only leads to a significant simplification for assembly, whereby each subchip has approximately 3 million transistors, 40K interconnections and 20 I/O pads, but also allows for optimization of functional resources.

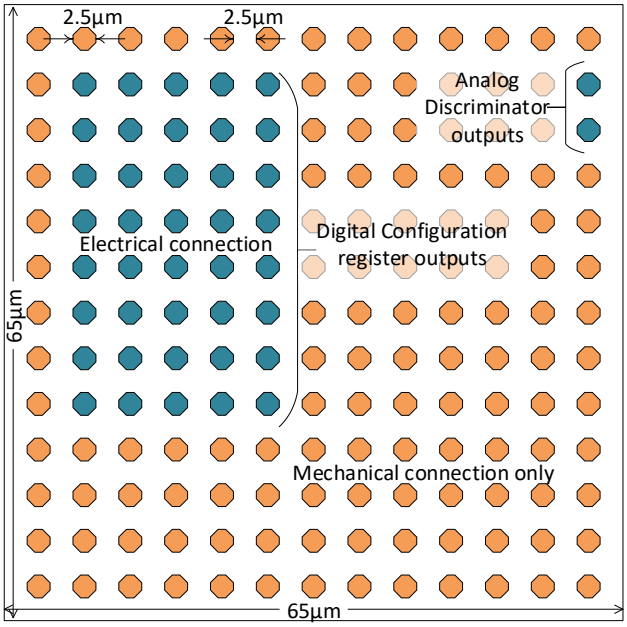

Fig. 7 Bonding interface for the analog pixel of VIPIC-L, showing the repeatable pattern array of 13 × 13 bond posts. 42 of these (in blue) are electrical interconnections to the digital section, with the remaining used as mechanical connections or occasionally for global signals.

B. Example of Single Tier Edgeless ROIC

The second example of the application of the SISRO approach to the design of a large gapless detector, is a two layer system combining one sensor layer (such as pixelated Si) and one ROIC layer, also accomplished by using backside through silicon vias B-TSVs, as shown in Fig. 8. The Edgeless 2D Photon Imaging Chip was designed for demonstration purposes only and is not a manufactured ROIC. It is a large area, edgeless ROIC containing a 128 × 128 array of 100 µm × 100 µm pixels. The larger pixel size corresponds to approximately two times the 3D pixel area. The chip size is 1.28 cm × 1.28 cm, with only a 7 µm periphery. The backside has an array of 20 × 16 bond pads distributed across the back of the die, with a pitch of approximately 800 µm. As shown in Fig. 12a, four analog sections are combined together to create an analog island, which is placed in a triple well occupying 140 µm × 140 µm; I/O pads can be placed in between analog islands.

With approximately 80 million transistors and one million interconnections between the analog islands and the digital logic, the 2D ROIC has the same spatial, functional, timing and I/O constraints as the digital tier of the 3D ROIC discussed in the previous section.

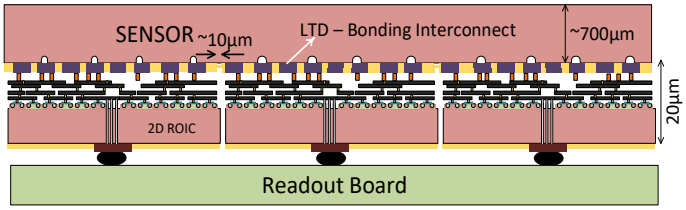

Fig. 8 Large area two layer gapless detector system with one wafer scale sensor layer bonded to an array of traditional 2D ROICs. Sensor is oxide-oxide bonded to the top metal layer, whereas back side I/O pads are bump bonded to the PCB.

V. Constraints In Assembling A subchip

The SISRO approach eases some of the chip level constraints by scaling them to manageable smaller subchips. The constraints with regards to the above examples is discussed in this section with the overarching theme of 'divide and conquer'. The assembly of the subchip is an iterative process, which starts with defining a floorplan based on spatial constraints and I/O constraints, while satisfying the timing and functional requirements. The detailed methodology for assembly of pixel detectors is discussed in [34]. This section outlines the key issues associated with this process.

A. Floorplanning Constraints:

- *Define the size of the subchip.* Once the size of the subchip has been determined, the tool cannot be given free rein to place digital logic within the subchip area solely based on timing constraints.

- *Define pins associated with signal interchange between analog and digital sections*. In the 3D ROIC, the top metal bonding interface, with the pin positions associated with the inter-tier signal interchange, is set by the analog tier. Each bonding interface element with electrical connection to the analog pixel is placed as a 'fixed pin' for the P&R tool, to connect the relevant signals. Similarly, in the 2D ROIC, the pin positions at the periphery of the analog islands are defined. This interface is repeated at the pixel pitch for a total of over 40K interconnection per subchip, and sets the signal routing constraints for the two designs.

- *Define I/O pad placement.* Each subchip has 20 I/O pads placed at a predetermined pitch used for sending and receiving signals. In both ROICs, B-TSVs for I/O pads land on metal 1, as shown in Fig. 9a, hence these constitute exclusion areas where no transistors can be placed. Furthermore, for 3D ROICs, the subset of I/O pads carrying power, ground and global bias signals to the analog tier must be conveyed through the digital tier. These require the usage of all metal layers, and are ideally implemented as "pillars", as shown in Fig. 9b. Hence placement and routing blockages for the entire metal stack are created within the subchip for distributing these signals. Floorplanning should also take into consideration the placement of ESD protection circuits close to the I/O pads. The requirement for slots in large metal shapes, to provide thermal stress relief during fabrication, influences the placement of B-TSVs. Additional I/O-related constraints not specific to floorplanning are dealt with in the next subsection.

- *Strategic placement of larger blocks.* The next step is to identify the best locations for the placement of hard macros, such as data transmitters, line drivers and receivers, which sets additional exclusion regions. For example, the data controller and transmitter should be centrally located within the subchip, to minimize skew and power consumption due to parasitic capacitances.

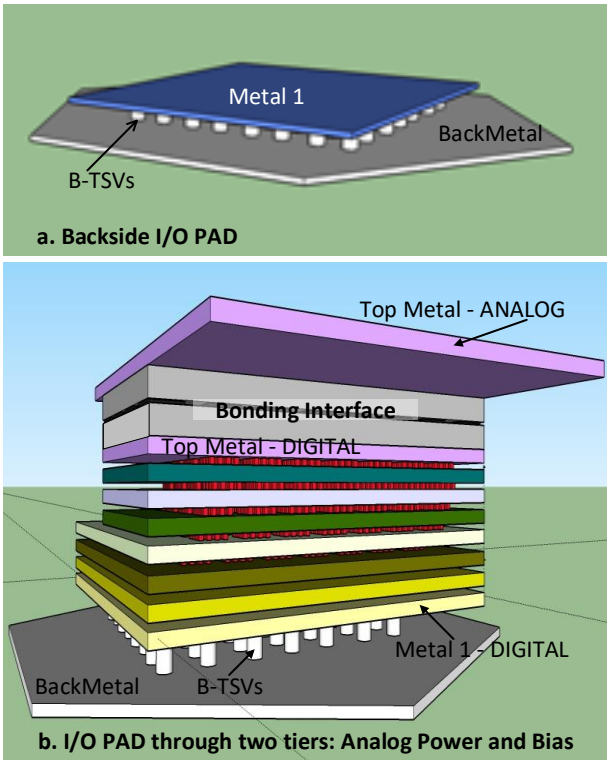

Fig. 9a. Single tier backside I/O pad connects back metal to metal 1 using B-TSVs, further metal layers might be required depending on the type and location of the signal. 9b. Two tier backside I/O pad allows analog power and bias signals to traverse through the digital tier and then the bonding interface to reach the top metal of the analog tier in the 3D ROIC. It appears like a tall pillar through the digital tier with blockage on metal 1 through metal top.

- *Digital logic place and route.* With all the signal interchange and exclusion areas well defined, the final step is to assemble the digital functionality, managing placement and routing congestion.

In VIPIC-L, approximately 85% of the total subchip area is occupied by the 1024 digital pixel logic, with an additional 2% used by the peripheral logic, as shown in Fig. 10. Occupancy above 70% is considered high utilization. Only 13% remains available for synthesis, routing, buffering, and clock tree distribution, which could lead to congestion and often failure in assembly. In the edgeless 2D ROIC, after accounting for the design rules associated with placement of analog and digital circuits in independent wells (triple well option), the available area is approximately 20%. The utilization figures for the 2 × 2 mm^2 subchip with ~400K gates equally applies to the 12.5 × 12.5 mm^2 full size chip, with ~14M gates. The former, however, is much more manageable in terms of resources (e.g. computing, tool licenses, time) and iterations required to close the design, while also likely resulting in better optimization.

This validates the SISRO approach as an effective methodology to design edgeless ROICs with very high level of area utilization and complexity.

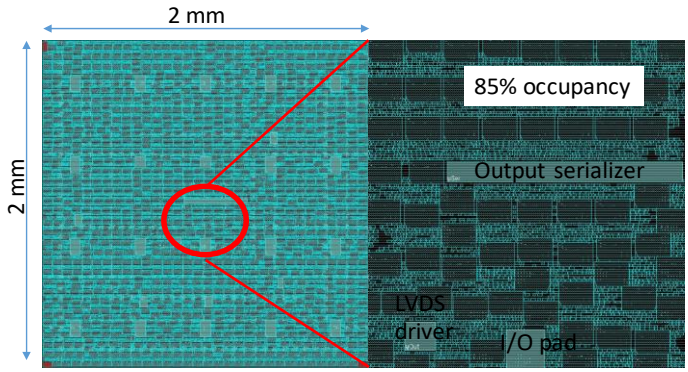

Fig. 10 Edgeless subchip with 85% occupancy. The zoom in shows the high area utilization and the placement of various functional blocks.

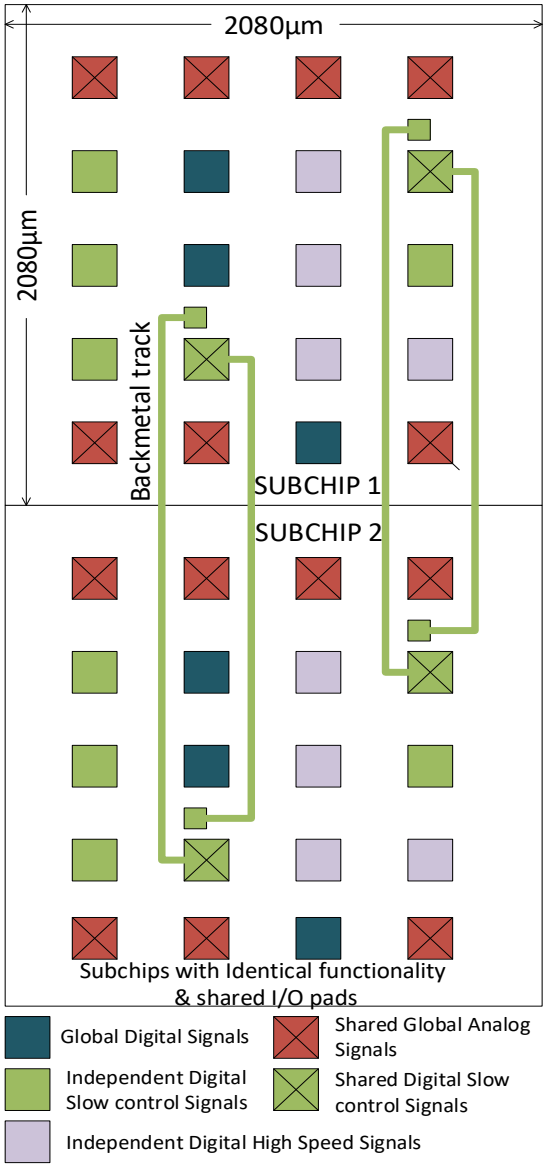

Fig. 11 Back view of two independent subchips with shared I/O pads. These back metal I/O pads are connected to the metal 1 of the ROIC with backside through silicon vias (B-TSVs). The global analog I/O pads are shared between subchips, however these signals are connected within the ROIC across all pixels. The shared digital slow control signals are connected on the back side of the ROIC using back-metal tracks.

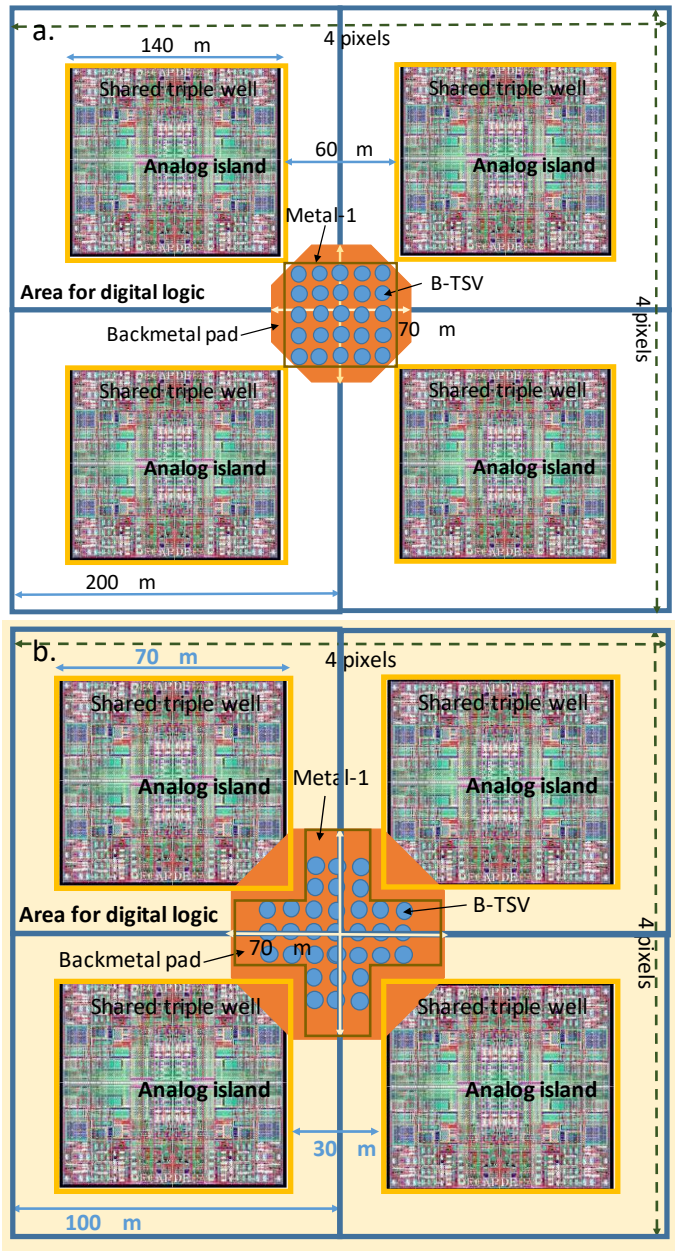

Fig. 12 Placement of I/O pads between analog islands for 2D ROICs. Two different design layouts of 16 pixels are shown, with placement of a 70 µm × 70 µm backside I/O pad in-between analog islands consisting of four-pixels grouped together. *a)* Pixel size of 100 µm with 60 µm gaps for placement of I/O and *b)* Pixel size of 50 µm with 30 µm gaps respectively for placement of I/O. Note: the two designs have different scales.

B. I/O constraints:

- *Sharing of global I/O pads across subchips*. Since the number of analog global signals (18) is larger than the number of available pads in a single subchip (9), to optimally use I/O resources, all analog global signals are shared between two subchips as shown in Fig. 11. These do not need to be connected through back metal, but instead abut through the metal grid inside the chip, as shown in Fig. 6.
- *Back metal redistribution.* Some of the digital slow control signals are also shared, and are made available to the adjoining subchip by re-routing via a back metal trace to a mini I/O pad. These mini I/O pads are not used for bump bonding but are used solely to avoid the design of two different subchips. They allow

the pin position of slow control signals to be swapped at the final step, to create two subchips with minimal variation.

- *Propagation of global signals through the bonding interface.* All pads that go to the analog tier should not overlap with the fixed pixel bonding interface. This is not trivial since the size of the bump-bond pads (60 µm × 60 µm) is comparable to the size of pixels.

- *Avoid congestion hotspots.* The I/O "pillars" mentioned in the previous subsection entail large and localized routing blockages across all metals, which can lead to congestion hotspots. As shown in Fig. 11 the pillars associated with the analog global signals are placed at the opposite outer rows of the subchip.

- *Avoid IR drops.* A uniform I/O grid for power distribution is one of the advantages of using B-TSVs across the entire area of the ROIC instead of just the sides. To avoid interconnect resistance (IR) drops across the large area ROIC, 22% of the pads are reserved for this purpose.

- *Overcome limitation due to the scaling of pixel sizes in 2D ROIC*. In 2D ROICs, I/O pads can only be placed between analog islands as shown in Fig. **12**a. As the size of the detector pixel decreases to improve image resolution, so does the gap between analog islands. For example, as pixel sizes decreases from 100 µm to 50 µm, the gap between the analog islands decreases from 60 µm to 30 µm respectively. The 30 µm gap is not large enough to accommodate a 70 µm I/O pad. In such cases, although the size of the back metal does not need to change, the layout of metal 1 and placement of B-TSVs needs to be tailored to fit, as shown in Fig. **12**b, to accommodate for the reduced area between analog islands. Localized physical relocation of analog islands with a minor fan out of the pixel to the front-side sensor bonding interface can also provide the required gap to insert backside I/O pads.

C. Place and Route timing constraints:

The functionality of the digital tier includes both high speed, localized blocks, as well as slow control, distributed blocks, with vastly different timing requirements, which are alleviated by dividing the design into subchips.

For example, the data control and transmitter block (30 µm × 300 µm) synchronously receives data from the pixels and sends them out of the ROIC at high speed (e.g. 400 Mbps in VIPIC-L). Good clock distribution and careful design of output busses to minimize parasitics therefore become critical. Conversely, the configuration register of 25 bits per pixel, daisy-chained in a single shift register of approximately 25K bits, operates at ~ 1 MHz and is distributed over the entire subchip area (2080 µm × 2080 µm).

D. Functional constraints:

Depending on the logical functions and the timing requirements of the blocks, a full-custom, semi-custom, or automatic place and route (or a combination thereof) should be employed to best deal with the functionally diverse blocks within a subchip.

In both ROICs the pixel logic is used for registering asynchronous photon arrival. Asynchronous blocks such as the hit processor and Gray code counters are sensitive to glitches, requiring a full custom assembly approach. These are placed close to the comparator outputs from the analog section.

The output serializer, on the other hand, is assembled as an independent block through timing-driven automated P&R, and is centrally placed in the subchip, in close proximity to the input and output line drivers. The aforementioned distributed configuration register is also an example of timing-driven P&R. Finally, a constraint-guided semi-custom design assembly is required for the readout architecture. In this instance, a binary tree priority encoder [30] is implemented to select pixels for readout and enable the transfer of data from the pixels to the periphery, along with generating the addresses of the selected pixels. A symmetrical mirror clone-placement and route allows to minimize pixel-to-pixel timing skew in selection and data transfer. Such diversity is challenging from an EDA tool perspective. As shown in Fig. 13, the various blocks communicate extensively with each other, and thus should be concurrently optimized.

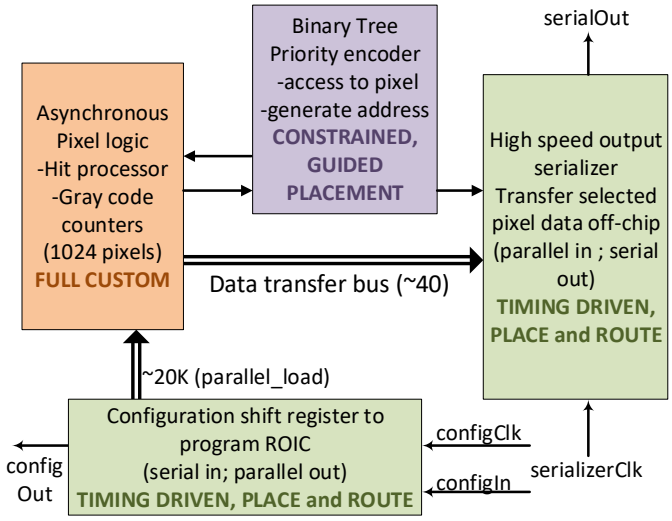

Fig. 13 Subchip functionality consists of asynchronous pixel logic requiring a full custom design, a binary tree priority encoder requiring semi-custom design and configuration shift register and output serializer both requiring timing driven, automated, place and route design. All these blocks extensively communicate with each other and cannot be developed in isolation.

VI. Conclusion

The "Segmenting Independent Subchips for Resource Optimization" (SISRO) approach for creating edgeless ROICs allows the development of a new class of large area detectors without deadzones. It can be applied to both two tier 3D integrated as well as single tier 2D ROICs as shown by the two examples, which illustrate the process and demonstrate its advantages and versatility. It effectively exploits the repetitive nature of pixel detectors, by identifying a self-contained, independent subchip which can absorb all peripheral functions within the pixelated area, without growing the pixel size. Additionally, it eases some of the chip level constraints by scaling them to manageable smaller subchips. Small diameter TSV is the enabling technology utilized in these designs.

SISRO would benefit from pixel size scaling to the extent that the criteria of connection to the sensor (e.g. using DBI) and transfer of information to and from the backplane (e.g. PCB) is

achievable. Advanced techniques, such as edge computing for data reduction, or the integration of optical transceivers for higher data rates, can alleviate the congestion on the backplane by reducing the number of I/O required for a given frame rate.

For a two tier ROIC, the smallest pixel size is limited by the analog pixel layout in addition to the size and pitch of the TSV. Furthermore, the bonding interface pitch of the analog tier connection to the sensor would limit the pixel sizes to the order of 5 μm.

For single tier ROICs, the limiting factor for analog dominant designs would be the size and number of TSVs required for I/O pads and the size and pitch of I/O pads required for communication to the backplane.

The smaller features and enhanced performance offered by CMOS scaling will evidently benefit individual tiers, particularly digital. While 3D ROICs can consist of tiers of different process nodes, single tier ROICs are poised to benefit significantly from modern multi-platform CMOS processes, which on the same substrate offer transistors with different voltage ratings, optimized for digital or analog applications.

These detectors will enable a new class of time resolved experiments at X-ray photon sources, which require large imaging figure-of-merit. The thinning of ROICs and elimination of wire bonds can create compact large area detectors, meeting the stringent material budget requirements in detectors for high energy physics [35]. In astronomy, due to the small size of stellar images, stars can go undetected when they fall directly in gaps in detectors [36]. Hence gapless detectors will reduce the need to reposition and reacquire images to compensate for the gaps in the sensing areas. Furthermore, creating smaller independent subchips operating with reconfigurable readout techniques will enable regions of interest in large camera systems, a step towards implementing advanced imaging techniques such as foveation.

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REFERENCES

[1] Ch. Broennimann E. F. Eikenberry, B. Henrich, R. Horisberger, G. Huelsen, E. Pohl, B. Schmitt et al., *The PILATUS 1M detector*, *J. Synchrotron Rad.* **13** (2006) 120 - 130

[2] N. Tartoni et al., *Excalibur: a three million pixels photon counting area detector for coherent diffraction imaging based on the Medipix3 ASIC*, *IEEE Nucl. Sci. Symp. Conf. Rec.* (2012) 530.

[3] N. D. Parab, M. Hudspeth, B. Claus, Z. Guo, T. Sun, K. Fezzaa, and W. W. Chen. "Real-time visualization of dynamic particle contact failures." In *AIP Conference Proceedings*, vol. 1793, no. 1, p. 120006. AIP Publishing, 2017.

[4] K.S. Raines, S. Salha, R. L. Sandberg, H. Jiang, J. A. Rodríguez, B. P. Fahimian, H. C. Kapteyn, J. Du, and J. Miao. "Three-dimensional structure determination from a single view." *Nature* 463, no. 7278 (2010): 214.

[5] Lewellen, John, Kip Bishofberger, Nikolai Yampolsky, Frank Krawczyk, Leanne Duffy, Steven Russell, Bruce Carlsten, Quinn Marksteiner, Dinh Nguyen, and Richard Sheffield. "Status of the MaRIE X-FEL accelerator design." (2015): TUPMA026.

[6] G. Hülsen, Ch Broennimann, and E. F. Eikenberry. "Distortion calibration of the PILATUS 1M detector." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 548, no. 3 (2005): 540-554.

[7] S. Herrmann, S. Boutet, B. Duda, D. Fritz, G. Haller, P. Hart, R. Herbst, C. Kenney, H. Lemke, M. Messerschmidt, CSPAD-140k: a versatile detector for LCLS experiments. Nucl. Instrum. Methods Phys. Res. Sect. A: Accel. Spectrom. Detect. Assoc. Equip. **718**, 550–553 (2013)

[8] Ch. Brönnimann, and P. Trüb. "Hybrid pixel photon counting X-ray detectors for synchrotron radiation." *Synchrotron Light Sources and Free-Electron Lasers: Accelerator Physics, Instrumentation and Science Applications*(2014): 1-29.

[9] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos, and W. Wong. "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 581, no. 1-2 (2007): 485-494

[10] A. Mozzanica, A. Bergamaschi, M. Brueckner, S. Cartier, R. Dinapoli, D. Greiffenberg, J. Jungmann-Smith et al. "Characterization results of the JUNGFRAU full scale readout ASIC." *Journal of Instrumentation* 11, no. 02 (2016): C02047.

[11] G. Finger, R.J. Dorn, S. Eschbaumer, D. NB Hall, L. Mehrgan, M. Meyer, and J. Stegmeier. "Performance evaluation, readout modes, and calibration techniques of HgCdTe Hawaii-2RG mosaic arrays." In *High Energy, Optical, and Infrared Detectors for Astronomy III*, vol. 7021, p. 70210P. International Society for Optics and Photonics, 2008.

[12] P. Seller. "Technology needs for modular pixel detectors." *Solid-State Radiation Detectors,–Technology and Applications* (2017).

[13] M. Okihara *et al*., "Progress of FD-SOI technology for monolithic pixel detectors," *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)*, Anaheim, CA, 2012, pp. 471-474. doi: 10.1109/NSSMIC.2012.6551151

[14] T. Hatsui, M. Omodani, T. Kudo, K. Kobayashi, T. Imamura, T. Ohmoto, A. Iwata et al. "A direct-detection X-ray CMOS image sensor with 500 μm thick high resistivity silicon." In *Proc. Int. Image Sensor Workshop*, vol. 3, p. 4. 2013.

[15] R. Turchetta, N. Guerrini, and I. Sedgwick. "Large area CMOS image sensors." *Journal of Instrumentation* 6, no. 01 (2011): C01099.

[16] N. Guerrini, R. Turchetta, G. Van Hoften, R. Henderson, G. McMullan, and A. R. Faruqi. "A high frame rate, 16 million pixels, radiation hard CMOS sensor." *Journal of Instrumentation* 6, no. 03 (2011): C03003.

[17] X. Zhang, P. K. Jo, M. Zia, G. S. May and M. S. Bakir, "Heterogeneous Interconnect Stitching Technology With Compressible MicroInterconnects for Dense Multi-Die Integration," in *IEEE Electron Device Letters*, vol. 38, no. 2, pp. 255-257, Feb. 2017. doi: 10.1109/LED.2016.2643502

[18] P. Garrou, C. Bower, and P. Ramm, eds. *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits*. John Wiley & Sons, 2011.

[19] M. Campbell, J. Alozy, R. Ballabriga, E. Frojdh, E. Heijne, X. Llopart, T. Poikela, L. Tlustos, P. Valerio, and W. Wong. "Towards a new generation of pixel detector readout chips." *Journal of Instrumentation* 11, no. 01 (2016): C01007.

[20] M.C. Veale, et al. "Characterization of edgeless CdTe detectors for use in hard X-ray imaging applications." IEEE Transactions on Nuclear Science 59.4 (2012): 1536-1543.

[21] K. Kasinski, et al., "Development of a Four-Side Buttable X-Ray Detection Module With Low Dead Area Using the UFXC32k Chips With TSVs", IEEE Trans. on Nucl. Sci., vol. 64, no. 8, August, 2017, pp. 2433-2440

[22] P. Enquist, "High density direct bond interconnect (DBI) technology for three dimensional integrated circuit applications." *MRS Online Proceedings Library Archive* 970 (2006).

[23] L. Wang, G. Fountain, B. Lee, G. Gao, C. Uzoh, S. McGrath, P. Enquist, S. Arkalgud, and L. Mirkarimi. "Direct Bond Interconnect (DBI®) for fine-pitch bonding in 3D and 2.5 D integrated circuits." In *Microelectronics Symposium (Pan Pacific), 2017 Pan Pacific*, pp. 1-6. IEEE, 2017.

[24] G.W. Deptuch, G. Carini, P. Enquist, P. Gryboś, S. Holm, R. Lipton, P. Maj et al. "Fully 3-D integrated pixel detectors for X-rays." *IEEE Transactions on Electron Devices* 63, no. 1 (2016): 205-214.

[25] X. Llopart, "Towards a new generation of Medipix and Timepix ASICs" FEE 2018, May 21 – 25, 2016, Jouvence, Canada

[26] G.Deptuch. "Status of 3D integration ", FEE 2016, May 30 – June 3 2016, Krak w, Poland

[27] D. Lammers, "Heterogenous strategies gaining steam", 2018, https://blog.globalfoundries.com/heterogenous-strategy-gaining-steam/

[28] S. Chen, and M. Ker, "Investigation on seal-ring rules for IC product reliability in 0.25-μm CMOS technology." *Microelectronics Reliability* 45, no. 9-11 (2005): 1311-1316.

[29] Fahim, Farah, Grzegorz W. Deptuch, James R. Hoff, and Hooman Mohseni. "Design Methodology: Edgeless 3D ASICs with complex in-pixel processing for Pixel Detectors." In SPIE Nanoscience+ Engineering, pp. 95550M-95550M. International Society for Optics and Photonics, 2015.

[30] F. Fahim, S. Joshi, S. Ogrenci-Memik, H. Mohseni "A low power, high speed, bus arbitration technique for pixel detector readout", IEEE Trans. on VLSI, accepted for publication

[31] F. Fahim, G. Deptuch, S. Bianconi, S. Joshi, C. Rabinowitz, M. Rezai, H. Mohseni, et al. "Reconfigurable data readout of pixel detectors with automatic synchronization with Data Acquisition Systems, to be published

[32] F. Fahim "Edgeless large area ASIC." No. 15/214,758, Fermi National Accelerator Lab.(FNAL), Batavia, IL (United States), 2019.

[33] F. Fahim, G. W. Deptuch, P. Grybos, R. Szczygiel, P. Maj, P. Kmon, D. P. Siddons et al. "Edgeless large area camera system." No. 16/123,857, Fermi National Accelerator Lab.(FNAL), Batavia, IL (United States), 2018.

[34] F. Fahim, B.Cauble, A. Shenai, H. Mohseni. " Design Methodology Overview: ASICs with complex in-pixel processing for Pixel Detectors", to be published

[35] A. Tricomi, "SLHC: The LHC luminosity upgrade." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 596, no. 1 (2008): 43-47.

[36] P. Martinez, and A. Klotz. *A practical guide to CCD astronomy*. Vol. 8. Cambridge University Press, 1998