The ETROC Project: Precision Timing ASIC Development for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

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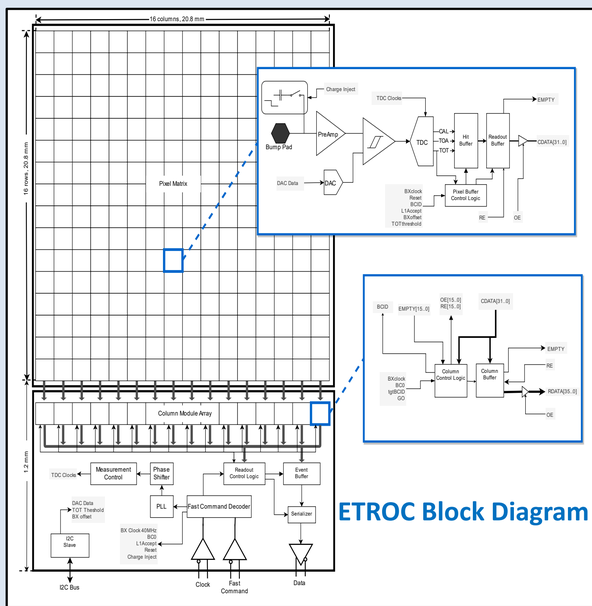


ETROC Block Diagram

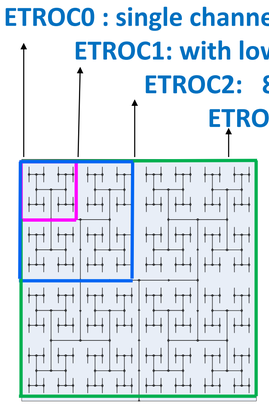
ABSTRACT

The **ETROC (Endcap Timing Readout Chip**) is being developed for the **LGAD-based CMS Endcap Timing Layer (ETL) at HL-LHC**. The ETL on each side of the interaction region will be instrumented with a two-disk system of MIP-sensitive LGAD silicon devices to be read out by ETROCs for precision timing measurement with down to 30 ps timing resolution. The ETROC is designed to handle a **16 x 16 pixel cell matrix**, with each pixel cell being **1.3 mm x 1.3 mm** to match the LGAD sensor pixel size. Approximately 15% of the sensors near the highest eta region will experience hadron fluence above 1e15 neq/cm^2 towards end of operation of HL-LHC, resulting in small signal amplitude with LGAD gain reduced to around 10. For this reason, the front-end design for preamplifier and discriminator has been specifically optimized for the reduced LGAD signals, with enough flexibilities to meet the ETL specific needs for time resolution, power budget and radiation profile.

The ETROC chip is implemented in **TSMC 65nm**. At the pixel level, each channel consists of a preamplifier, a discriminator, a TDC used for TOA (time of arrival) and TOT (time over threshold) measurements, and a memory for data storage and readout. The TOT is used for time-walk correction of the TOA measurement. The detailed hit information (TOA and TOT) from within each cell will be read out from a local circular buffer after each Level-1 Accept (about 1 MHz). In addition, a charge injection circuit is implemented to allow for testing and calibration. For more detailed monitoring of the signal pulses as radiation dose increases, waveform sampling circuits will be included in selected pixel cells. Additional peripheral circuits include a PLL, a phase shifter, an I2C slave, a fast control block, a serializer, and a data driver. The main design challenge is how to extract precision timing information from the small LGAD signals in the presence of high irradiation fluence, while keeping the power consumption low. The ETL design goal for the time resolution of 50 ps per hit is required in order to achieve a 35 ps arrival time measurement for a MIP particle, which has its track registered in two ETL disk layers. The LGAD contribution is known to be about 30 ps, this means that the jitter from the ETROC has to be kept below 40 ps.

ETROC DEVELOPMENT STAGES

ETROC0 : single channel with preamp + discriminator (Dec. 2018)
ETROC1: with low power TDC and 4x4 clock tree (Aug. 2019)
ETROC2: 8x8 and full functionality (Q1 2021)
ETROC3: 16x16 full size chip (Q1 2022)

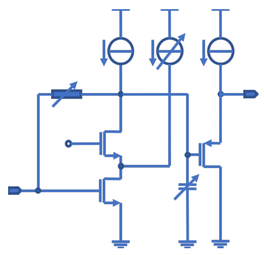


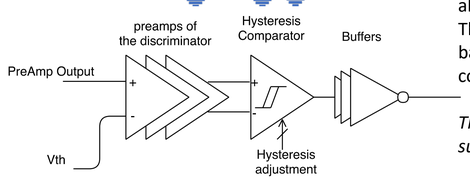
ETROC 16x16 clock H-tree

The challenge of designing the ASIC, while optimizing its performance and that of the sensor together as a unit, is approached in several design stages. The first stage has two components: 1) using test beam data taken with LGAD sensors being readout by an external preamplifier with its waveform recorded by an oscilloscope to study different timing measurement algorithms; and 2) using detailed LGAD simulation as input to simulate the behavior of various ASIC front-end designs. Much information can be extracted from the sampled waveforms of different sensors, with different irradiation levels, operated at different bias voltages. This shortens the development cycle for the ASIC.

Based on the design study results, the second stage is to design and develop a small scale prototype chip and, again using the LGAD simulation for input, to study the design performance with post-layout simulation. Subsequent stages involve the production of prototypes with increasingly more complex structure to test and further optimize the ASIC design. There are essentially three important areas we intend to focus on. The first is the analog front-end performance. This includes the preamplifier, the discriminator, and the TDC stage. The second is the precision clock distribution within the chip. The third is the evaluation of the radiation-hardness (TID, SEU) of the design. To effectively and efficiently meet these design challenges we have divided the prototyping phase into a series of ever more complex prototype chips named ETROC0 through ETROC3.

ETROC0: PREAMPLIFIER and DISCRIMINATOR

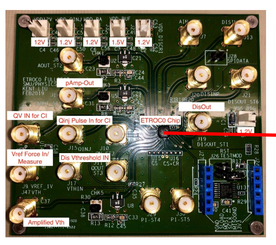


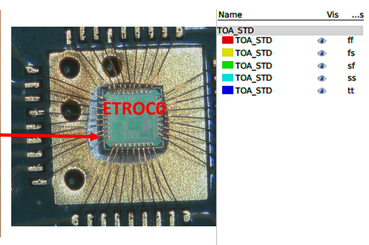


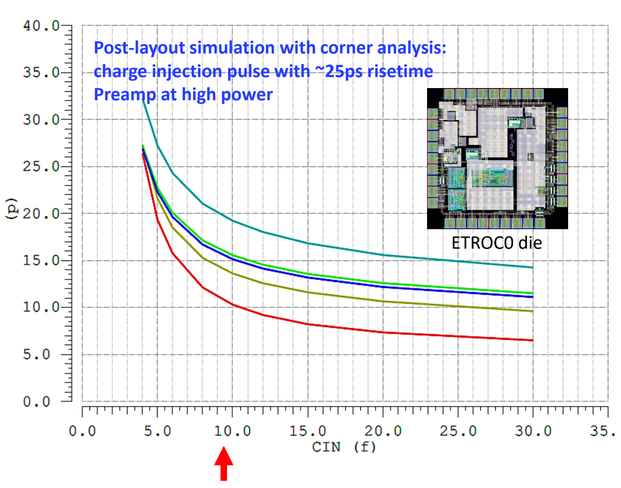
The goal of the ETROC0 mini-ASIC is to study and demonstrate the performance of the preamplifier and discriminator. The ETROC0 is a **single channel design** which consists of a preamplifier with integrated charge injection followed by a discriminator with a user programmable threshold controlled by an internal DAC.

The **preamplifier** has a two-stage design. A cascode amplifier with resistive feedback acts as the first stage, and a source follower as the second stage. The size of each transistor in the preamplifier has been optimized by using an LGAD simulation as the input signal. The design considers both leading and trailing edge to optimize the TOT measurement for the time-walk correction. The feedback resistance is programmable to allow adjustment of the fall time, while the bias current is also programmable to allow different trade-offs between power consumption and performance. The load capacitance of the first stage is also programmable to allow optimization of the bandwidth. The discriminator is optimized for the full chain for low signal size while keeping power consumption low.

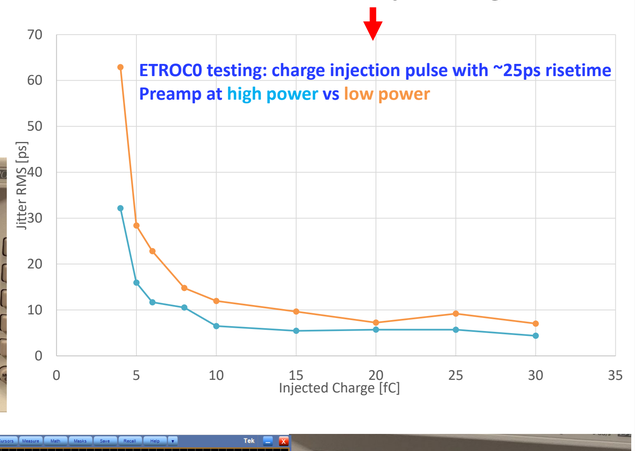
The front-end preamplifier and discriminator has been implemented in single channel ETROC0 and submitted in Dec. 2018. The testing of the ETROC0 has been on-going since April 2019.



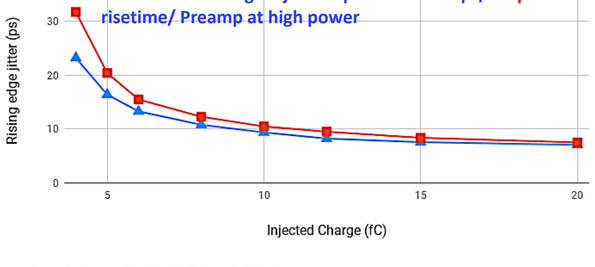




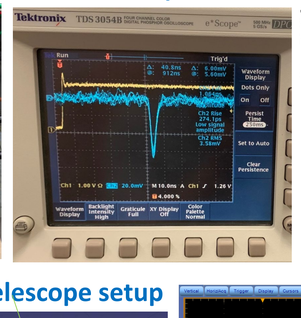
Simulation and Chip Testing



Injected Charge vs Jitter (High power, low gain) (Board-1)

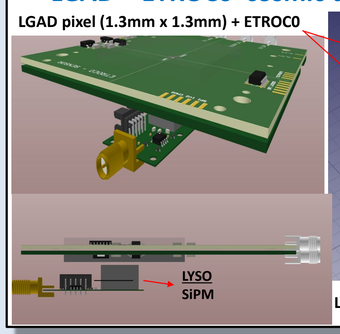


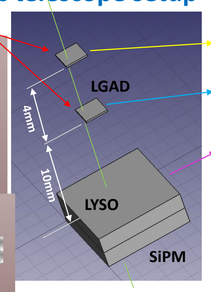
LGAD + ETROC0 1060nm laser test setup



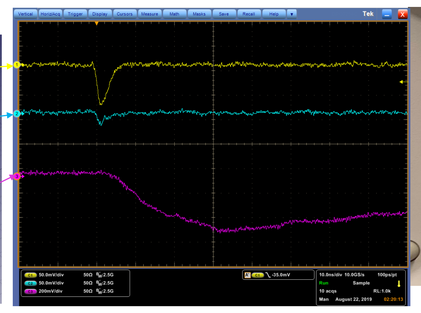
LGAD + ETROC0 cosmic telescope setup

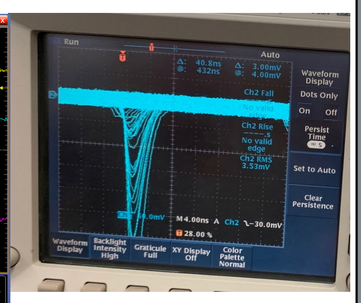
LGAD pixel (1.3mm x 1.3mm) + ETROC0





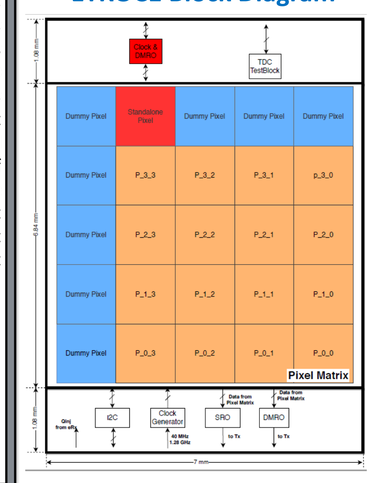
LYSO/SiPM to confirm cosmic





Preparation for beam test at Fermilab in Dec 2019

ETROC1 Block Diagram



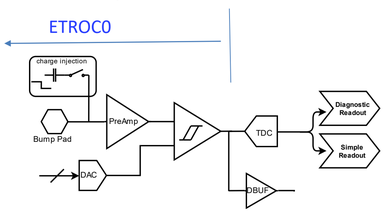
ETROC1: new TDC and 4x4 PIXELS

The goals of the **ETROC1** chip are to study the performance of the full front-end chain and a simple precision clock distribution scheme. The ETROC1 chip is a **4x4 pixel matrix** with each pixel consisting of a preamplifier, a discriminator, and a TDC stage used to measure TOA and TOT. The precision clock distribution scheme will use a simple H-tree structure, to provide clock for sixteen full front-end chains, and will allow us to compare the clock distribution performance with simulation. Lastly, the TDC output data will feed into an E-link output port which includes a high speed serializer. The ETROC1 design has been submitted in August 2019, using the same preamplifier and discriminator design as in ETROC0 after successful testing of ETROC0.

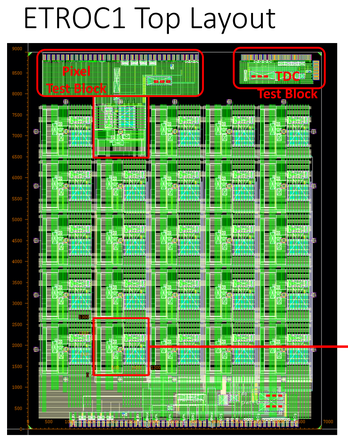
The new **TDC** takes as input the discriminator output and records the TOA and TOT for a fixed discriminator threshold. The specification for TOA and TOT TDC bin size is not to exceed 30 ps and 100 ps, respectively. To allow improvements in particle identification in heavy ion collision events, the TDC measurement time window is extended to 6.25 ns. The TDC stage design has been optimized for low power operation in such a way that one simple delay line with uncontrolled delay cells is used to measure both TOA and TOT at the same time. This is made possible by using an in-situ delay cell self-calibration technique, that is, to use two consecutive rising clock edges to record two time stamps for each hit. The time difference between the two time stamps is the known clock period, and this fact can be used for delay cell calibration for every hit.

Effective clock distribution is a challenge and care must be taken in minimizing clock skew and jitter. For ETROC we have adopted the most common and conservative clock distribution scheme, known as **H-tree.**

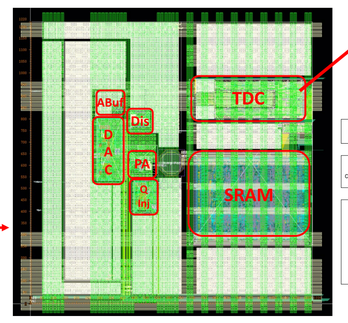
ETROC0

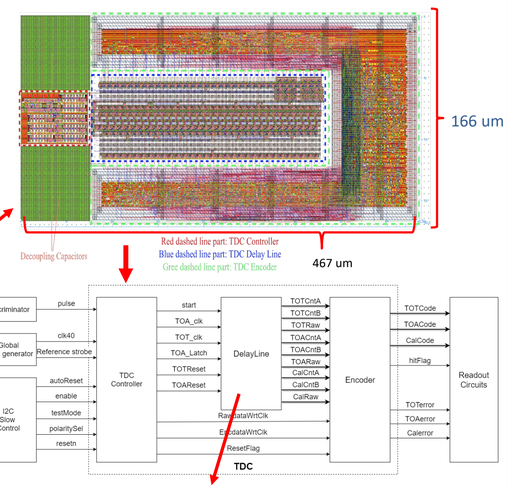


ETROC1 Top Layout



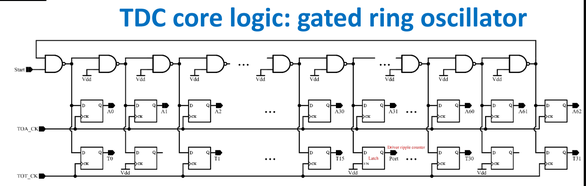
ETROC1 Single Pixel Layout





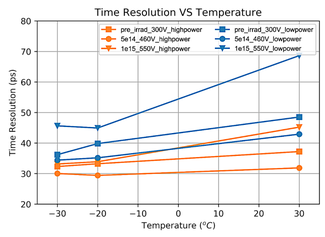
TDC core logic: gated ring oscillator

A 63-tap gated ring oscillator (GRO) is used for the core TDC delay line, with uniform and uncontrolled ***NAND*** gate delay cells and ~20 ps latency per cell. The load of all the nodes are well matched, and the period of oscillator is about 2*63*20 ps = 2.52 ns. This is a simple and fast GRO structure with no latency control logic, no DLL used. Instead, real time calibration will be used because each hit will be measured twice using two consecutive clocks. One delay line is used for both TOA/TOT measurements. TOA bin size is one cell delay latency (~20 ps) and TOT bin size is twice the cell delay latency (~40 ps). Dynamic range is configurable and up to 12.5 ns for both TOT and TOA measurement. TOA DNL estimated to be ± 0.15 LSB and INL is about ±0.3 LSB.



No hit, not action design. Low standby power and easy to extend the dynamic range by using a counter. The typical power consumption of TDC is ~75 uW for 1% occupancy rate according to post layout simulation.

LGAD + ETROC EXPECTED SYSTEM PERFORMANCE



The ETL design goal for the time resolution is 50 ps per hit, in order to achieve a 35 ps arrival time measurement for a MIP track with an ETL hit in each of the two-disk layers. The LGAD contribution is known to be about 30 ps, this means that the jitter from the ETROC has to be kept below 40 ps. This should be achieved with reasonable power consumption and signal efficiency, and maintained even after irradiation. The jitter contributions and ETROC power consumption are summarized below. Time resolution as a function of temperature in post-layout simulation using LGAD simulation as inputs, with the nominal process, with default and also a higher power preamplifier setting. The parasitic components of the preamplifier and the discriminator are included, assuming 20 ps bin sizes for both of the TDCs.

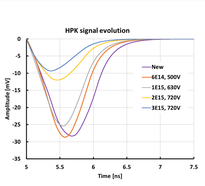
Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

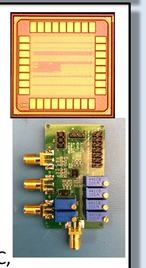
LGAD+ preamp/discriminator + TDC bin	35 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	41 ps
Per track (2 hits) total time resolution	29 ps

5e14 with preamp low power, OR, 1e15 with preamp high power

WAVEFORM SAMPLING

For the robust long term operation of the ETL it will be important to monitor signal waveforms to detect variations from the increasing radiation dose. Recorded waveforms can be used to optimize thresholds and bias voltages in order to try to maintain the target performance. Since implementing waveform sampling for all channels is not possible, the plan is to only implement it for two pixels per chip, based on the assumption that nearby sensor pixels will behave and age in a similar way. Beam test data waveform studies have shown that a waveform sampling speed between 2 and 3.2 GS/s is sufficient for this purpose.





This can be implemented using an existing 12bit 320MS/s ADC design block in 65nm. The 10bit (Effective Number of Bits (ENOB)) 320MS/s ADC is the critical building block for waveform sampler for ETROC. ETROC can use a 2.56 GS/s 12-bit wave sampler which interleaves 8 channels of the 320MS/s 12-bit single-channel ADC. A single-channel 320MS/s 12-bit ADC prototype chip, implemented in 65nm CMOS process for ETROC, has been designed and received in Aug 2019. The silicon area of the 2.56GS/s waveform sampling circuit is expected to be less than 1 mm x 1 mm.

ACKNOWLEDGEMENT

We use several design blocks (I2C slave, ESD-pad, eRx and the phase-shifter) developed through common projects at CERN, and the CERN ELT library in the ETROC1 development. We would like to thank the designers of these design blocks, especially Syzmon Kulis and Paulo Moreira (both from CERN) for the support. This poster has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.