Characterization of LVDS Transmission Data Integrity

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FERMILAB-POSTER-19-088-PPD

Introduction

Differential Signaling, or LVDS, is a physical layer interface that allows for high-speed transmission over short distances, and is an efficient alternative to single-ended signaling. Differential signals are robust to common-mode noise, as the equal and opposite signals both incur identical disturbances. LVDS circuits also utilize a constant current, which allows for lower power consumption. LVDS links will be implemented in future neutrino experiments, so developing and testing a proper design is necessary for incoming projects. This presentation will detail the results of the testing of an LVDS implementation that was designed by the ASIC department at Fermilab.

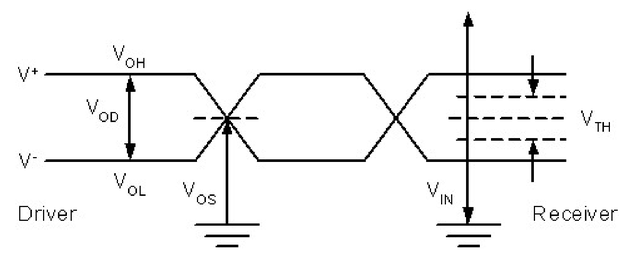
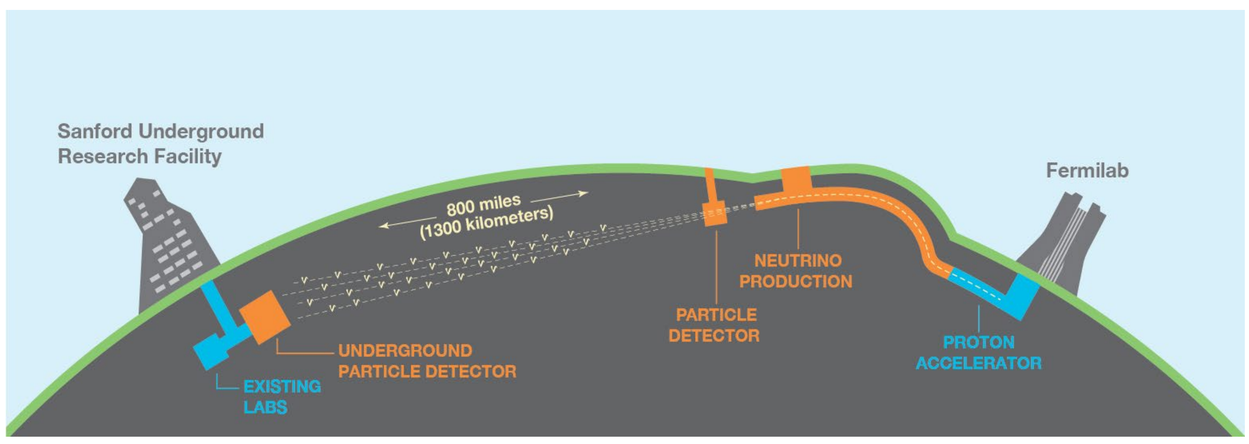


Diagram of LVDS driver and receiver[2]

Purpose

- DUNE or the Deep Underground Neutrino Experiment, is projected to be in operation by 2026 at the Sanford Research Facility in South Dakota. There will be the home of the largest detector of its type to ever be built. 70,000 tons of liquid argon will be used within the detector, and the readout electronics will need to be able to withstand 87 kelvin for the lifetime of the experiment [3].
- Fermilab's LVDS designs utilize longer length transistors to increase the lifetime of the electronics in cryogenic conditions [1].
- LVDS is robust towards noise, so such a design is beneficial for accurate data acquisition in DUNE.

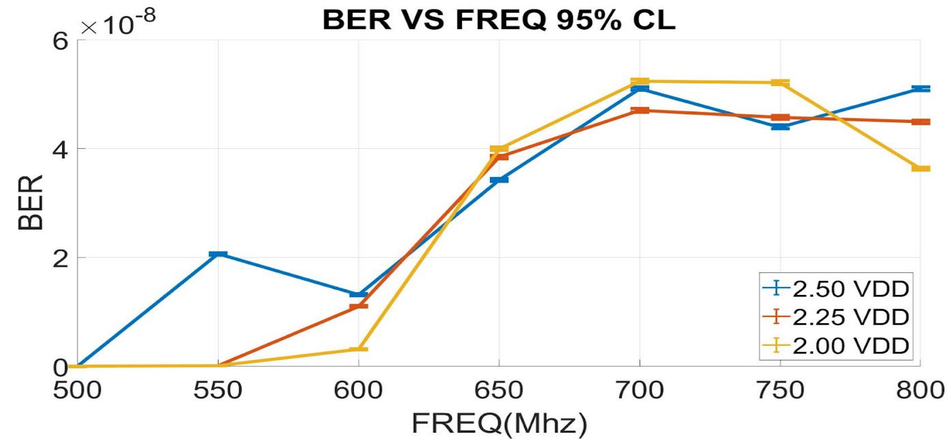


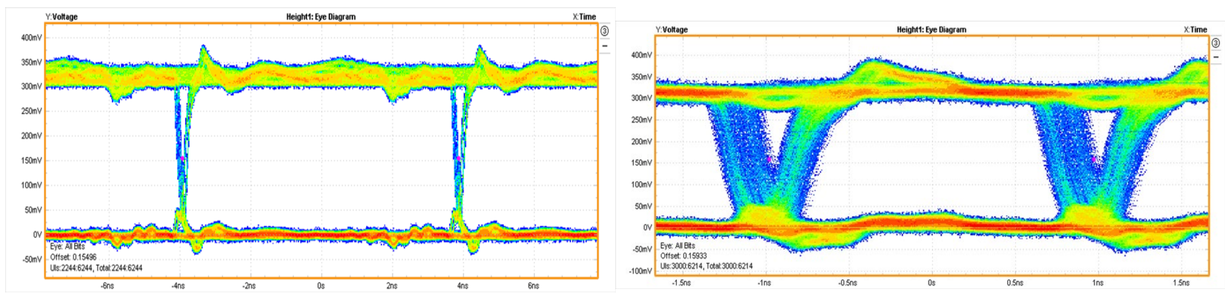
Pictured above is a visual representation of how DUNE will be implemented [3].

Testing Methods

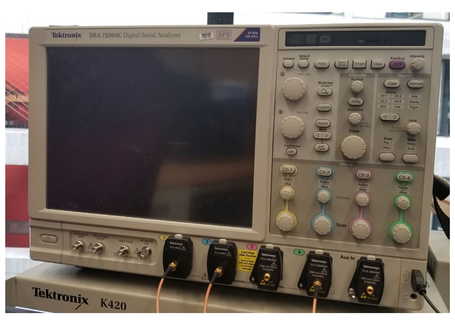
- BER stands for Bit Error Ratio, and is a common figure of merit for signal integrity. BER is the ratio of bits received in error over the total bits received
- The LVDS test board was connected to a signal generator and analyzer so that BER could be measured for multiple frequencies with the same number of transmitted bits. A Pseudo-random bit sequence was used for the testing.

- As expected, BER showed an upwards trend with frequency.
- Lowering the voltage from the nominal 2.5 V to 2.0 V did not increase the BER significantly.
- Eye diagrams measured on an oscilloscope show that the LVDS test board had strong signal transmission capabilities at 128 Mbps and 512 Mbps.





Top: BER of the LVDS Tx + Rx chain for different frequencies and supply voltages.
Bottom: eye diagrams at 128 Mbps (left) and 512 Mbps (right).



Pictured above: Tektronix GigaBERT signal analyzer, generator, and digital serial analyzer

Conclusions

The LVDS test board displayed promising figures in pertinence to data transmission. At frequencies below 500 Mbps, no measurable error could be detected in the signal analyzer, even after multiple hours of testing. At the nominal frequency of 128 Mbps, the eye was wide open with minimal signs of jitter, which meets the specifications for DUNE with ample margin.

References

Hoff, J. R., et al. "Cryogenic Lifetime Studies of 130 Nm and 65 Nm NMOS Transistors for High-Energy Physics Experiments." *IEEE* , 3 June 2015.[1]
"Parameters of a Differential Signal." *Www.ni.com*, Texas Instruments, 24 May 2019, www.ni.com/en-us/innovations/white-papers/06/understanding-lvds-for-digital-test-systems.html.[2]
"The Deep Underground Neutrino Experiment (DUNE)." *Www.fnal.gov*, 2019, www.fnal.gov/pub/science/lbnf-dune/index.html.[3]