Defense Innovation Technology Challenge: Tampa, FL, US

Fermi National Accelerator Laboratory

FASPAX / ASIC Development

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Company Information:

- Fermi National Accelerator Laboratory
- Founded in 1967
- Located in Batavia, Illinois (Greater Chicago Area)
- www.fnal.gov
- ~1,700 Employees
- Mission: High Energy Physics Research (Discovery Science)

Typical sensors have:

- Large areas with sensing gaps from assembling reticle size ROICs with wire-bonding on one edge
- Low full-frame readout speeds due to the bottleneck of moving data to the periphery

Technology Information:

Large Area pixel detectors - Example: FASPAX

- ASIC has been fabricated and tested, with V1.0b in development
- TRL 4
- High Dynamic Range, High Burst Frame Rate
- Zero-suppressed data for low occupancy & extremely fast acquisition
- User programmability to change between different operating modes in small regions of interest
- Simultaneous multi-functional regions to enable foveation or edge detection

- New regime in area detectors:
X-ray camera beyond the dynamic range of a CCD, sensitivity of a photon counting detector, and:
 - un-matched burst image rate (~ 13 MHz),
 - large, fully active (seamless) area (15×15 cm²),
 - small pixel size (100×100 μ m²) for 2.2M pixels
- Enabler of science for studies of irreversible processes, time-resolved or high flux applications and high speed imaging (DCS)
- Approach uses 3D integrated technology to provide seamless, wafer-scale detector; interposer adapts sensor pixel to ASIC pitch; ASICs in SiGe process, bump-bonded to interposer; 500 μ m thick Si X-ray detector
- New front-end concept: single - 10^5 photon per image capability in small pixel footprint

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FASPAX
sensors!

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ASTRONOMY

NIGHT VISION

SYNCHROTRON
BEAMLINES

MEDICAL IMAGING

DEFENSE
SYSTEMS

FOVEATION

ATOMIC SCALE
PHENOMENA

LOW
OCCUPANCY

DEFENSE INNOVATION

TECHNOLOGY ACCELERATION CHALLENGES

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	VIPRAM	VIPIC	FLORA	FASPAX
Functionality	Content Addressable Memory w Digital Processor	Analog + High-speed Digital Readout	MAPS Sensor, Analog, 8-10b ADC per Pixel	Bipolar Transistor for current splitting, large dynamic range w analog readout
Technology	2-tier TSV Daisy Chains	130nm CMOS	ROIC tier 130nm CMOS w Si sensor	.13 μ m BICMOS +sensor: Si or CdTe
Application	Real-time Pattern Recognition	Photon counting with zero suppressed readout	High-speed Imaging, Hard X-ray	Camera for APS, Hard X-ray

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Thank You!

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