The phase-1 upgrade of the CMS pixel detector

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***Abstract*—The pixel detector of the CMS experiment will be upgraded during the extended end of year shutdown during winter 2016/2017. The upgraded detector will operate at full efficiency at an instantaneous luminosity of $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with increased detector acceptance and additional redundancy for the tracking, while at the same time reducing the material budget.**

The design and technological choices will be reviewed, and the status of the construction of the detector and the performance of its components as measured in system tests are discussed.

I. Introduction

THE innermost detector of the CMS experiment [1] is a pixel tracker [2] arranged in three barrel layers (BPIX) and two forward disks in each endcap (FPIX). The original CMS detector was designed for the nominal instantaneous LHC luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Already in the current running, a small decrease of pixel hit efficiency in the first layer of the BPIX has been observed, as shown in Figure 1. Under the conditions expected in the coming years, which will see an increase of a factor two of the instantaneous luminosity, the CMS pixel detector will see a dynamic inefficiency caused by data losses due to buffer overflows.

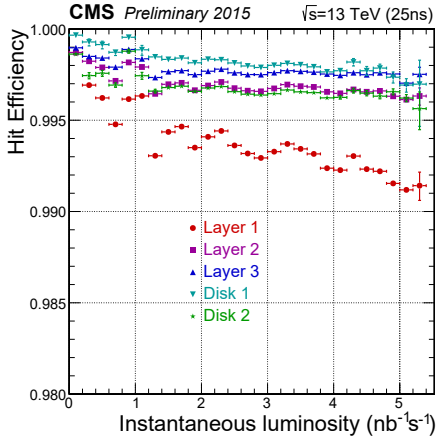

Fig. 1: Hit efficiency vs. instantaneous luminosity for pixel barrel layers and forward disks. The innermost layer is most affected by dynamic inefficiency which is due to data losses due to the limited buffer size.

For this reason the CMS Collaboration has been building a replacement pixel detector [3], which is scheduled for installation in an extended end-of-year shutdown during winter 2016/2017. This "phase-1" upgrade of the CMS pixel detector has been designed to overcome these inefficiencies for instantaneous luminosities up to $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ using a new read-out chip (ROC) with larger buffers and increased data transmission bandwidth, as well as modified powering and read-out schemes. Also, an additional layer of pixels both in the barrel and endcap region is introduced resulting in a higher track hit coverage for absolute pseudorapitities ($|\eta|$) smaller than 2.5. The innermost layer will be closer to the interaction point (IP), 2.9 cm instead of 4.4 cm. Due to a new mechanical support, including a new CO_2 cooling system, and the relocation of the on-detector service electronics further away from the IP, the passive material inside the tracking volume is largely reduced. A comparative sketch of the current and upgraded pixel detectors is shown in Figure 2.

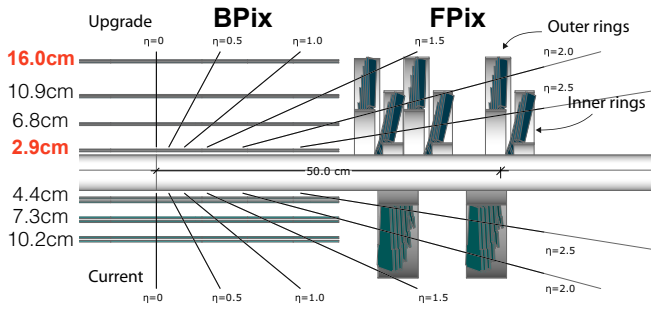

Fig. 2: Comparison of the layout between the upgraded (top) and current (bottom) pixel detector.

This note is organized as follows: first, the design changes of the pixel modules and their testing are discussed in Section II. Then, the new cooling and mechanic support are reviewed in Section III. In Section IV, the service electronics and data acquisition system are discussed. Finally, the construction and testing status, as well as plans for installation are outlined in Section V.

II. Pixel module design and testing

The pixel modules have a similar design as in the current detector: the active material is an n^+-in-n silicon sensor that comprises 66,560 pixels, each with a size of $100 \times 150\,\mu\mathrm{m}^2$. These pixels are read out by 16 ROCs that are bump-bonded to the sensor. The ROC is based on the psi46 chip [4], [5], currently used in the detector: the 250 nm CMOS technology is used with zero-suppressed read-out based on the column-drain architecture.

Thin flexible printed circuits, so-called high density interconnects (HDIs), are glued to the sensor, and connected via wire-bonds to the ROCs. The data from and to the ROCs are routed by the HDI to token bit manager (TBM) ASICs. These TBMs control the read-out of the ROCs and also format the read-out data. In the case of modules located in the first layer

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Manuscript sent November 30, 2016. This version was made public under http://dx.doi.org/10.1109/NSSMIC.2016.8069719.

This document was prepared by CMS collaboration using the resources of the Fermi National Accelerator Laboratory (Fermilab), a U.S. Department of Energy, Office of Science, HEP User Facility. Fermilab is managed by Fermi Research Alliance, LLC (FRA), acting under Contract No. DE-AC02-07CH11359.

of the BPIX, two TBMs are used. The HDIs are also wire-bonded to the sensor to provide bias voltage.

While the pixel modules layout hasn't changed, there are important improvements, especially to the ROC: the current 40 MHz analog read-out has been replaced by a 160 Mbits/s digital read-out by adding an 8-bit ADC. Also, the hit and timestamp buffer sizes have been increased from 32 to 80 and 12 to 24, respectively. These two changes allow to overcome the inefficiencies, mentioned in Section I, expected for the present pixel detector. Further improvements to the comparator, chip-internal cross-talk and transistors allow to reduce the operational threshold from 3,500 e^- to 1,800 e^-. Also, the radiation hardness of the chip is increased.

The ROC for pixel modules in the first layer has to be modified further due to the high expected hit rates of about 600 MHz/cm^2. The read-out of this chip uses a dynamic cluster column drain [6] where clusters of 2×2 pixels are transferred to the buffer instead of individual ones.

The pixel module is the smallest unit in the detector, and undergoes rigorous testing. All modules are thermally stressed and then evaluated in a series of calibration tests to measure the amount of defects, such as poor bump-bonds, and the quality of the read-out, such as the noise of a pixel unit. The leakage current as a function of the bias voltage is measured, and the read-out under high hit rates is tested using an X-ray source. The combination of the test results are used to grade the quality of the pixel modules, and poor modules are discarded. In Figure 3, examples of calibration tests are shown.

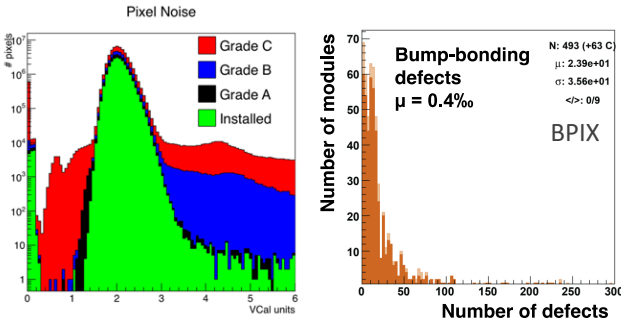

Fig. 3: Left: Measurement of the noise in ADC units of test voltage (V_{cal}) setting the calibration signal amplitude for FPIX modules. Grade A and B modules are of detector-quality, with A being the best quality, and B with only minor deficiencies, while grade C modules are discarded due to low quality, right: Number of defective bump-bonds for layer 2-4 BPIX modules.

All modules needed for the construction of the pixel detector have been assembled and tested good. The assembly and testing is in its final phase for obtaining more spare modules.

III. Mechanical support and the CO_2 cooling system

The mechanical support structure of the pixel detector, as sketched in Figure 4, has to satisfy three important aspects: holding the pixel modules, provide them with cooling, while being light-weight in order to have only a small amount of passive material.

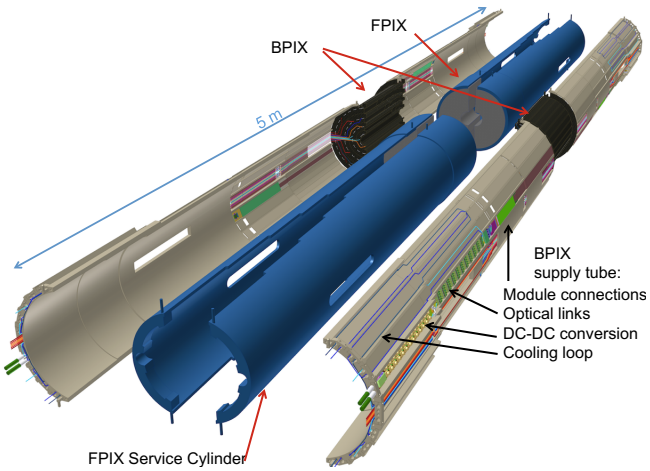

Fig. 4: Exploded view of the upgraded pixel detector. The figure shows the positions of the different partitions FPIX and BPIX and their respective service cylinders.

For the BPIX, the pixel module support is built using a high thermal conductive carbon fiber and Airex foam compound except for the most outer layer, that is made only out of carbon fiber. This structure is organized in half-shells, and each half-shell is supported by an endflange. The endflange of the most outer layer carries the weight of the BPIX detector. The service electronics, described in the next section, is supported by a half-cylinder (HC), that is made out of carbon fiber close to the IP, and a carbon fiber / Airex foam compound further away from the IP.

The FPIX modules are mounted on blades made out of thermal pyrolitic graphite. These blades are supported by two carbon-fiber half-rings on either side. This support structure comes in two flavours: a "half-disk" with a smaller radius and closer to the beam line, the inner ring, and a half-disk with a larger radius, the outer ring. This can be also appreciated in Figure 2. The disks are supported at the end of another HC made out of carbon fiber. This HC also supports the service electronics for the FPIX modules.

A significant difference in the mechanical design of the phase-1 and the current detector is that the service electronics hosted in both the BPIX and FPIX HCs have been moved further away from the IP, thus greatly reducing the passive material within the tracking volume, as shown in Fig. 5.

The most important change in the mechanical design concerns the cooling of the pixel modules and service electronics. The current cooling system using mono-phase liquid C_6F_{14} will be replaced with a system using bi-phase CO_2 as coolant. The heat produced inside the detector will be absorbed as latent heat of the CO_2. The cooling tubes guiding the CO_2 are made out of stainless steel with an inner diameter of 1.6 mm and a wall thickness between 50 and 100 μm, thus significantly smaller than the tubing of the present detector. The CO_2 will be highly pressurized at 20 bar. The nominal operation temperature will be -20 °C. The cooling tubes are embedded in the mechanical support. An example for embedded cooling lines in an FPIX inner ring is shown in Figure 6. The cooling will also be routed through the section of the service

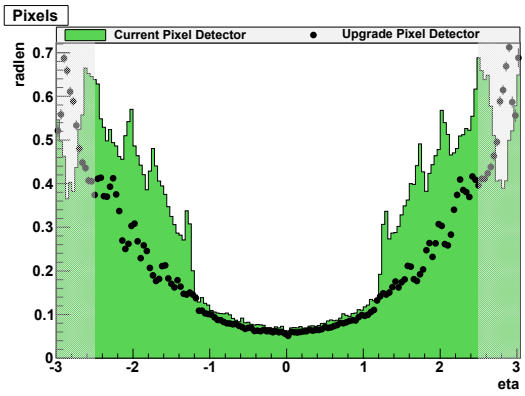

Fig. 5: The amount of material in the pixel detector shown in units of radiation length for the current pixel detector (green histogram), and the phase-1 upgraded detector (black points). The shaded region at high $|\eta|$ is outside the region for track reconstruction.

electronics. The coolant will first pass the service electronics, before it is routed along the pixel modules, and returned through the service electronics section.

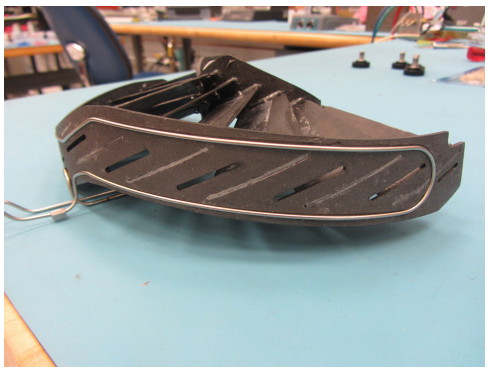

Fig. 6: An FPIX inner ring with embedded stainless steel cooling tubing. A production ring will have an additional carbon skin on the outside, covering the currently exposed tubing.

IV. Service Electronics and Data Acquisition System

Inside the pixel detector, there are two classes of service electronics: power related electronics, and electronics assisting the control and read-out of the pixel modules.

A. Power system

The upgraded phase-1 detector has almost twice as many read-out channels as the present detector, leading to an increase of the power losses by almost a factor four. Therefore, the power supplies outside the detector in their present configuration are not able to adequately provide power to the pixel detector, as the resistive power loss would be too high. This is avoided by providing lower currents at a higher voltage to the pixel detector, and use newly introduced DC-DC converters [7] to transform this input to the necessary voltages needed by the pixel modules. The DC-DC converters, located in the service HCs of the detector, receive a voltage of 10 V and convert it to 3.0 and 2.4 V for the digital and analog circuits of the pixel modules, respectively.

As mentioned in the previous section, the DC-DC converters are cooled with the same coolant as used for the pixel modules. In fact, the heat produced in the DC-DC conversion is used to preheat the CO_2 and force it into the bi-phase state.

B. Control and read-out electronics

One of the main tasks of the on-detector control and read-out electronics is to receive control, clock, and trigger signals, convert them into the data format of the pixel modules' TBMs, and then correctly distribute them to the various modules. These signals are transmitted to the detector using optical fibers. Digital opto-hybrids [8] convert the light into electrical signals. Auxilary chips on printed circuit boards subsequently encode and convert those signals, which are then distributed to each individual pixel module.

In addition, the (electric) signals from the pixel modules are guided to so-called pixel opto-hybrids [9]. These host linear laser drivers, level-translator chips, and transmitter optical subassemblies that convert the electric signal to light, which is sent out of the detector in optical fibers. In case of the FPIX and the third- and fourth-layer BPIX modules, one fiber connection per module is used, while modules in the first and second BPIX layer use four and two fibers to transmit the pixel read-out data, respectively.

C. Data acquisition system

The backend of the read-out and control system [10] will be based on the μTCA standard, allowing for high-speed signal links up to 10 Gbits/s. Two types of boards are used: so-called front-end controllers (FECs) which distribute clock, trigger, and control signals, and front-end drivers (FEDs) which read out the optically converted signals from the pixel modules. Both types are FC7 boards that can house one or two FPGA mezzanine cards (FMCs). The FEC board hosts up to two FMCs with eight SFPs each, and can send control and clock signals to up to eight digital opto-hybrids. The FEC boards come in two flavours: one controlling the calibration of the pixel modules, the other controlling the service electronics. The two versions only differ by their firmware. The FED board hosts one FMC with two FITEL twelve channel receivers and one SFP+, and can read out the data of up to 24 pixel channels. The full phase-1 pixel detector will use 108 FEDs to read out the pixel data, 16 FECs for controlling signal, clock, and trigger distribution to the pixel modules, and 2 FECs for controlling the service electronics. They are housed in twelve μTCA crates.

D. Pilot test system

The full read-out chain, from the pixel modules up to the μTCA system, is being tested inside the CMS experiment, using a pilot system [11] that has been installed in 2014.

This system uses prototypes of 8 FPIX modules, read-out and control boards, and DC-DC converter boards. In the beginning the pixel modules were read out with a data acquisition system similar to the one currently used, and later with the new μTCA system. As such, the pilot system has provided vital information for the final design of the electronics, and is still used to validate the latest developments of the FEC and FED firmwares.

V. Status of production and testing, and plans for installation

The production of all individual elements needed for the assembly of the phase-1 detector has been completed. The pixel modules of the BPIX are being mounted onto their mechanical support. This is expected to be finished by the end of November 2016. For FPIX, all modules have been successfully mounted on the support rings. Also, the production of the service HCs has been completed for both BPIX and FPIX. The integration of the service electronics into the HCs for BPIX is ongoing, while it is completed for FPIX. The BPIX detector will be assembled and tested at the Paul Scherrer Institut in Switzerland. The fully assembled detector is expected to be transported to CERN in January 2017, where a final check-out will be performed. The FPIX HCs were assembled and tested at its assembly center at the Fermi National Accelerator Laboratory in the USA. The tests used the final read-out system chain. All four HCs and all support rings with mounted pixel modules were shipped separately to CERN, where the support rings were re-inserted into the HCs. All FPIX HCs undergo a complete calibration both at the Tracker Integration Facility and/or Point-5, the location of the CMS detector and service cavern. These tests will be done at the final operating temperature.

In order to install the phase-1 pixel detector, the current one will be extracted in mid-January 2017. Also service elements need to be replaced, such as the cooling lines for the new CO_2 cooling. The new phase-1 detector will then be inserted end of February/beginning of March 2017. The final commissioning and initial alignment will need both cosmic data and the very first proton-proton collision data.

VI. Summary

The phase-1 CMS pixel upgrade will replace the current CMS pixel detector during the extended shutdown in the beginning of 2017. The upgraded detector will be able to reconstruct tracks with high efficiency for the high LHC instantaneous luminosities expected in the coming years. At the same time, the number of read-out channels, and the overall hit coverage of tracks is increased, and the amount of passive material in the tracking volume is reduced. The construction and assembly of the upgraded detector is almost complete, and the commissioning of it is ongoing.

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