

# Modeling and analysis of hybrid pixel detector deficiencies for scientific applications

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## ABSTRACT

Semiconductor hybrid pixel detectors often consist of a pixellated sensor layer bump bonded to a matching pixelated readout integrated circuit (ROIC). The sensor can range from high resistivity Si to III-V materials, whereas a Si CMOS process is typically used to manufacture the ROIC. Independent, device physics and electronic design automation (EDA) tools are used to determine sensor characteristics and verify functional performance of ROICs respectively with significantly different solvers. Some physics solvers provide the capability of transferring data to the EDA tool. However, single pixel transient simulations are either not feasible due to convergence difficulties or are prohibitively long. A simplified sensor model, which includes a current pulse in parallel with detector equivalent capacitor, is often used; even then, spice type top-level (entire array) simulations range from days to weeks.

In order to analyze detector deficiencies for a particular scientific application, accurately defined transient behavioral models of all the functional blocks are required. Furthermore, various simulations, such as transient, noise, Monte Carlo, inter-pixel effects, etc. of the entire array need to be performed within a reasonable time frame without trading off accuracy. The sensor and the analog front-end can be modeling using a real number modeling language, as complex mathematical functions or detailed data can be saved to text files, for further top-level digital simulations. Parasitically aware digital timing is extracted in a standard delay format (sdf) from the pixel digital back-end layout as well as the periphery of the ROIC. For any given input, detector level worst-case and best-case simulations are performed using a Verilog simulation environment to determine the output. Each top-level transient simulation takes no more than 10-15 minutes. The impact of changing key parameters such as sensor Poissonian shot noise, analog front-end bandwidth, jitter due to clock distribution etc. can be accurately analyzed to determine ROIC architectural viability and bottlenecks. Hence the impact of the detector parameters on the scientific application can be studied.

**Keywords:** pixel detectors, modelling, readout ASIC, parasitic extraction, simulations.

## 1. INTRODUCTION

Highly segmented, position sensitive hybrid pixel detectors are used in a variety of applications including high-energy physics, x-ray imaging, infra-red imaging etc. [1]. Semiconductor hybrid pixel detectors often consist of a pixellated sensing layer (sensor) bump-bonded to a matching pixelated processing layer readout integrated circuit (ROIC). The sensor layer converts the incoming electromagnetic radiation to charge and the ROIC converts the charge to either analog or digital data. The ROIC's have complex in-pixel processing capabilities contained within either a single or multiple tiers. Additionally, several functional blocks are typically present in the periphery including bandgap references for analog biasing, buffers, further digital processing, LVDS drivers and receivers, etc. as shown in Figure 1. Multi-tier ROICs, are 3D integrated to create edgeless detectors – i.e. sensors and ROICs with no active area lost to peripheries. These require the peripheral functions to be placed within the area occupied by the array; hence the digital pixel is no longer an indivisible unit, as shown in **Error! Reference source not found.**

A wide variety of sensors are available from planar silicon to III-V or II-VI material composites with a range of pixel and array sizes. Increasingly smaller pixel sizes with large area arrays are being manufactured yielding reliable and consistent pixel performance [2]. These sensors require low power, complex per-pixel processing, customized for particular characteristics and applications.

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A ROIC pixel analog front-end or analog pixel often consists of a charge sensitive amplifier (CSA) with detector leakage current compensation, a shaping amplifier (band-pass filter), and at least one comparator. The ROIC pixel digital back-ends or digital pixel can contain a variety of functions including analog to digital converters (ADC), time to digital converters (TDC), Digital to analog converters (DAC) for trimming comparator offsets, counters, sparsified readout logic, configuration registers, data readout shift registers etc. [3]. Transistor counts often exceed 1000 in a small pixel area typically tens of microns, and therefore require a compact layout, often hand crafted with the use of custom digital cells. Moreover, these customized digital back-ends often contain asynchronous logic, have to be parasitically aware and do not have any pixel level timing information available. However the pixel still needs to cope with the stringent high-speed data readout requirements of the peripheral logic.

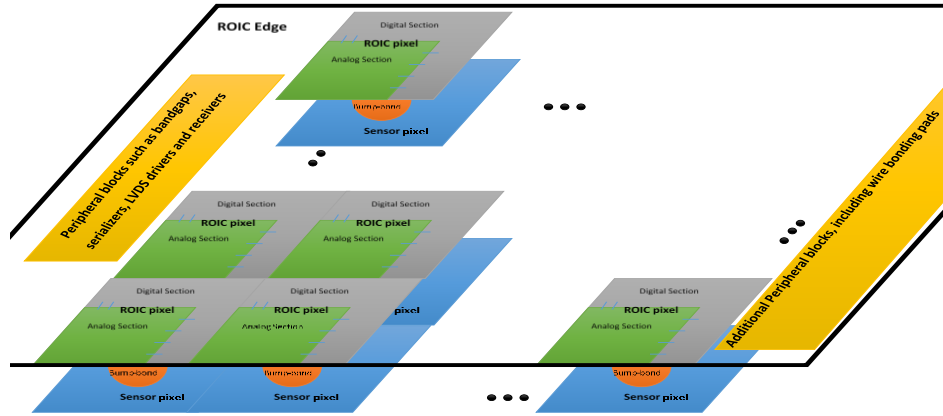


Figure 1. Hybrid pixel detector

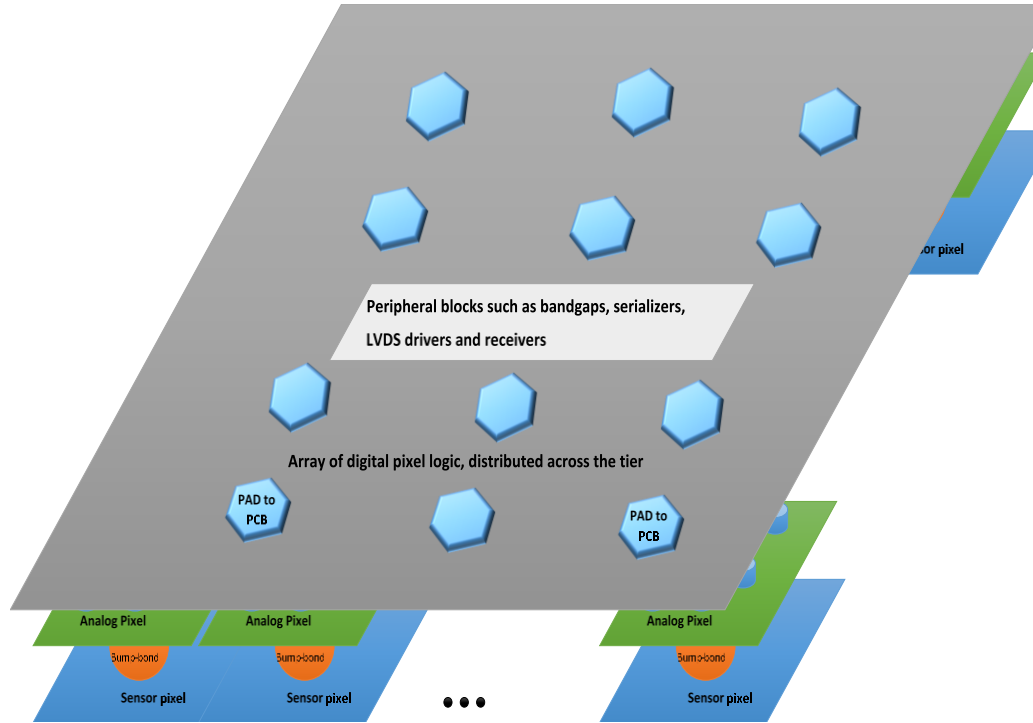


Figure 2. 3D edgeless hybrid pixel detector

Simulation and analysis of the detector system allows inefficiencies and performance limitations to be identified. Furthermore, the impact of the detector parameters on the scientific application can be studied. A full detector model with

different parts interfaced to each other needs to be practical for verification of the interconnections and bottlenecks between the various sections. At the same time it needs to allow for detailed theoretical performance analysis.

## 2. SENSOR AND ANALOG PIXEL MODELLING

Detailed simulations of both the sensor and the ROIC require specialized tools, which often take copious amounts of time to yield detailed performance metrics. These simulations are initially performed at a single pixel level. They can take a few hours to a few weeks to run and are extremely important for successful detector development. Since the tools used for the two developments often use different criteria for analysis, the simulations performed do not have a direct correspondence. E.g. sensor simulations could be studying charge transport characteristics with various type of incoming radiation, on the other hand, the analog pixel simulation is studying the transient behavior of the circuitry. The output of the sensor simulation does not have a one-to-one correspondence with the input of the analog simulation.

Furthermore, although single pixel behavior is studied in great details, due to time and resource constraints top-level detector simulations are never performed.

### Sensor Pixel simulations and modeling

Physics solvers such as Comsol Multiphysics are often used to perform detailed sensor simulations. This allows for a thorough understanding and analysis of the sensor. The results from these simulations need to be translated to a transient response of the sensor, as most detector performance analysis is time-based - e.g. light sensitivity for an IR sensor, corresponds to the number of photons generated, which then can be modeled as the charge generated by the detector as a function of position and time. Furthermore, a silicon detector behavior exposed to a Cd source varies from that exposed to a Fe source depending on its thickness and depletion voltage. Hence the same detector can have various models based on the scientific application. A simplified sensor model, which includes a current pulse in parallel with detector equivalent capacitor, is often used, but this can be further augmented based on sensor leakage currents and shot noise. Detailed, single pixel file based models can also be developed, corresponding to a time-based piecewise linear response of the detector to various stimuli. Multiple files corresponding to detector sub-poissonian noise behavior and sensor leakage currents also need to be added. Several, typical, best-case and worst-case transient performance files need to be established. These files can then be used as inputs to the analog simulation.

### Analog pixel spice based simulations and file based model

Spice level simulations are carried out to verify the analog pixel performance across process manufacturing corners and mismatches in a pixel. These detailed simulations are essential to determine the circuit performance. Detailed Monte Carlo simulations need to be performed to calculate the mean and the standard deviation of the analog outputs, which are inputs to the digital pixel. A comparator, window discriminator or an ADC is often the interface between the analog and digital functions in a pixel. The output of the interface block is critical to allow further multi-pixel simulations. The result of a Monte Carlo simulation of a comparator is shown in figure, this will be used to determine the typical, best-case and worst-case performance of the pixel based on the mean and standard deviation. Multiple files corresponding to each of the sensor output files need to be recorded. Unlike the sensor output files these files are relatively simple and require only the time of transition of the comparator output (interface block output), corresponding to the time the sensor received the incoming signal.

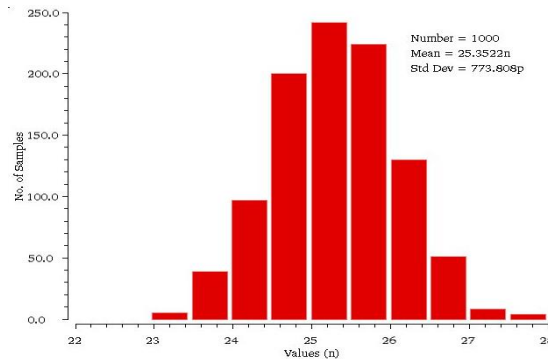


Figure 3 Monte Carlo analysis of a comparator output

### Detector and analog pixel wreal based model

An alternate theoretical modeling technique is to use a mathematical real number modeling language (such as Cadence wreal), to model the sensor and the analog front-end of the pixel as complex mathematical functions. A characteristic equation with appropriate time scales is used to define the block [3]. The inputs and outputs of these blocks are wreal, then model parameters are defined, additionally an initial\_block is defined for variable initialization and other preliminary one time calculations. This is followed by the setup of an always procedural block, triggered off the events which change the output of the model. The model calculations are within this always block.

## 3. DIGITAL FUNCTIONAL & POST LAYOUT PARASITIC MODEL

So far, multiple simulation output files have been created for various stimuli. These files correspond to a detailed analysis of single pixels. A few cross-talk scenarios can also be identified and simulated to study coupling between pixels but a full top-level multi-pixel simulation of the sensor and analog front-end is laborious and unnecessary. However once we are in the digital domain, logical simulations can have relatively fast turn around and it is best to perform top-level simulations in the digital domain.

### Digital pixel and peripheral functional model

The Verilog description of the entire digital section can be used as its functional model. The analog function is partially modeled in Verilog, by emulating the comparator output and forcing the digital input to “1” at a well-defined time. E.g. in Table 1, the output of two comparators (CompH and CompL) is listed for various pixels and multiple hits at different time. The test bench can be programmed to identify ‘-1’, which indicates that the output never changed. The user has control over the definition of the time, which is extracted for the application based best-case and worst-case analog performance. The time definition model can be as simple as a single pixel value or can be more complicated to include several values which are a result of different sources of jitter including but not limited to the detector shot noise, analog front-end noise across temperature, process and mismatch corners etc.

Table 1. Text file format for the data source generator

Row no.	Col no.	CompL 0→1	CompH 0→1	CompH 1→0	CompL 1→0	Time Frame	Comment
4	4	300	-1	-1	310	1	Valid data
4	4	420	423	426	427	1	Should not be counted
3	40	320	-1	-1	340	1	Valid data
5	20	600	-1	-1	615	1	Valid data

### Digital post-layout parasitic model

Generating timing for custom hand-crafted digital cells requires the development of a timing library with the use of a library characterization tool. The digital pixel needs to pass cell level layout vs. schematic (LVS) check followed by a detailed parasitic .spef file generation at various temperature and process corners using a parasitic extraction tool. The format of output .spef file is then modified to be compatible with a digital floorplan, routing & timing analysis tool (such as Cadence Encounter). The .spef file needs to be imported in timing mode, and used to generate timing libraries (.lib) and standard delay format (.sdf) files for further assembly and verification simulations. Functional verification can be performed in a Verilog simulator using the .sdf files created in the previous step. This step is critical for the iterative flow of the design. Digital high-speed data transfer blocks are routed and timed by the fully automated tool and also generate .sdf files for simulations.

## 4. TOP LEVEL SIMULATIONS

Developing a test bench and using the top-level digital Verilog functional model and/or post layout parasitic model are used to perform various top-level simulations. The output of the analog-to-digital interface block is an input to the digital pixel matrix. Depending on the application, per-pixel sensor and analog response to the incoming electromagnetic radiation can be consolidated in a text file. Using this file for top-level simulation the detector behavior can be analyzed for various scenarios within a relatively short time. These top-level simulations take between 10-15 minutes each. A data source generator could use multiple input files for the same application but corresponding to different sensor and analog front-end performance such as noise, mismatch, process variations etc. to create a range of input files to the digital section. The data required for such analysis was intensively processed and recorded using detailed spice simulations. The output of the digital section is often a bit-stream. Data packets need to be reconstructed from this bit stream. A monitor compares the input and output data to check for accuracy. It checks for delays in the data and inconsistencies in the output stream such as incorrect sequences etc. It also checks if any data is missing (data loss) or if other additional spurious data exists (false positives). Errors often help identify bottlenecks in the data transfer or improper interconnections between functional blocks. Figure 4 shows the flowchart of the modeling methodology developed.

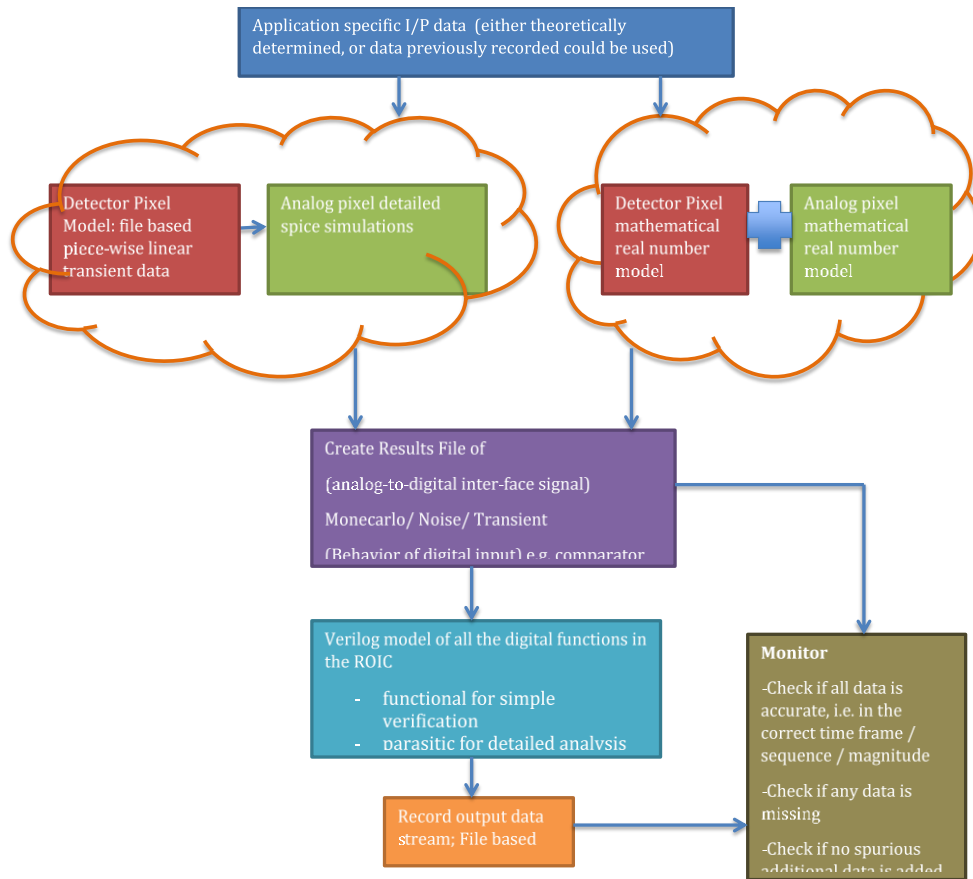


Figure 4. Flowchart of the modeling methodology

## 5. CONCLUSIONS

Physics solvers are used to determine sensor characteristics and transient piece-wise linear data of the output is recorded. This data is used as stimuli to the analog front-end circuitry. Detailed spice level simulations are performed to develop typical, best-case and worst-case timing for the analog-to-digital interface blocks. Alternately, a mathematical real number modeling language can be used to model the sensor and the analog front-end. Verilog description of the digital backend is used to perform top-level, multi-pixel simulations in the digital domain. The parasitic information of custom digital layouts

is extracted using a parasitic extraction tool and subsequently using a place and route tool in the timing mode, timing and delay files are created. This technique allows top-level parasitic simulations, which are useful for determining architectural performance metrics as well as verifying behavior at interfaces of large functional blocks. Depending on the application, per-pixel sensor and analog response to the incoming electromagnetic radiation can be consolidated in a text file. Using this file for top-level simulation the detector behavior can be analyzed for various scenarios within a relatively short time. These top-level simulations take between 10-15 minutes and are useful to study detector inefficiencies for scientific applications.

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