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Characterization of Silicon Detector Readout Electronics

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ABSTRACT: Configuration and calibration of the front-end electronics typical of many silicon detector configurations were investigated in a lab activity based on a pair of strip sensors interfaced with FSSR2 read-out chips and an FPGA. This simple hardware configuration, originally developed for a telescope at the Fermilab Test Beam Facility, was used to measure thresholds and noise on individual readout channels and to study the influence that different configurations of the front-end electronics had on the observed levels of noise in the system. An understanding of the calibration and operation of this small detector system provided an opportunity to explore the architecture of larger systems such as those currently in use at LHC experiments.

KEYWORDS: Silicon strip detectors; Front-end electronics; Noise; FSSR2.

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1. Introduction

Silicon detectors have been used as elements of tracking detectors since the 1970's but their use in colliding beam experiments was only made possibly in conjunction with the development of custom readout ASIC's [1]. Today, silicon detectors are ubiquitous in the tracking systems of almost all high energy collider experiments and although typical numbers of channels now exceed 50×10^6[2, 3], the main interfaces to the front-end readout are similar to those used in much smaller systems. The operation of a small scale silicon detector system, originally designed for test beam instrumentation, provides a useful way to investigate the procedures needed to configure, calibrate and read out these and similar systems. The exercises carried out in this lab explore the procedures used to characterize the noise performance of the front-end electronics in this small system, and the results illustrate general principles that can be applied to other silicon detector systems.

2. Hardware

The physical hardware used in this laboratory exercise, shown in Figure 1, reads out a pair of strip sensors that are mounted on the same mechanical support used at the Fermilab test beam facility. The sensors have implanted strips with a pitch of 30 μm but alternate between those that are read out and those that are left floating. This reduces the channel count, while still maintaining good spatial resolution for ionization that induces signals on multiple adjacent strips. Each sensor has 639 strips that are read out using five FSSR2 ASICs[4, 5] that are wire-bonded to pads on a printed circuit board. The printed circuit board not only provides the electrical connections between the readout chips and a connector, but also provides the mechanical support for the sensor so that the whole assembly can be mounted as an autonomous module on the mechanical support structure.

The FSSR2 chip was designed using a 0.25 μm CMOS process to provide a self-triggered readout architecture. A 3-bit ADC on each channel is implemented by means of 8 discriminators

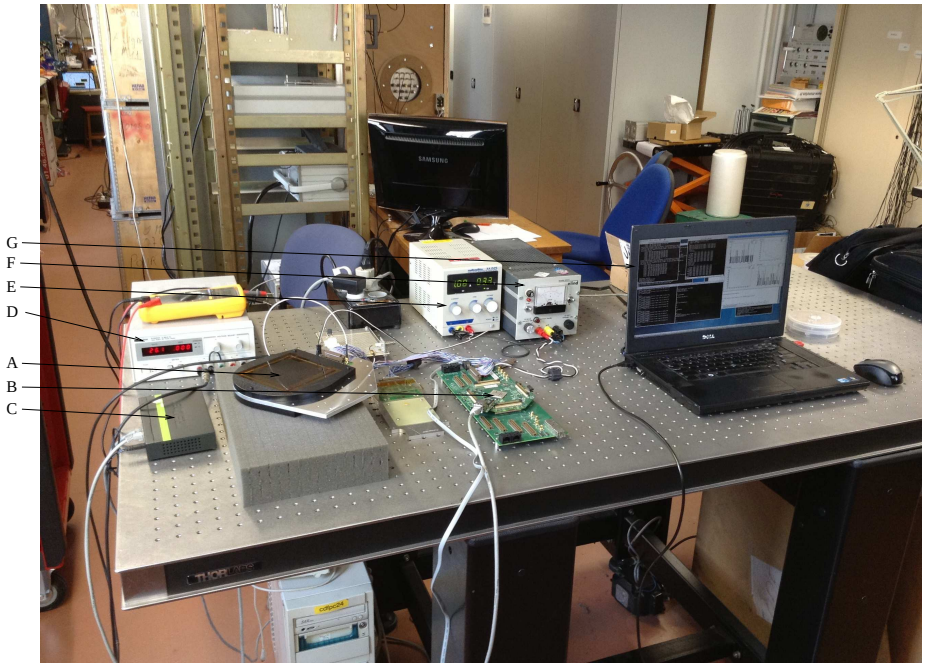

Figure 1. Experimental setup for reading out the silicon strip detector planes (A). Data from the readout chips is processed by firmware operating in the FPGA (B) which transfers data via 1 Gb Ethernet switch (C) to a host computer (G). Sensor bias is provided by power supply (D) while low voltage for the readout chips and FPGA are provided by power supplies (E,F).

that are normally configured to provide monotonically increasing thresholds using 8-bit DACs. The lowest threshold provides zero suppression which optimizes the use of the available readout bandwidth. A clock signal is used to advance an 8-bit bunch counter that needs to be synchronized across all readout chips in the system. Input signals with amplitudes exceeding the lowest discriminator threshold are tagged with the current bunch counter which forms part of the readout data word along with the channel number and 3-bit ADC data. This data is buffered internally and read out over a serial interface.

All digital interfaces to the readout chips are compatible with 2.5 volt LVDS, and interface directly with a Virtex-4 FPGA, by means of a multi-pair cable. In this setup, the FPGA is part of the CAPTAN system [6], developed at Fermilab for general purpose data acquisition system development, but the readout and calibration of the system is not constrained to this specific architecture. Interfaces between the FPGA and a host computer include a 1 GbE network adapter and a low speed serial port which allows one to interact via a command line interface with an embedded MicroBlaze processor core[7] which has been synthesized into the design downloaded into the FPGA.

The architecture of the readout logic is organized into independent firmware blocks that can be configured by means of memory-mapped registers in the 32-bit address space of the embedded processor. These registers are read and written using either the command-line interface or by means of a custom protocol in which sequences of read/write operations are sent via UDP packets over the network interface. Raw data from the readout chips is buffered and formatted into 32-bit

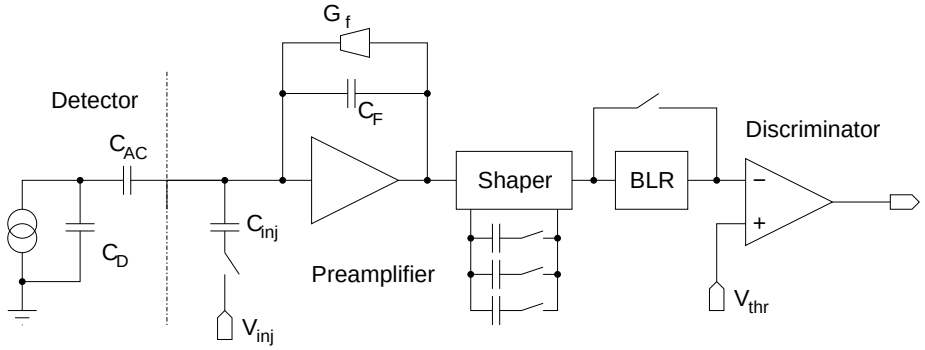

Figure 2. Equivalent detector, charge injection and preamplifer circuits which subsequently drive the configurable shaper/integrator, baseline restorer and discriminator. There is an additional gain factor of 10 between the preamplifier and the output of the shaper. Only one of 8 discriminators is shown for simplicity.

words streamed over the network, but for many of the calibration procedures this is unnecessary. Instead, it is sufficient to provide digital logic that simply counts the number of times a signal above threshold is detected on a given channel in a particular time interval, with the final values made available via the memory mapped register interface.

3. Front-end Electronics

The FSSR2 readout chip, shown schematically in Figure 2, was designed to interface with capacitively coupled strip sensors. A preamplifier integrates the induced current by means of feedback capacitance C_F which is discharged by the transconductance G_f. A programmable shaper circuit modifies the bandwidth of the signal, which can be selected to improve the signal-to-noise ratio at the expense of lower readout rate capability. A optional baseline restorer circuit can be enabled to reduce biases in charge and timing measurements for high rate applications.

The readout chips are configured by programming several DAC's to generate internal voltage references and by enabling the digital hit processing logic circuits. The interface to these circuits is made using the internal register space of the readout chip which is accessed using a relatively slow serial interface. Serial data words are shifted into the command decoder logic on each rising edge of a clock signal and are decoded into address and data fields as well as a command field to specify the type of operation (*eg.* read/write) that is to be performed. In this way, the internal bias voltages, including a set of 8-bit discriminator thresholds, are programmed. Other registers configure specific discrete parameters, such as the selection of low-gain or high-gain operation of the entire chip, disabling individual channels, or enabling the charge injection circuit on individual channels. Finally, setting bits in certain register allows the internal logic circuits to process hit data and to transmit it via high speed serial links. When configured in this way, charged particles passing through a biased sensor will result in the readout of digitized signals, but the characterization of several properties of the readout chip itself are more conveniently performed by injecting a known quantity of charge into the front-end preamplifier circuits of selected channels.

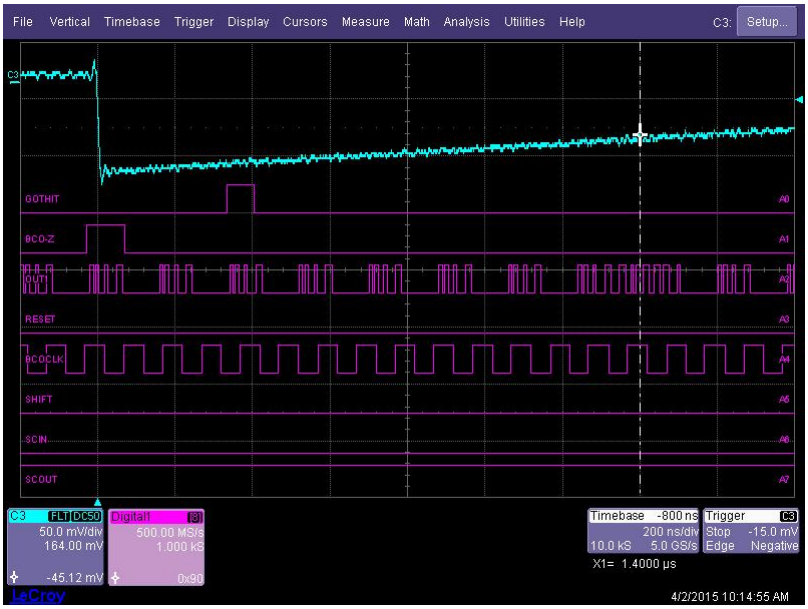

Figure 3. Injected voltage step (C1) timed to coincide with zero in the low 8-bits of the bunch counter (BCO-Z). The injected charge causes the discriminator on the selected channel to fire, generating a fast trigger output (GOTHIT) followed by readout of the hit data (OUT1) approximately 1.4 μs after the trigger. The bunch counter clock (BCOCLK) provides the time stamp with which to tag the data.

4. Calibration Using Charge Injection

The correspondence between discriminator thresholds and an absolute measure of input signal charge is established by injecting a known amount of charge into a selected channel and determining whether the resulting signal was above the discriminator threshold. The equivalent charge injection circuit, which is typical of many strip and pixel readout chip designs, is shown in Figure 2. In this case, the capacitance $C_{\rm inj}$ is designed to have a value of approximately 40 fF, and a voltage step applied to $V_{\rm inj}$ will inject a charge $Q = C_{\rm inj}V_{\rm inj}$ into the preamplifier of a selected channel. Even if $C_{\rm inj}$ is not known precisely, process variations across the readout chip are generally small enough that an almost identical charge will be injected into any given channel. This knowledge alone is sufficient to perform a relative calibration of individual channels.

The voltage step applied to $V_{\rm inj}$ is provided by a 500 MSPS DAC with an arbitrary waveform generated using the same FPGA used to control and read out the FSSR2 chips. Figure 3 shows the states of several logic signals received from the FSSR2 chip when triggered on the falling edge of the externally generated pulse. The measured amplitude of this pulse for a known DAC setting determines a scale factor used to convert DAC counts to voltage and when combined with the effective input capacitance, will yield the nominal injected charge. For this hardware configuration, the DAC value is related to the nominal injected charge by multiplying it by the factor 56.3 electrons.

Figure 4 shows results that are typical for a charge injection calibration on a single channel of an FSSR2 readout chip which has not been wire-bonded to a sensor. For each of the discriminator threshold settings, the fraction of pulses producing hits that are read out in the data stream is described by a step function convoluted with a Gaussian noise distribution. Thus, the measured

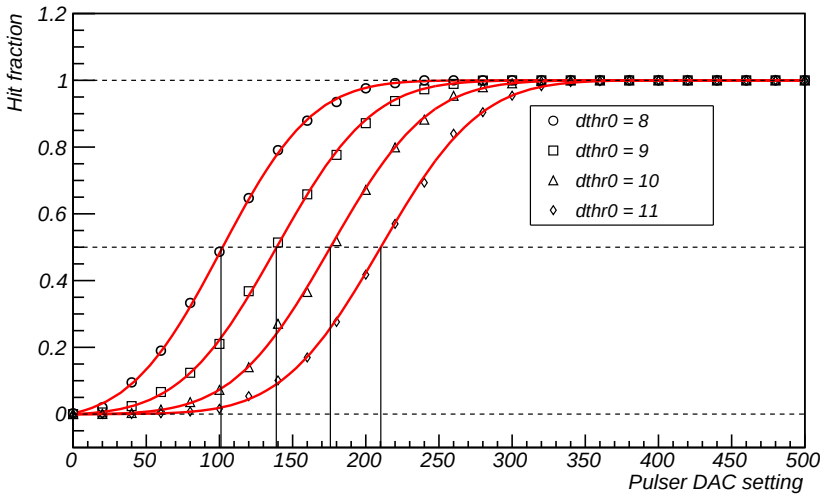

Figure 4. Fraction of injected pulses resulting in the readout of data plotted as a function of the charge injection DAC setting, for three different discriminator thresholds. In this case, the FSSR2 chip was configured for high gain, 65 ns shaping time, with the BLR enabled.

fraction is fitted using an error function:

$$f(V) = \frac{1}{2}\left(1 + \mathrm{Erf}\left(\frac{V-\mu}{\sigma\sqrt{2}}\right)\right) \tag{4.1}$$

in which μ represents the threshold and σ the RMS of the noise distribution. Because of its shape, the parametrization of this data is frequently referred to as an "S-curve". Figure 5 shows the mean μ, measured in terms of the DAC setting, plotted as a function of the discriminator threshold for two different gain settings. The dependence is seen to be linear and the x-intercept defines the discriminator threshold offset that must be subtracted when relating thresholds to absolute signal amplitudes. On the FSSR2 chip, a single register defines the discriminator threshold for all 128 channels but on more recently developed readout chips, including the PSI46 chip used in CMS and the FE-I4B chip used in ATLAS, each channel has an associated register that can be programmed so as to minimize differences in the response of all channels.

5. Noise Studies

In Equation 4.1, σ represents the RMS noise that is present when scanning the DAC across the corresponding discriminator threshold. The noise that is present in any measurement is an important characteristic of the readout system because it can limit the precision of hit position measurements that are based on the ADC weighted mean of adjacent hit channels. The intrinsic level of noise is influenced by the capacitive feedback in the preamplifier circuit, with subsequent gain stages amplifying the noise already present at their inputs. The shaper circuit effectively filters low- and high-frequency components of the signal, reducing the integrated noise at the expense of increasing the width of pulses being processed. In high rate environments, long pulses could overlap resulting in efficiency losses or biased ADC measurements. The baseline restorer circuit mitigates these

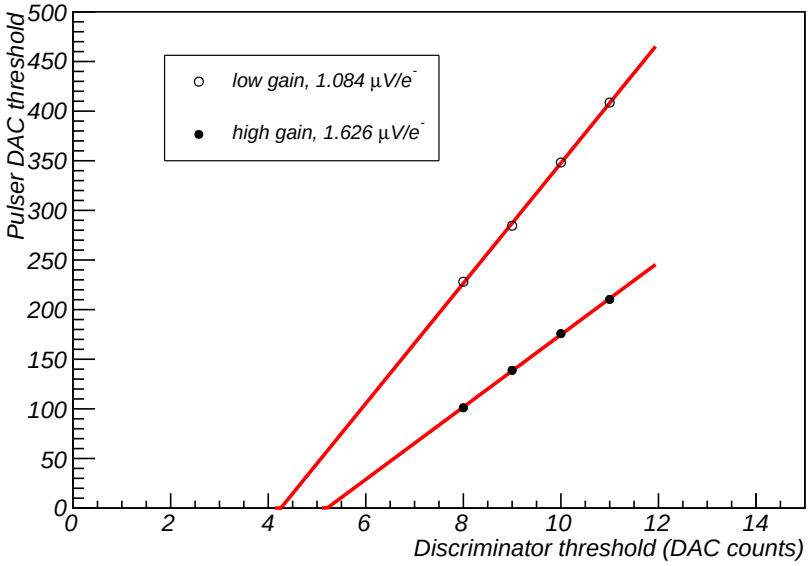

Figure 5. Mean DAC setting corresponding to different discriminator thresholds for low- and high-gain configurations. This data corresponds to 65 ns shaping time with the BLR enabled.

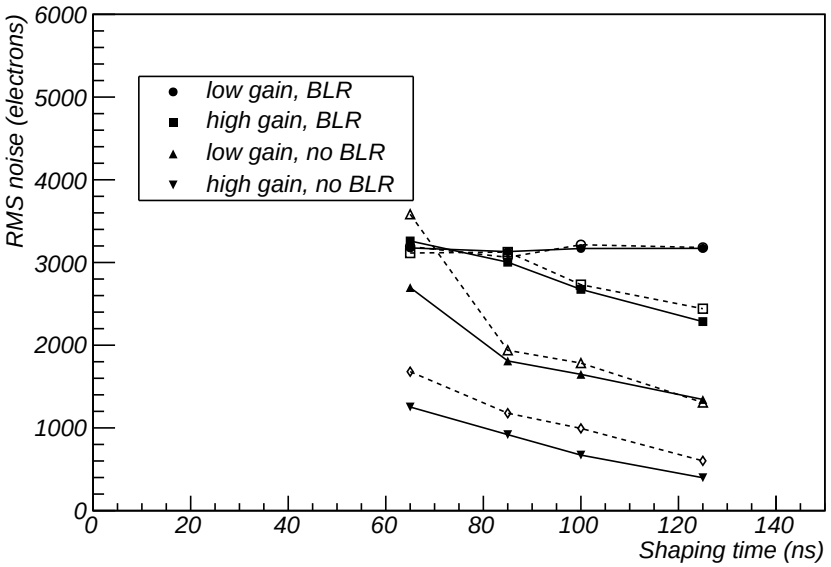

Figure 6. RMS noise as a function of shaping time. Solid and dashed lines are for discriminator thresholds of 12 and 13 DAC counts, respectively.

problems to some extent but also increases the overall level of noise present at the input to the discriminator.

Figure 6 shows the measured RMS noise for the four different shaping time constants for each combination of gain and BLR settings. The general trend of decreasing noise with increasing shap-

ing time is apparent although long shaping times would not necessarily provide optimal operating conditions in a high rate environment. The dynamic input capacitance of the preamplifier, C, is proportional to the feedback capacitance, C_f, while the gain is inversely proportional to $1/C_f$. Voltage noise typically scales as[8]

$$e_n^2 \sim C^2/T_S \tag{5.1}$$

where T_S is the shaping time, which explains the lower RMS noise observed for the high-gain setting with longer shaping times. The statistical interpretation of these noise figures should include the additional gain factor of 10 between the output of the preamplifier and the shaper. The latter circuits do contribute to the overall noise, but primarily amplify the noise already present in the preamplifier.

A silicon strip sensor adds approximately 15-20 pF of input capacitance to the front-end electronics in addition to the parasitic capacitance introduced by the pitch adapter. This naturally increases the level of noise that is present in a real detector system, but can be compared to the intrinsic performance described above. A specific comparison can be made using the high-gain setting with the BLR disabled, for which we observe an RMS noise of 18,000 electrons with 65 ns shaping time, which is reduced to approximately 4000 electrons with 125 ns shaping time. In a low-occupancy test-beam environment, using the longer shaping time is a practical way to improve the overall signal-to-noise of the measurements.

6. Conclusions

These exercises modeled the procedures typically used to characterize and tune the performance of silicon detector systems in use today. These procedures demonstrated the use of techniques to measure thresholds and gain on individual channels and provided a way to study the dependence of noise on signal shaping time. Such procedures are frequently performed while characterizing the design of a new readout chip, commissioning a new detector system, or monitoring changes in operating characteristics throughout the lifetime of a detector system.

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