QIE : Performance Studies of the Next Generation Charge Integrator

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ABSTRACT: The Phase 1 upgrade of the Hadron Calorimeter (HCAL) in the Compact Muon Solenoid (CMS) detector at the Large Hadron Collider (LHC) will include two new generations (named QIE10 and QIE11) of the radiation-tolerant flash ADC chip known as the Charge Integrator and Encoder or QIE. The QIE integrates charge from a photo sensor over a 25 ns time period and encodes the result in a non-linear digital output while having a good sensitivity in both the higher and the lower energy values. The charge integrator has the advantage of analyzing fast signals coming from the calorimeters as long as the timing and pulse information is available. The calorimeters send fast, negative polarity signals, which the QIE integrates in its non-inverting input amplifier. The input analog signal enters the QIE chip through two points: signal and reference. The chip integrates the difference between these two values. This helps in getting rid of the incoming noise, which is effectively cancelled out in the difference. Over a period of about six months between September, 2013 and April, 2014 about 320 QIE10 and about 20 QIE11 chips were tested in Fermilab using a single-chip test stand where every individual chips were tested for it's characteristic features using a clam-shell. The results of those tests performed on the QIE10 and QIE11 are summarized in this document.

KEYWORDS: HCAL, Phase 1 upgrade, front-end electronics, QIE.

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Contents

1. Introduction

The HCAL in CMS can be divided into four parts: Barrel (HB), Endcap (HE), Outer (HO) and Forward (HF) ,see ref. [1]. The different parts of the HCAL share a common electronics chain. The QIE converts the signal received from the phototransducers into a digital output which is then transmitted to the back-end electronics. Two types of the QIE - QIE10 and QIE11 are discussed in this document. The QIE10 is a crucial part of the HF and processes the signal coming from Silicon photo multipliers (SiPMs) while the QIE11 is a part of the electronics in the HB and HE. The QIE10 has a wide dynamic range, see figure 1 - it integrates 330 pC charge with a resolution of 3 fC requiring a 17 bit dynamic range. The charge can be expressed in terms of mantissa and range. The charge values are sorted into 256 bins, which can be expressed in 8 bits of data. The bins are called Mantissa (M). Each range can be divided into 64 bins (M0-M63) and there are four such ranges (R0-R3) scaled by factors of 8. Each range is further subdivided into four subranges (SR0-SR3). Each of the subranges has a specific sensitivity. The range, also called the exponent consists of 2 bits of the output data, while the mantissa is represented by 6 bits of data in the output.

The sensitivity and dynamic range of both the inverting and non-inverting inputs are the same. Time to digital conversion or TDC is an important added feature in the new QIE, which, was missing in the previous QIE8. The QIE has four almost identical capacitors (CID0-CID3) through which the input signal is passed. The digital output therefore has a four clock period latency of a 100 ns due to the four functions - integrate, compare, digitize and reset. The QIE has a 64 bit serial register which, is crucial to it's programming.
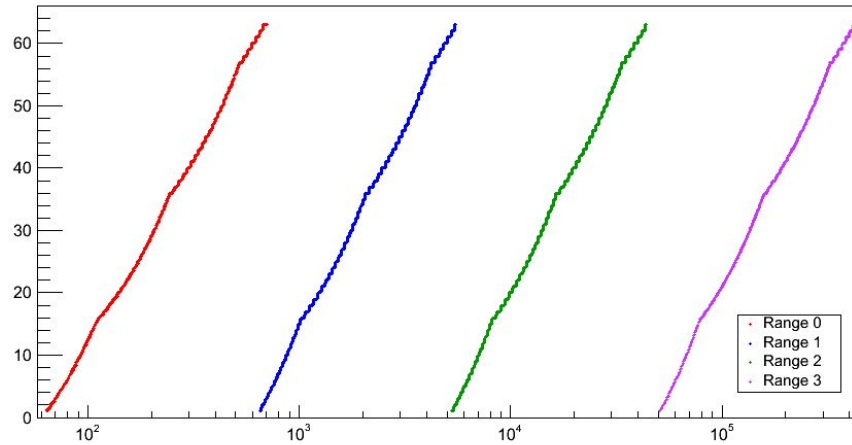
Figure 1. Mantissa vs Charge - All four Ranges

2. QIE10

The following features are studied and observed to understand the behaviour of the chips. The results are then compared to the expected theoretical values to determine good behaviour of the chip and consequently whether it can be accepted or rejected.

1. Pedestal tuning
2. Range overlap
3. Sensitivity or bin-width
4. TDC

2.1 Pedestal Tuning

The adjustable mantissa reported by the QIE when no charge is flowing through it is called the pedestal. This pedestal is flexible and can be adjusted to a higher or lower value by pedestal tuning with the help of the serial. The polarity, the overall pedestal DAC value and each of the individual CID tuning of the pedestal can all be adjusted through the serial. When dealing with a huge number of chips it is helpful to have them all tuned to the same pedestal value. The natural pedestal is usually a number between Mantissa 2 - 7 but for the sake of uniformity all 320 chips were tuned to Mantissa 3 (M3), see figure 2. It is also important to check that the pedestal remains stable over time, see figure 3.
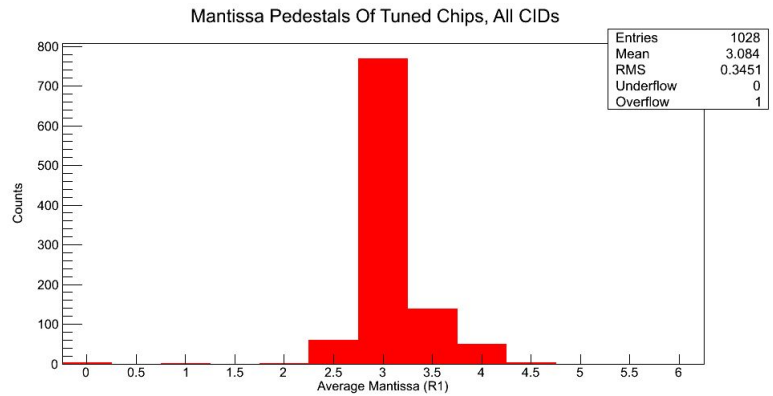
Figure 2. Pedestal Tuned to M3
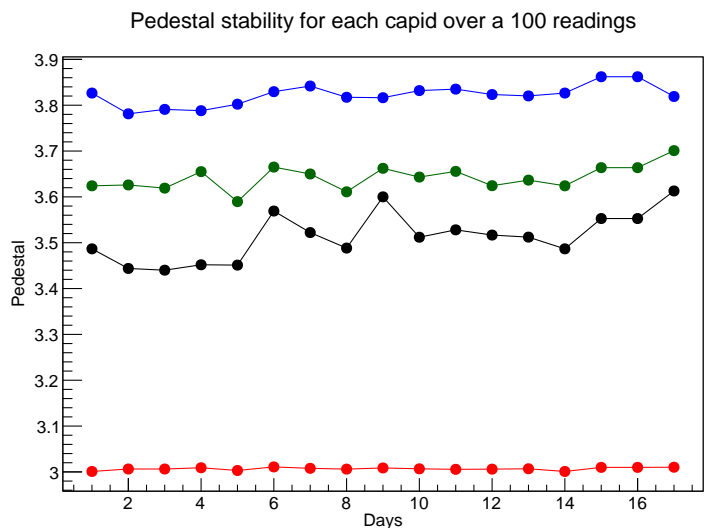
Figure 3. Pedestal stability over a period of 17 days for each CapID

2.2 Range Overlap

The QIE has four ranges, each higher than the previous one by the order of one magnitude. A certain overlap of about 3 ADC counts is present between the ranges, see figure 4.

2.3 Sensitivity

The sensitivity can be calculated from the slope of the charge vs mantissa plot for each sub-range, see figure 5. This sensitivity or charge/bin in each subrange is supposed to remain constant
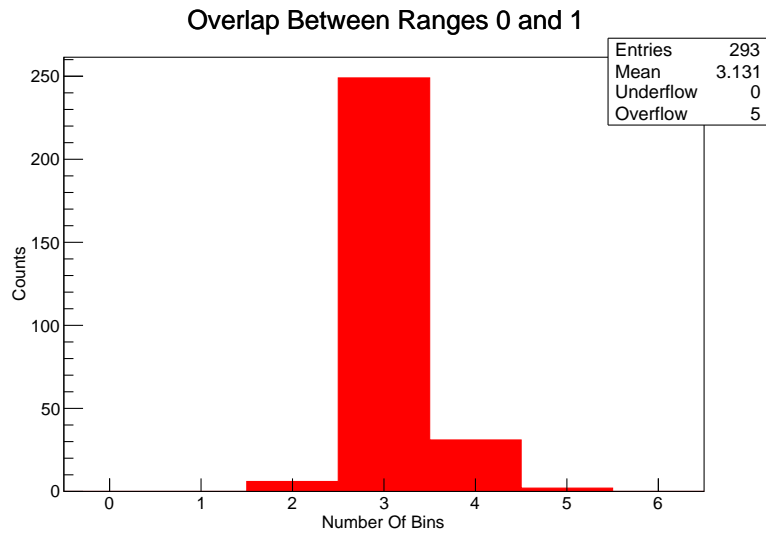
Figure 4. Overlap of ranges
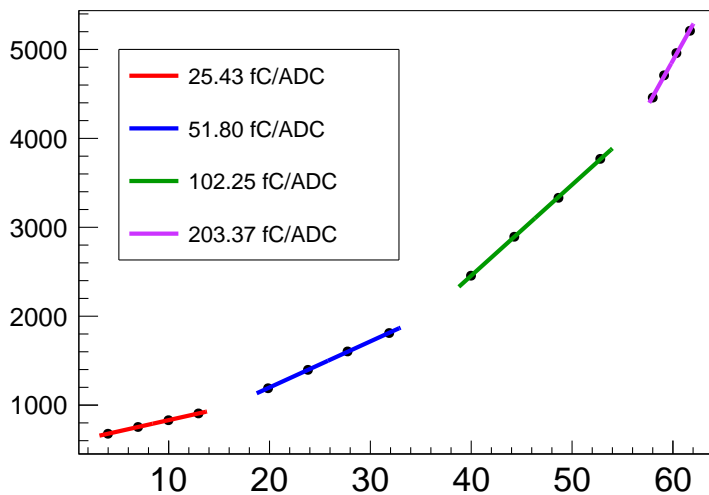
Figure 5. Charge vs Mantissa plot to determine Sensitivity

and has expected theoretical values, see figure 6. The differential non linearity plot, see figure 7 demonstrates the match between the theoretical and experimental values.

2.4 TDC

The Time to the Digital Conversion is an important added feature in the QIE10. It tells us when in the 25 ns window the pulse arrives. The 25 ns is divided into 50 bins (TDC0-TDC49) of 500 ps each, see figure 8. The TDC information is conveyed in 6 bits of the output data.
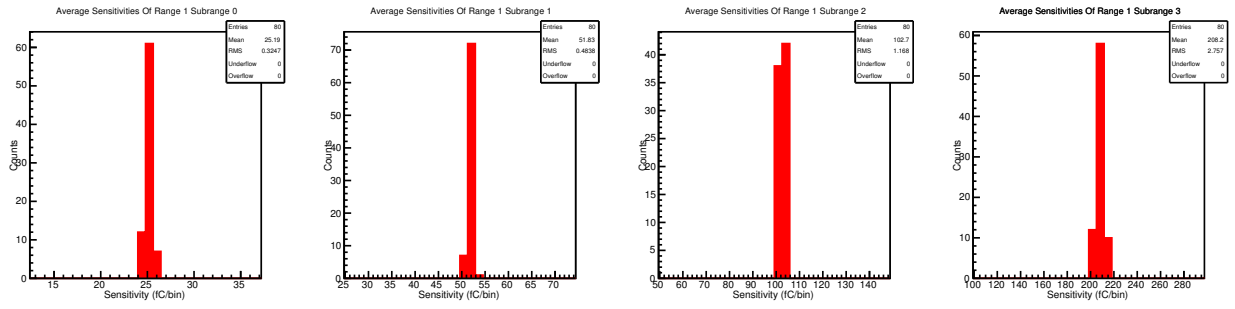
Figure 6. Almost constant sensitivity in each subrange of R1
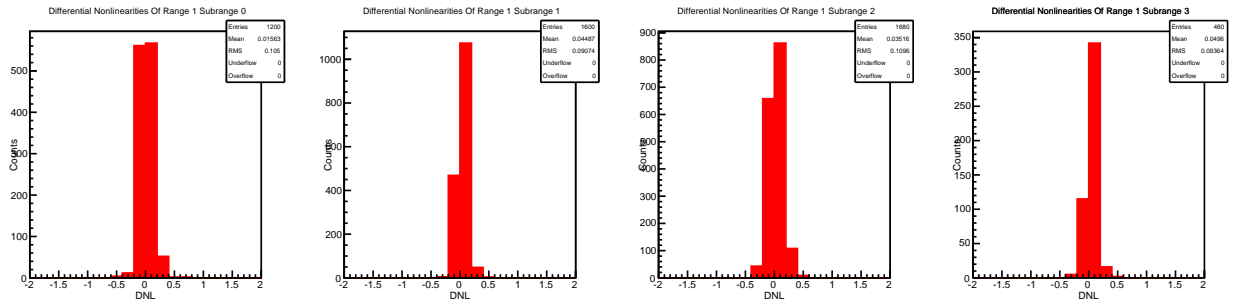
Figure 7. Differential Non Linearity plot for sensitivity in R1
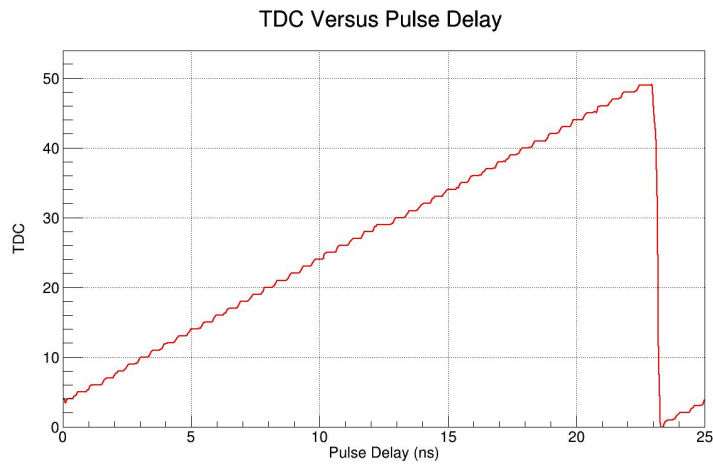
Figure 8. TDC reported in the 25ns window

There are two sepcial TDC codes:62 and 63. When the pulse is always above the discriminator the TDC reports 62 and when it is always below the discriminator it reports 63, see figure 10. The
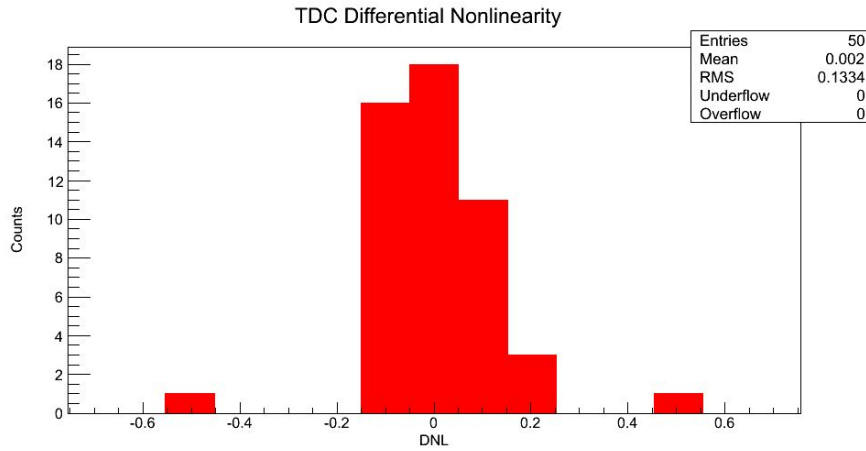
Figure 9. Differential Non Linearity plot of TDC

discriminator can be set to any value desired depending on how much charge is being integrated by the QIE.

3. QIE11

QIE11 will be a part of the front electronics of the HB and HE. The two main differences of the QIE11 from the QIE10 are : a) The existence of shunts which can bring about an increase in the sensitivity upto a factor of 12, see figure 11. The shunts can be acyivated or deactivated in a number of different combinations depending on the sensitivity factor desired. This is again done through the Serial Register. The increased sensitivity factor is necessary as the QIE11 has to handle the high gain of the SiPMs in HE/HB. b) Much lower input impedance - less than 10 ohms as opposed to the 20 ohms impedance in QIE10

4. Conlcusion

Around 330 QIE10.p5 chips have been tested in FNAL successfully. The chip behaves as expected.

The first prototype of QIE11.p1 has also been successfully tested at FNAL, the shunts are working fine and producing the expected increase in sensitivity.

A large engineering run to produce around 10,000 chips each of QIE10 and QIE11 will be done by Winter 2014.
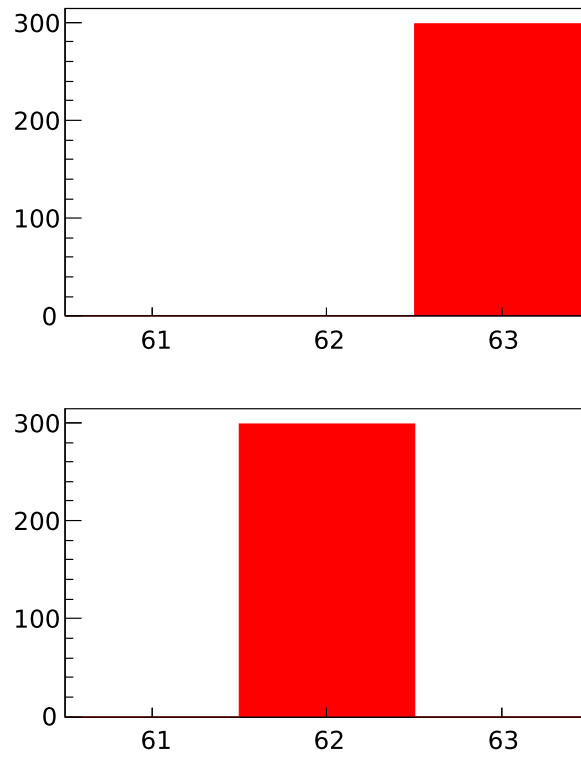
Figure 10. TDC63 (remains below threshold) in the first plot and TDC62 (remains above threshold) in the second
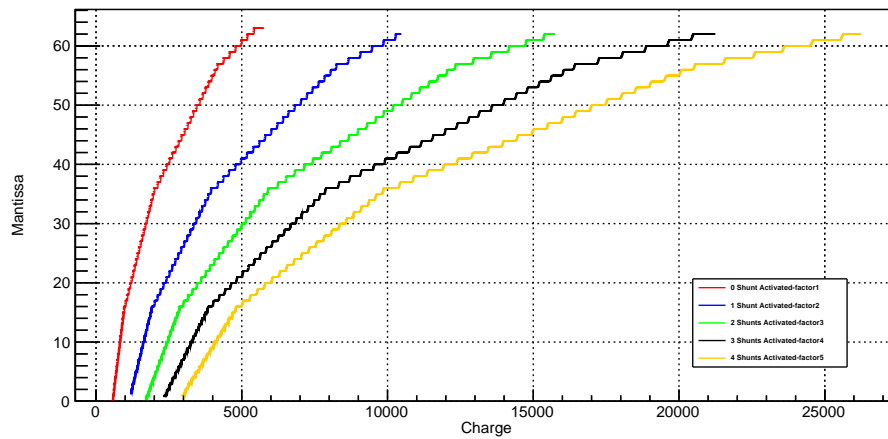

Figure 11. Range 1,with increased sensitivity upto a factor of 5

Acknowledgments

References

[1] CMS Collaboration, *"CMS Technical Design Report Volume 2, Physics Performance"* *J.Phys. G***34** (2007) 995-1679,doi:10.1088/0954-3899/34/6/S01.

[2] CMS Collaboration, *"The CMS experiment at the CERN LHC"* *JINST***4** (2008) S08004, doi:10.1088/1748-0221/3/08/S08004.

[3] CMS Collaboration, *"Phase 1 Upgrade of the CMS Hadron Calorimeter"* (2014).

[4] A.BAumbaugh et al. *"Charge Integrator and Encoder ASIC for Readout of the CMS Hadron Calorimeters Photodetectors"* (1998).