Uneven Bin Width Digitization and a Timing Calibration Method Using Cascaded PLL

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***Abstract*— Digitizers with uneven bin widths become more practical as the calibration in digital domain becomes convenient. In order to specify and compare the measurement ability of digitizers with uneven bin widths, it is necessary to define a parameter that takes effects of the various bin widths into account. In this paper, a parameter called equivalent bin width is defined based on mechanism of digitization. A scheme for timing bin widths calibration using cascaded phase lock loop (PLL) circuits is also presented in this document.**

***Index Terms*— Fast Timing, Front end electronics, Phase Lock Loop, Time to digital converters**

I. Introduction

In the history, calibration in digital domain was not as convenient as today, and therefore large amount of efforts were made to reduce differential nonlinearity of the digitizer, essentially in analog domain. With availability of bin-by-bin calibration in online system, especially inside FPGA devices, digitizers with uneven bin widths become more acceptable and applicable. In many cases, such as in FPGA based TDC [1-6], allowing uneven bin widths reduces implementation complexity as well as cost significantly.

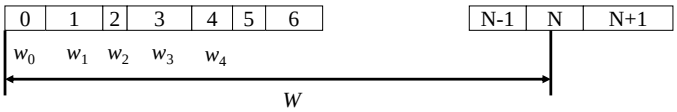

Fig. 1. Digitization with uneven bin width

In order to specify and compare the measurement ability of digitizers with uneven bin widths, it is necessary to define a parameter that takes effects of the various bin widths into account. A natural choice is the average bin width but it is not very suitable for describing measurement precision. For example, a TDC with alternating 20 ps and 0 ps bins has average bin width 10 ps, but it can only make measurements with precision as a TDC with 20 ps bins. Therefore, it is necessary to define a new value based on mechanism of digitization.

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In this paper, a value called equivalent bin width is first defined in Section II.

Unlike ASIC TDCs in which differential non-linearity (DNL) can be well controlled and a lot of times the raw TDC bin number can be directly used without calibration, in FPGA TDCs, the DNL is large and a bin-by-bin calibration is indispensable. A scheme of generating correlated hits with cascaded PLL for fast automatic calibration is covered in Section III.

Several details regarding the implementation of the cascaded PLL and further applications of the cascaded PLL are discussed in Section IV.

II. Definition of Equivalent Bin Width

In this section, we define a value that reflects the measurement precision in actual digitization process. When the digitizer has bins with various widths, there are two effects that must be considered. First, in many cases, the input to be measured may have all possible values with the same probability which is true in for TDC when the TDC clock is not correlated to the input hits. In this situation, a hit is more likely to fall into a wider bin than into a narrower bin. Second, assume all bins are correctly calibrated, when a hit falls into a narrower bin, the measured result is more precisely reflect the actual input value than that in a wider bin.

If the bin widths of a digitizer are w_i, and W is the sum of the widths being considered (see Fig. 1) then the equivalent standard deviation σ_{eq} can be defined as:

$$\sigma_{eq}^{\ 2} = \sum_i \left(\frac{w_i^{\ 2}}{12} \frac{w_i}{W} \right) \quad W = \sum_i w_i \tag{1}$$

Note that the contributions of wider bins are significantly larger than that of narrower bins, which are proportional to the third power of the widths. When an event falls into a wider bin, it is clear that the error of the measurement represented by the factor ($w_i^2/12$) is larger. In addition, the event is more likely to fall into a wider bin and the factor (w_i/W) in the sum is the probability. Equation (1) is true for events evenly spread over the entire range W of the digitizer.

We further define an equivalent bin width w_{eq} to represent the capability of the measurement precision that the digitizer is able to make from the equivalent standard deviation (see also Ref. [7]):

$$w_{eq} = \sigma_{eq} \sqrt{12} = \sqrt{\sum_i \left(\frac{w_i^{\ 3}}{W} \right)} \tag{2}$$

A digitizer with various bin widths makes measurements with precision as a digitizer with w_{eq} bin width. From Equation (2) above, it is obvious that for a digitizer with even bin width w, its equivalent bin width $w_{eq} = w$.

It should be pointed out that when the total width W is calculated, only the bins that actually used in the measurements should be included. In an FPGA based TDC, for example, the delay line length is usually chosen to be longer than the clock period. When the input hits are recorded, only a portion of the delay bins will register hits. Here the total width W should be the sum of the widths of these bins, not all bins. Note that the total width equals to the clock period in this case.

III. Cascaded PLL for Timing Bin Calibration

A special issue of the FPGA-based TDC is its large differential nonlinearity (DNL), which is seen as large variation of apparent width of each TDC bin. Furthermore, the propagation speed of the delay cell is a function of temperature and power supply voltage. Therefore, it is necessary to calibrate the delay line as frequently as possible, preferably online. In this section, several topics regarding automatic calibration are discussed.

For FPGA-based TDCs, bin-by-bin calibration is recommended since the widths of the bins vary by a large range.

In the bin-by-bin calibration scheme, a bin width histogram is first booked and then summed into a calibration lookup table. In this process, random hits are used which are generated either by actual events or an oscillator uncorrelated with the system clock. In order to reduce statistical fluctuation, very large number of events must be collected that increases calibration time when high precision calibrations are required. To speed up the calibration process, a scheme using cascaded PLL circuits is developed to generate calibration hits that are evenly spread relative to the system clock. The scheme will discussed in detail in this section.

A. Calibration Processes

Assuming that the widths of all TDC bins are measured and stored in an array w_k, then the calibrated time t_n corresponding to the center of bin n can be written as:

$$t_n = \frac{w_n}{2} + \sum_{k=0}^{n-1} w_k \tag{3}$$

It should be emphasized that it is crucial to calibrate to the centers of the bins, i.e., the first term representing the half width must not be omitted. It is not impossible for one to implement the sum term only and omit the half width term when the calibration algorithm is buried in complicate codes.

It can be shown that the RMS measurement errors are the minimum when the times are calibrated to the centers of the bins. Consider the RMS error σ contributed by one bin with lower and upper limits of t_1 and t_2 respectively. If this bin is calibrated to a value t_c between the lower and upper limits, the contribution of the error can be written:

$$\sigma^2 = \frac{1}{(t_2 - t_1)} \int_{t_1}^{t_2} (t - t_c)^2 dt = \frac{(t_2 - t_c)^3 - (t_1 - t_c)^3}{3(t_2 - t_1)} \tag{4}$$

When the bin is calibrated to the center, i.e., $t_c = (t_1 + t_2)/2$, the error above reaches a minimum which is $(t_2 - t_1)^2/12$.

The sum term in equation (2) represents the calibration to the edges of the bins. When all the bins have identical width, the half width term is a constant offset and calibrating to either bin edges or to bin centers will result in the same RMS errors. However, when the widths of the bins are different, the RMS errors will increase.

Integrating the look-up table (LUT) for the calibration to the centers of the bins takes a few extra steps than calibrating to the edges. Once the widths of all TDC bins become available, usually as contents of the DNL histogram, a sequence controller starts to build the LUT in the FPGA's internal memory. The process is as following:

1. Half of the width of the first bin becomes the time at its center.
2. Another half bin width of the first bin and the half bin width of the second bin are added to get the center time of the second bin.
3. This sequence is repeated for remaining bins.

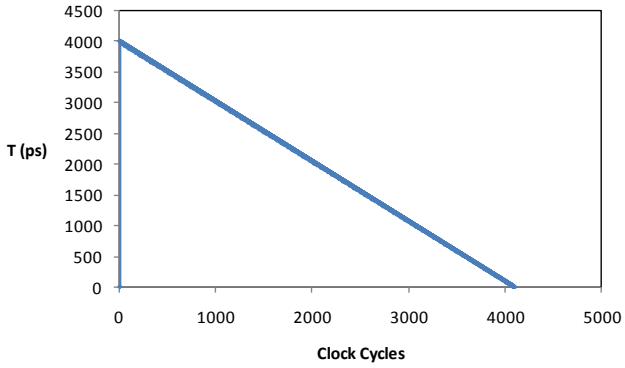
B. Calibration Hits: Random vs. Correlated

The widths of the TDC bins are measured through booking a DNL histogram. After booking a large amount of hits into the histogram, the count in each bin is proportional to its widths. For example, if 16384 hits are booked into the histogram and assume these hits are evenly spread over 4000 ps, the period of 250 MHz clock driving the TDC, then the width of an N-count bin is N*(4000 ps)/(16384) = N*0.24 ps.

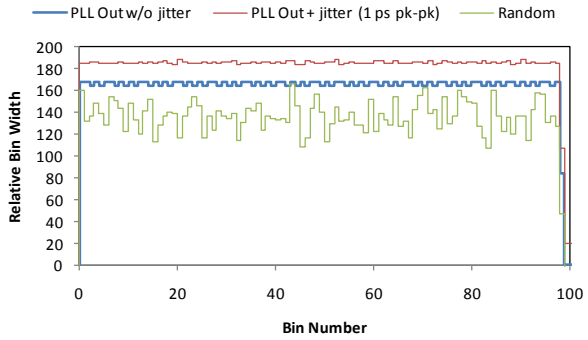
There are two options for generating the calibration hits. The most common approach is to use random real event hits during the operation. Alternatively, hits generated by an oscillator different from the one driving the TDC clock may be used as the calibration hits. Care must be taken to ensure that the calibration hits have no correlation with the TDC clock. In high energy physics applications, for example, it is safer to use an on-board free running clock rather than a clock signal derived from the accelerator RF. A disadvantage of the random hit approach is that the statistical fluctuation may cause errors in the calibration LUT. The errors will reduce as $1/\sqrt{N}$ when the total number of hits N increases. Sometimes a very large amount of calibration hits is necessary in order to reach required precision.

An alternative method of generating calibration hits is to use correlated pulses that have repeating rate slightly different than the system clock frequency. For example, if the system clock frequency is 250 MHz and the calibration hits are generated by a clock at 250.06 MHz = (4096/4095)*250 MHz, up to 4096 timing phases are possible between the calibration hits and the system clock within the 4000 ps period. To generate the calibration clock, large frequency multiplication ratios such as 4096 are needed which excess capabilities of most PLL

circuits. Therefore, multiple PLL circuits are cascaded together to achieve required frequency multiplication ratio. The time differences of 4096 calibration clock cycles relative to the 250 MHz clock edges are plotted in Fig. 2(a). The shift step between two cycles is 0.97 ps.



(a)



(b)

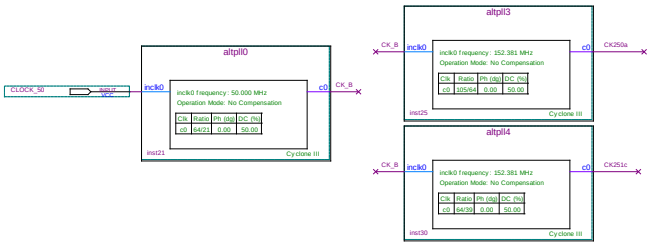
Fig. 2. (a) Relative timing between the calibration clock cycles and the system clock, (b) Simulation of the bin width booking with calibration clock edges

Histograms of a delay line 4000 ps long are booked as show in Fig 2(b) with 16384 events that scan the range 4 times. To show the fluctuation more clearly, an even bin width of 40.6 ps is chosen. When the calibration clock has no jitters, the apparent widths of the bins jump up and down due to step rounding at the boundary. A small jitter helps the histogram to become smoother with the dithering effect. As a comparison, the third histogram is booked with totally random events. For relatively small number (about 160) per bin, a large fluctuation is seen as expected. (Arbitrary offsets are added so that the histograms can be seeing clearly.)

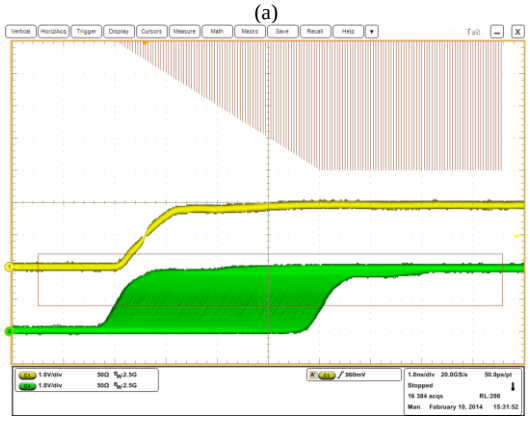
The advantage of this approach is that the precision of the calibration LUT is predictable and can be achieved with a small number of hits. The drawback is that the precision of the LUT is limited (in the case above, 0.97 ps) and it will not simply improve by collecting more hits, although it is sufficient for many practical applications.

C. Actual Implementation

A practical implementation inside an Altera Cyclone III FPGA device uses three PLL circuits as shown in Fig. 3(a). The input clock (CLOCK_50) to the FPGA chip is 50 MHz and an intermediate clock (CK_B) with frequency 152.381 MHz = (64/21)*50 MHz is generated with the first PLL. The intermediate clock drives the second PLL with ratio (105/64) to generate the 250 MHz system clock (CK250a). It also drives the third PLL with ratio (64/39) to generate the 250.06 MHz calibration clock (CK251c).



(a)



(b)

Fig. 3. (a) Cascaded PLL circuits in Altera Cyclone III FPGA, (b) Oscilloscope screen capture of the edges generated by calibration and system clocks

In Fig 3(b) 16384 calibration clock edges are measured while the oscilloscope is triggered by the transition edges (Channel 1) generated by the 250 MHz system clock. The calibration clock edges (Channel 4) cover the 4000 ps range evenly and the histogram accumulated in 50 ps bins serves as a demonstration of calibration lookup table.

IV. DISCUSSIONS

In the implementation described in this paper, the connections between the PLL blocks are routed inside the FPGA. In some FPGA families, connecting PLL blocks inside the FPGA is not supported and the connections are to be routed on printed circuit board. In this case, it is preferable to use differential standard such as LVDS for the clock loop back path and a lot of time, the clock outputs must be sent out from dedicated pins. A very careful pin planning is needed before designing the printed circuit board.

The ratio between the clock frequencies can also be other values to generate clocks with small relative phase shift. The reason why we choose 4095/4096 is for the convenience of calibration process. Using a 2^N number as events to be collected for full coverage makes design of the calibration sequence simple.

The clocks from the cascaded PLL blocks can also be used to generate pulses with arbitrary relative delays for TDC self test. Another application is to use the cascaded PLL block to make high precision measurements of relative phases of two

input clock signals. These applications will be discussed in separate papers.

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