A Pixel Readout Chip in 40 nm CMOS Process for High Count Rate Imaging Systems with Minimization of Charge Sharing Effects

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***Abstract* – We present a prototype chip in 40 nm CMOS technology for readout of hybrid pixel detector. The prototype chip has a matrix of 18x24 pixels with a pixel pitch of 100 μm. It can operate both in single photon counting (SPC) mode and in C8P1 mode. In SPC the measured ENC is 84 e^- rms (for the peaking time of 48 ns), while the effective offset spread is below 2 mV rms. In the C8P1 mode the chip reconstructs full charge deposited in the detector, even in the case of charge sharing, and it identifies a pixel with the largest charge deposition. The chip architecture and preliminary measurements are reported.**

I. Introduction

A hybrid pixel detector operating in a single photon counting mode requires a pixel readout chip with the geometry that matches the geometry of the detector array [1]. Stringent and growing requirements on smaller pixel size, higher data throughput and more sophisticated functionality like amplitude or time measurements, etc. are imposed on such imaging systems. Additionally charge sharing cannot be neglected when pixels achieve smaller sizes. The effect of the charge sharing was analyzed many times in the literature both for strip and pixel detectors, for example:

- to find the total charge deposited in detectors the charges were summed from a several neighbor detector strips/pixels [2, 3],
- to eliminate the double counting caused by all efficiency losses due to charge sharing [4],
- to minimize the effects of the charge sharing on spectral response [5].

Suppressing the negative effects of charge sharing directly in the pixel readout is not an easy task, mainly because of strong demands on low power dissipation, small silicon area of a single pixel and effects of mismatch [6-10]. Nanometer CMOS or 3D technologies seem to be very attractive for pixel readout integrated circuits [11, 12], especially in the case of implementing more complex functionality or advanced algorithms on the chip. However, these technologies are mainly driven by high density and very fast digital circuits, while for hybrid pixel detectors the analog performance of front-end electronics like noise [10], offset spreads [11] or crosstalk minimization are of primary importance.

Therefore, we have designed a prototype integrated circuit of pixel architecture in TSMC 40 nm CMOS technology (with 10 metal layers), that operates as a fast single photon counting readout for an X-ray imaging application. Additionally, the chip has C8P1 algorithm implemented [8, 9]. It measures total amount of the charge deposited in the detector (reconstructs full signal), even in the case of charge sharing, and it identifies a pixel with the largest charge deposition (see Fig. 1).

Our aim was to perform tests with the chip bump bonded to a silicon detector with a use of X-ray radiation. Because in our case the bump bonding is done on the chip-to-chip basis, thus it has pitch limitation. As a result of that the prototype has pixel size of 100 x 100 μm^2, despite the fact that significantly smaller pixels are achievable in this technology node.

In the course of the design, a special attention was given to:

- low noise performance of the front end electronics, which is essential for achieving correct operation of the C8P1 algorithm,
- fast operation of the front-end electronics by using short peaking times in the shapers,
- trimming DACs to adjust both gain and offsets in each pixel and auto-zero correction techniques for fast and low area comparators,
- chip testability to check a single pixel performance and the effectiveness of the algorithm responsible for minimization of the charge sharing effects.

The paper is organized as follows. In Section II we briefly remind the main idea of C8P1 algorithm. The prototype chip architecture is presented in Section IIIl. The preliminary measurements of IC connected to pixel are discussed in Section III.

II. C8P1 Algorithm Idea

The goal of algorithms implemented for the elimination of the charge sharing effect inside the integrated circuit, is the

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compensation for both errors in pulse amplitude (total photon energy) and precise hit-position measurements. The C8P1 algorithm presented for the first time during Nuclear Science Symposium 2011 [8] shows the best behavior among many others analyzed. It uses eight comparators (C8) in each pixel to determine if its value is higher than all eight neighbors, and one discriminator (P1) in the signal rebuilt hub, which verifies the total amount of charge deposited in each group of four pixels (Fig. 1).

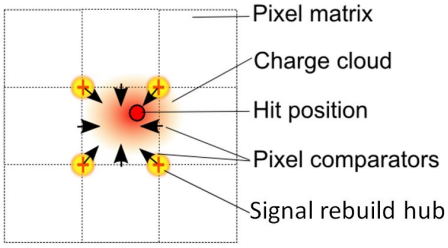
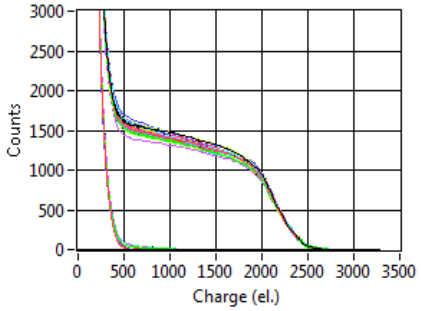


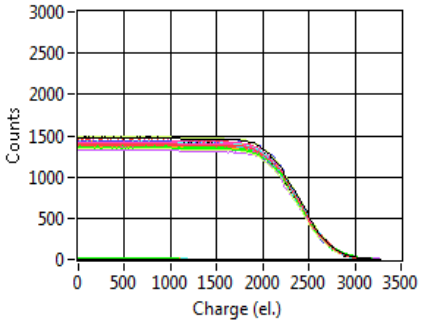
Fig. 1. C8P1 algorithm: to reconstruct the total charge; each pixel corner has a signal rebuild hub. Eight comparators (shown as black arrows) are used to determine the winning pixel.

Examples of threshold scans simulated in single photon counting (SPC) mode and C8P1 mode are presented in Fig. 2 (pixel pitch is 100 µm and photons of energy of 8 keV are deposited in 300 µm thick Si pixel detector) [8, 9]. In performed simulations, we assumed to not only diffusive charge spread occurring in the course of charge drifting towards the electrodes but also limitations in a readout electronics, i.e. signal fluctuations due to noise and mismatch (gain and offsets). Two effects are clearly visible:

- no noise counting in C8P1 mode,
- an additional offset in the CP81 mode compared to SPC mode which depends on the noise level and the comparator offsets.



(a)



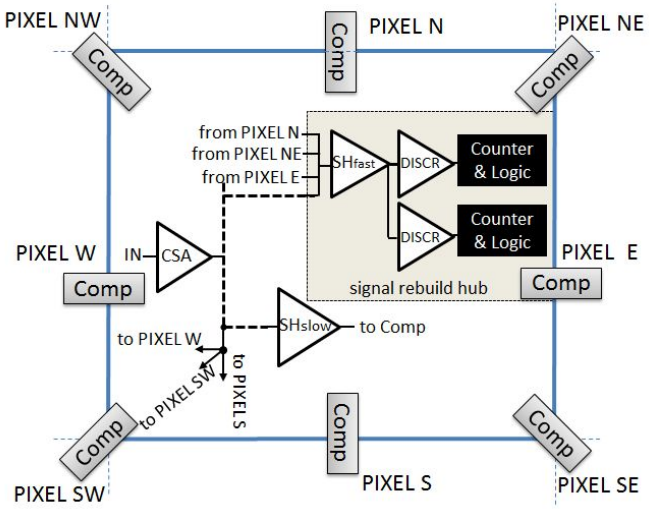
(b)

Fig. 2. Simulation of charge sharing for pixel pitch 100 µm: a) SFC mode, b) C8P1 mode.

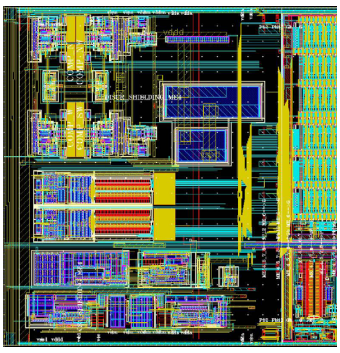
III. Single Pixel Architecture and Interpixel Communications

A block diagram of the analog part of the front-end electronics and the pixel layout are shown in Fig. 3. Each pixel contains:

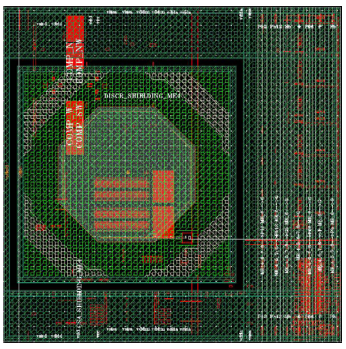
- a charge-sensitive amplifier (CSA) with a controlled gain and a slow shaper (SHslow with peaking time t_{peak}=80ns) only for the use inside a pixel,
- a fast shaper (SHfast with t_{peak}=48ns and with a controlled gain) and two discriminators (DISCR) with 6-bit trim DACs in signal rebuild hubs to share between four pixels (one discriminator is used for C8P1 algorithm and the another one for threshold scan in energy measurement),
- a set of comparators (Comp) with auto-zero correction to share each of them with a neighbouring pixel.



(a)



(b)



(c)

Fig. 3 Single pixel: a) front-end electronics diagram, b) layout - layers up to MET2 without dummy filling structures, c) layout - layers MET7-MET10; each readout pixel is provided with octagonal pad for bump bonding (40 µm wide) to make the tests with pixel sensors possible.

The chip can operate in several different modes and the most important are:

- a standard fast SPC mode with two discriminators operating per pixel (without any inter-pixel communication),
- a C8P1 mode with effective pixel size of 100 µm,

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- test SPC mode with additional charge summing in signal rebuilt hub but with C8P1 algorithm switched off.

The C8P1 mode uses reconstruction of full signals that is performed in signal rebuild hubs using fast shapers. The proper hit allocation is done later, involving controlled delay time up to 150 ns and using the slow shapers signals and eight comparators.

IV. Preliminary Measurements

A. Measurement setup

The prototype chip contains a matrix of 18x24 pixels located in the upper part of the chip. The control and the power supply wire-bonding pads are placed in the bottom half of the chip. The tests were performed both for the integrated circuits alone and for IC stud bump bonded to the silicon detector (see Fig. 4). Because we were limited by used bonding techniques only a matrix of 18x15 pixel is connected to the detector.

The tests were performed using NI PXI-6562 200 MHz Digital Waveform Generator/Analyzer. Software for communication with the chip and automatic data analysis is written in LabView 2013.

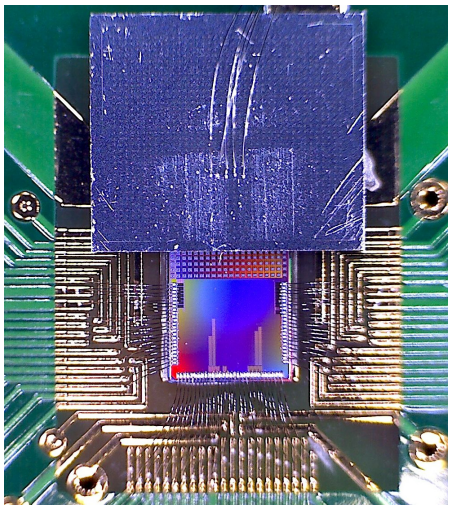

Fig. 4. Photo of the chip bump-bonded to the detector.

B. Offsets, gain and noise in SPC mode

The AC coupling implemented in the front-end electronics between the CSA and the shapers significantly reduces the problem of offset spread from pixel to pixel. The measured offset spread from pixel to pixel of the IC before correction is about σ = 20.2 mV and after correction it is reduced to σ = 1.9 mV rms using the 6-bit trim DAC.

The gain measurements were performed using an internal test calibration circuit (voltage step was applied via series capacitor of 4.8fF) and also with X-ray tube. The exemplary results of the test with internal test calibration circuit is shown in Fig. 5. The chip operates in the high gain mode. The measured mean gain and the gain spread on one sigma level are respectively 80.6 $\mu V/e^-$ and 3.8 $\mu V/e^-$.

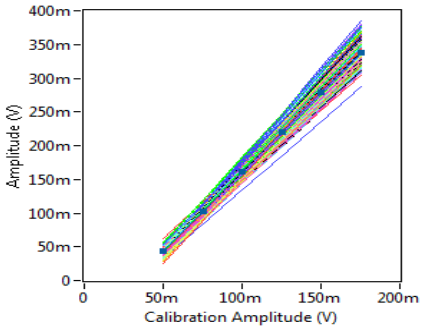

Fig. 5. Pulse amplitude at the output vs. calibration pulse amplitude.

The gain measurements with X-rays (Roentgen tube with Cr anode) gives the mean gain and the gain spread of respectively 79.7 $\mu V/e^-$ and 4.53 $\mu V/e^-$. The measured mean ENC for all pixels connected to the detector is 83.8 e^- rms. The chip has a possibility to control the gain in a wide range. For the low gain mode the mean gain and the gain spread are respectively 17.9 $\mu V/e^-$ and 1.37 $\mu V/e^-$. In this mode the mean ENC for all pixels connected to the detector is 104 e^- rms.

C. C8P1 algorithm measurements

The first tests in C8P1 mode were performed using the internal calibration circuit. We injected 4 different charges to neighboring pixels at the same time as it is shown schematically in Fig. 6.

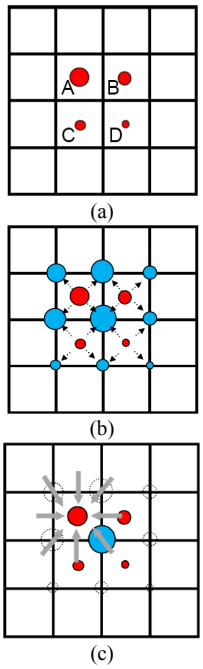

Fig. 6. Initial tests with internal calibration circuit to verify C8P1 algorithm: a) injection of 4 different charges to four different neighboring pixels, b) test SPC mode with additional charge summing in signal rebuilt hub but with C8P1 algorithm switched off, c) C8P1 mode.

We observed a discriminator output (threshold scan) for the following cases (see Fig. 7):

a) SPC mode - pixel A,

b) SPC mode - pixel B,
c) SPC mode – pixel C
d) SPC mode – pixel D,
e) test SPC mode with additional charge summing in signal rebuilt hub but with C8P1 algorithm switched off – pixel A,
f) C8P1 mode with the winning pixel A.

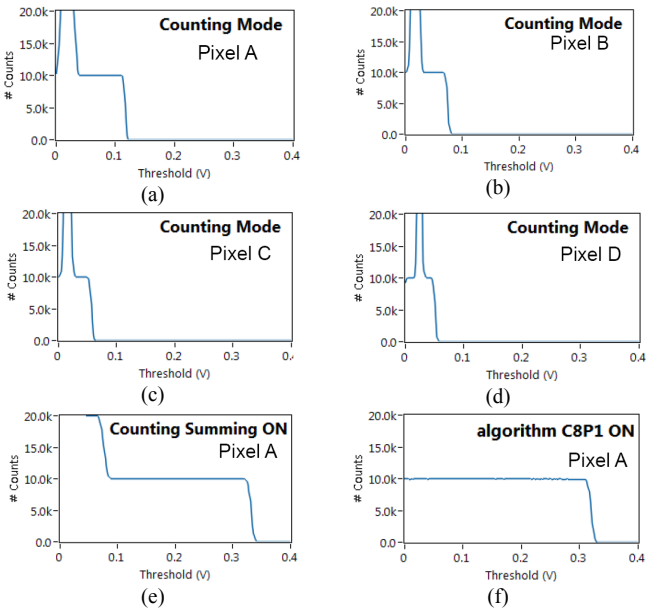

Fig. 7. Threshold scans during the initial tests with internal calibration circuit to verify C8P1 algorithm – see description in the text.

The results of the first preliminary tests with 8 keV X-rays are shown in Fig. 8. During this test the detector was uniformly illuminated with X-rays. The obtained results confirm that our C8P1 algorithm [8] implemented in the chip prototype in advanced 40 nm node works properly.

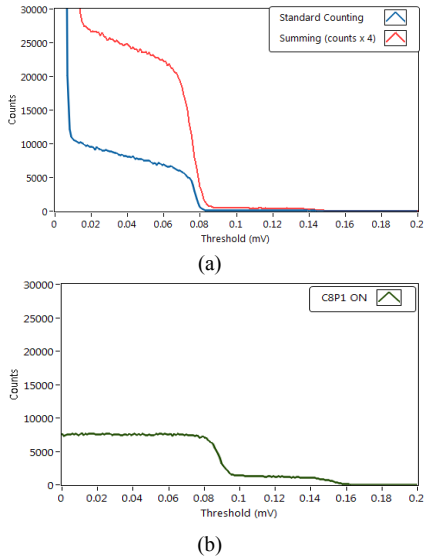

Fig. 8. Threshold scans with X-ray beam : a) in SPC mode and in test SPC mode with additional charge summing in signal rebuilt hub but with C8P1 algorithm switched off, b) in C8P1 mode.

V. Summary

We have presented a prototype pixel readout IC working in SPC mode and C8P1 mode for hybrid semiconductor detectors for low energy X-ray imaging systems. The preliminary measurements confirm that the implemented architecture (see Fig. 3a), trimming functionality of multichannel chip together with a low noise performance allow to perform a complex operations on chip, like C8P1 algorithm. The CMOS 40 nm technology is also a very promising solution for future new generation of readout electronics for pixel detectors, especially when more complex functionality or advanced algorithms are required on the chip.

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