Degradations of threshold voltage, mobility and drain current and the dependence on transistor geometry for stressing at 77 K and 300 K

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***Abstract*—Based on test results and a procedure which can isolate threshold voltage degradation and mobility degradation from the drain current degradation, we found that the log-log curves of mobility degradation show saturation with a change of slope from about 0.4 to smaller values at room temperature. Although both the mobility and threshold voltage degradations are more severe at 77 K than at 300 K for the same stress time, the temperature effect on the mobility degradation is larger than that on the threshold voltage degradation. In addition, the degradations of transistors with three different widths are compared after the stress tests at room and cryogenic temperatures, leading to the observation of degradation dependence on the transistor width. It is observed that the width dependence is more evident at 300 K and the temperature plays a more significant role on the degradation for larger width transistors.**

***Index Terms*—Cryogenic temperature, drain current degradation, hot-carrier effect, mobility degradation, threshold voltage degradation, stress tests**

I. Introduction

Electrical equipment operating at low temperature has drawn considerable attention over the last several decades because of the inherit performance improvements [1]-[3]. The liquid nitrogen range has commercial applications including large computer systems [2]. The work in this paper is motivated by the Long-Baseline Neutrino Experiment (LBNE) [4], where the related integrated readout electronics will work inside a liquid argon chamber. Given that the liquid nitrogen temperature (77 K) is very close to the liquid argon temperature (89 K), inexpensive and easy to obtain, the experimenters have chosen to perform these tests in liquid nitrogen.

Although cryogenic operation improves transistor performance in criteria such as speed, thermal noise, leakage current, etc, hot-carrier degradation accelerates at the same time [1][4]. Hot-carrier induced damage leads to degradation of various transistor characteristics such as the shift of threshold voltage, the decrease of subthreshold slope, the reduction of transconductance and the degradation of drain current. These effects are directly related to the long term performance of electrical circuits. The ultimate goal of this work is the development of microelectronic circuits for use in high energy physics experiments in liquid argon. Consequently, the intermediate goal is the development of reliable circuits that can operate for a long time (>20 years) at cryogenic temperatures. Finally, the immediate goal and the subject of this paper is an understanding of the effect of hot carriers on deep-submicron transistor performance especially at cryogenic temperatures.

Section II is an introduction to our tests of the transistors and their parameters. In section III, a procedure is presented to derive the threshold voltage degradation and the mobility degradation from the drain current degradation in the linear region. Then, based on this procedure, in Section IV, the threshold voltage degradation and mobility degradation are quantified by measuring the drain current of transistors biased in the linear region after each stress stage. Finally, the drain current degradations of transistors with three different widths are compared in Section V.

II. Test Transistors and Test Parameters

The test transistors were fabricated on the same wafer in a low power version of a 1.5 V, 0.13 μm bulk CMOS process with 2.3 nm effective gate oxide thickness, Lightly-Doped Drains (LDD) and Shallow Trench Isolation (STI). The MOSFET sizes available for testing are 80 μm/0.13 μm, 80 μm/0.5 μm, 2 μm/0.13 μm and 0.64 μm/0.13 μm.

The devices were stressed at drain voltages larger than nominal operation voltages and the drain stress voltages were deliberately chosen in order to observe detectable degradation within reasonable stressing time. The transistor gates were biased at half of the respective drain voltages [5][6]. A more detailed description of the chosen biasing in this paper is given in [5]. In brief, by our own testing, the dependence of peak substrate current is varying weakly with V_{GS} around the peak. Thus, $V_{GS} = 0.5V_{DS}$ is an adequate approximation of the most severe stressing condition in this case. Tests were performed at room temperature (300 K) and in liquid nitrogen temperature (77 K). For each kind of transistor, at least three of them were tested at different stress voltages. As the drain current can be easily measured and its degradation is related to the hot-electron-generated interface state density [7], the drain

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current degradation is often used as the indicator of hot-carrier effect. Specifically, a drain current degradation in the linear region ($V_{GS} = V_{DD}, V_{DS} = 0.05$ V or 0.1 V , and V_{DD} is the power supply voltage) is the bias condition of choice for most experimenters because under these conditions the entire length of the channel, including the damaged region is in inversion [8][9]. Therefore, after each stress time step, the drain current I_D versus V_{GS} at $V_{DS} = 0.05$ V was measured and the drain current degradation $\Delta I_D / I_D$ was examined. ΔI_D is the drain current difference between a fresh device and a stressed device, which is $\Delta I_D = I_D(t=0) - I_D(t=t_{stress})$. In addition, the threshold voltage degradation was also examined and the threshold voltage was extracted using the constant current method [10].

III. Procedure to Distinguish Threshold Voltage Degradation and Mobility Degradation

Hot carriers can cause damage through various processes whose probability is given by the distribution of the attainable energy of hot carriers. The high energy carriers can generate interface states and even surmount the silicon-insulator barrier to enter the insulator [6][9], which affects the threshold voltage V_{TH} and the carrier mobility μ. By the following deduction, both the threshold voltage degradation and the mobility degradation would be visible through the drain current degradation. According to the formula for the drain current of NMOS transistors in the linear region,

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS}\right) V_{DS} \quad (1)$$

the variation of drain current ΔI_D can be expressed as a function of the threshold voltage variation ΔV_{TH} and the mobility variation $\Delta\mu_n$, as showed by (2).

$$\Delta I_D = -\mu_n C_{ox} \frac{W}{L} V_{DS} \Delta V_{TH} + C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS}\right) V_{DS} \Delta\mu_n \quad (2)$$

Dividing (2) by (1), yields a formula (3) for the relative current change:

$$\frac{\Delta I_D}{I_D} = -\frac{\Delta V_{TH}}{V_{GS} - V_{TH} - \frac{1}{2} V_{DS}} + \frac{\Delta\mu_n}{\mu_n} \quad (3)$$

This formula provides a basis for isolating the threshold voltage degradation ($\Delta V_{TH}/(V_{GS} - V_{TH} - 0.5V_{DS})$) and the mobility degradation ($\Delta\mu_n/\mu_n$) which leads to a procedure that can be applied to investigate the degradation of transistors. First, after each stress time step, the drain current I_D versus V_{GS} is measured. Second, based on the measured I-V curve, the threshold voltage V_{TH} is extracted through the constant current method [10]. In this way, both the drain current degradation and the threshold voltage degradation can be estimated. Finally, in substituting these two kinds of degradation to (3), the mobility degradation is obtained. Thus the respective contributions of the threshold voltage degradation and the mobility degradation from the drain current degradation of a transistor are obtained.

IV. Saturation of Mobility Degradation

Based on the procedure proposed in Section III, the curves of the drain current degradation in the linear region, the threshold voltage degradation and the mobility degradation are plotted. Fig. 1 shows the degradation curves with stress time for 2 μm/0.13 μm transistors at room temperature (RT) and for the stress voltage of 2.6 V. Up to 10% of the drain current degradation and the threshold voltage degradation, both curves follow the classical power law format $y = At^n$ [5]-[9][9][11] (where A is a free fitting parameter that depends on stress voltage, t is stress time and n is a parameter containing information on the degradation mechanisms and may depend on the technology.) However, at around 2000 seconds when the mobility degradation is 13%, the curve shows a departure from the classical law. There is a visible knee and the slope of the mobility degradation curve changes from 0.41 to 0.21 in a log-log scale. Fig. 2 shows the degradation curves with stress time for 80μm/0.5μm transistors at room temperature and for the stress voltage of 3.0 V. Degradation levels are smaller but at approximately 200 seconds, where the mobility degradation is less than 1%, the slope of the curve noticeably begins to change.

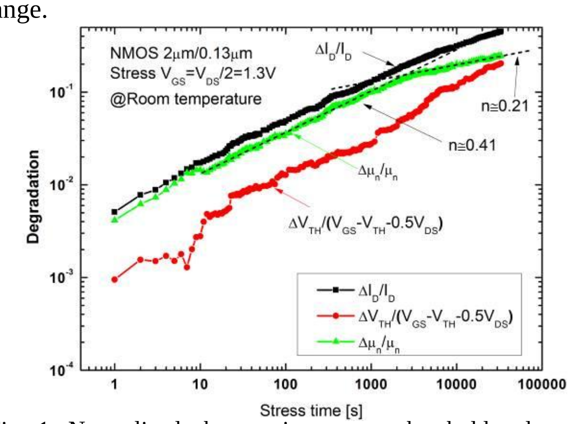

Fig. 1. Normalized changes in current, threshold voltage and mobility with stress time for 2 μm/0.13 μm transistor at room temperature. Stress voltage $V_{DS} = 2.6$ V.

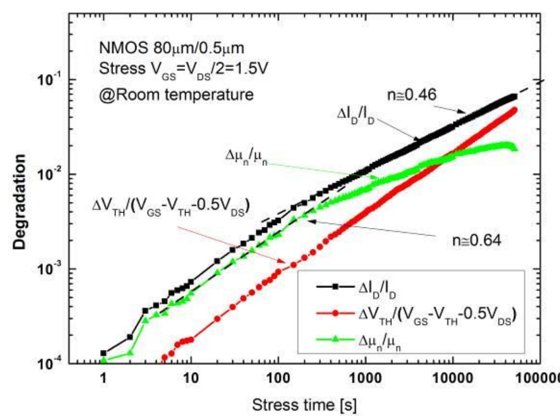

Fig. 2. Normalized changes in current, threshold voltage and mobility with stress time for 80 μm/0.5 μm transistor at room temperature. Stress voltage $V_{DS} = 3.0$ V .

Fig. 3 (a) shows the mobility degradation curves with stress time for 0.64 μm/0.13 μm, 2.0 μm/0.13 μm, 80 μm/0.13 μm and 80 μm/0.5 μm transistors measured at room temperature. All the curves appear to have the tendency to saturate at room temperature, which implies that the degradation mechanism changes because the mobility is related to the interface-state density induced by hot carriers [12].

Fig. 3 (b) shows the mobility degradation curves with stress time for 0.64 μm/0.13 μm, 2.0 μm/0.13 μm, 80 μm/0.13 μm and 80 μm/0.5 μm transistors measured in liquid nitrogen (Cryogenic Temperature (CT)) bath. Unlike the stress tests at room temperature, the saturation tendency during the testing periods is not visible on any of the curves.

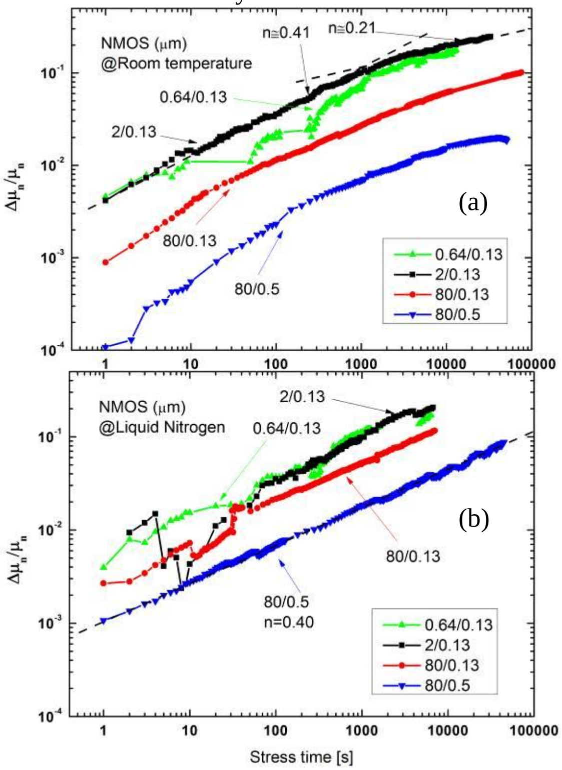

Fig. 3. Normalized changes in mobility with stress time (a) at room temperature, (b) in liquid nitrogen. Stress voltages $V_{DS} = 3.0$ V are for 80 μm/0.5 μm transistor; $V_{DS} = 2.6$ V for all other transistors.

Fig. 4 (a) and (b) show both the mobility and threshold voltage degradation curves at room temperature and in liquid nitrogen for the 80 μm/0.13 μm and the 80 μm/0.5 μm transistors, respectively. Both the mobility and threshold voltage degradations in liquid nitrogen are larger than that at room temperature for the same stress time. However, the relative magnitudes of the threshold voltage degradation and the mobility degradation, as extracted by the method introduced in Section III, are observed to be different depending on the operating temperatures. One way to study this is to fix the total current degradation at a certain point regardless of the stress time necessarily to reach that point. Table I fixes the total degradation at 5% and shows how much of that total current degradation is contributed by mobility degradation and threshold voltage degradation, respectively. Table II shows the same but at 10% of total current degradation. In both tables, contributions of the mobility degradation increase and contributions of the threshold voltage degradation decrease from the tests at room temperature to the tests in liquid nitrogen. In other words, there are always two components to the total current degradation, mobility degradation and threshold voltage degradation, regardless of the temperature. However, a transistor degrades its mobility more rapidly than its threshold voltage from the tests at room temperature to the tests in liquid nitrogen. This observation leads to the conclusion that the temperature effect on the mobility degradation is larger than that on the threshold voltage degradation.

TABLE I. DEGRADATION COMPONENT CONTRIBUTIONS FOR STRESSING AT 300 K AND 77 K AND AT DIFFERENT STRESS VOLTAGES

Size and drain current degradation	Temperature	Stress voltage (V)	ΔV_{TH} contribution percentage	$\Delta\mu_n$ contribution percentage
80 μm / 0.13 μm (5%)	300 K	2.4	2.2%	2.8%
		2.5	2.2%	2.8%
		2.6	2.2%	2.8%
	77 K	2.4	1.5%	3.5%
		2.6	1.9%	3.1%
80 μm / 0.5 μm (5%)	300 K	3.0	3.1%	1.9%
		3.1	3.5%	1.5%
		3.5	3.2%	1.8%
	77 K	3.0	2.0%	3.0%
		3.1	2.1%	2.9%
		3.5	1.8%	3.2%

TABLE II. DEGRADATION COMPONENT CONTRIBUTIONS FOR STRESSING AT 300 K AND 77 K AND AT DIFFERENT STRESS VOLTAGES

Size and drain current degradation	Temperature	Stress voltage (V)	ΔV_{TH} contribution percentage	$\Delta\mu_n$ contribution percentage
80 μm / 0.13 μm (10%)	300 K	2.4	5.2%	4.8%
		2.5	4.8%	5.2%
		2.6	4.8%	5.2%
	77 K	2.4	3.9%	6.1%
		2.6	3.8%	6.2%
80 μm / 0.5 μm (10%)	300 K	3.0	-	-
		3.1	8.4%	1.6%
		3.5	8.2%	1.8%
	77 K	3.0	5.2%	4.8%
		3.1	5.4%	4.6%
		3.5	4.8%	5.2%

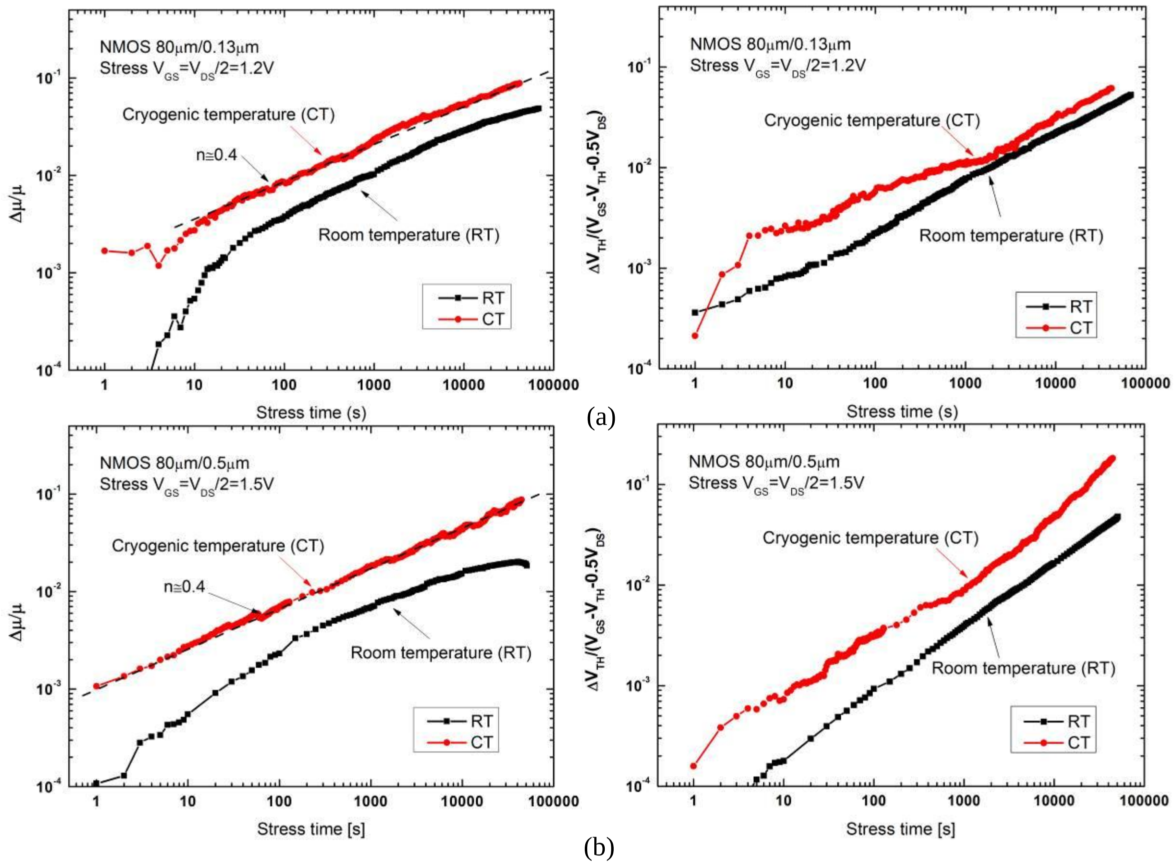

Fig. 4. Normalized changes in mobility and threshold voltage with stress time at room temperature (RT) and in liquid nitrogen (CT) for (a) 80 μm/0.13 μm (b) 80 μm/0.5 μm. Stress voltages $V_{DS} = 2.4$ V for 80 μm/0.13 μm transistor; and $V_{DS} = 3.0$ V for 80 μm/0.5 μm transistor.

V. The Degradation Dependence on Transistor Width

So far the existing analyses have been mainly focusing on the effect of the transistor length on degradation [6]-[9][11][13]. Only a few papers discuss the effect of width on transistor degradation [14][15], but degradation at cryogenic temperature is not their focus. In this work, we stressed transistors with the same length but different widths (0.64 μm/0.13 μm, 2 μm/0.13 μm and 80 μm/0.13 μm) at room temperature and in liquid nitrogen.

Fig. 5 and Fig. 6 show the drain current degradations in the linear region with stress time for transistors with three different widths at room temperature and in liquid nitrogen. Under both stress voltages ($V_{DS} = 2.4$ V in Fig. 5 and $V_{DS} = 2.6$ V in Fig. 6), the width indeed has effects on the device degradation at room temperature and in liquid nitrogen. The transistor with larger width (W=80 μm) degrades more slowly when compared to transistors with smaller widths (W=0.64 μm and 2 μm). However, the difference between W=0.64 μm and W=2 μm is insignificant, which implies that the degradation is a weak function of transistor width. Furthermore, the width effects are different at different temperatures. The width effect at room temperature is larger than that in liquid nitrogen regardless of whether the stress voltage is 2.4 V (Fig. 5) or 2.6 V (Fig. 6). For example, at room temperature, getting to the same percentage of degradation, such as 10% of $\Delta I_D/I_D$, the time it takes is one order of magnitude longer for transistors of W=80 μm than for transistors of W=0.64 μm or W=2 μm, while in liquid nitrogen the time is only approximately 5 times longer for W=80 μm than that for W=0.64 μm or W=2 μm. In addition, as the Fig. 3 showed, the mobility degradations are also width dependent and the width effect at room temperature is larger than that in liquid nitrogen.

Fig. 7 shows the normalized changes in current with stress time for transistors with three different widths at different stress voltages and at different temperatures. It is expected that the hot carrier degradation at low temperature is larger compared to the degradation at room temperature for the same stress time, and this is observed clearly for larger width transistors (W=80 μm), as Fig. 7 (a) shows. However, according to the test results, in up to 10% of the drain current degradation in the linear region, the degradation in liquid nitrogen is close to the degradation at room temperature for the smaller width transistors (W=0.64 μm and 2 μm), as Fig. 7 (b) and Fig. 7 (c) illustrate. This means that the temperature plays a more important role on the drain current degradation for larger width transistors (W=80 μm) than that of smaller width transistors (W=0.64 μm and 2 μm).

The width dependence can be attributed to a non-uniform channel across the width [14]. A non-uniform channel results in non-uniform current density. As the well-known model showed, the number of interface states generated by the hot carriers is a function of the drain current [16]; so this non-uniform current density may lead to non-uniform hot-carrier effects across the width of the device. For large and small width devices, these non-uniformities have different proportions, which give rise to the width dependence of degradation. In particular, in a technology with shallow trench isolation (STI), the electric field at the trench edge is enhanced [17] which introduces more severe hot-carrier effects. Hot carrier injection into the edge may not affect the entire channel for the wider devices while narrower devices would naturally experience this effect to a greater degree [5].

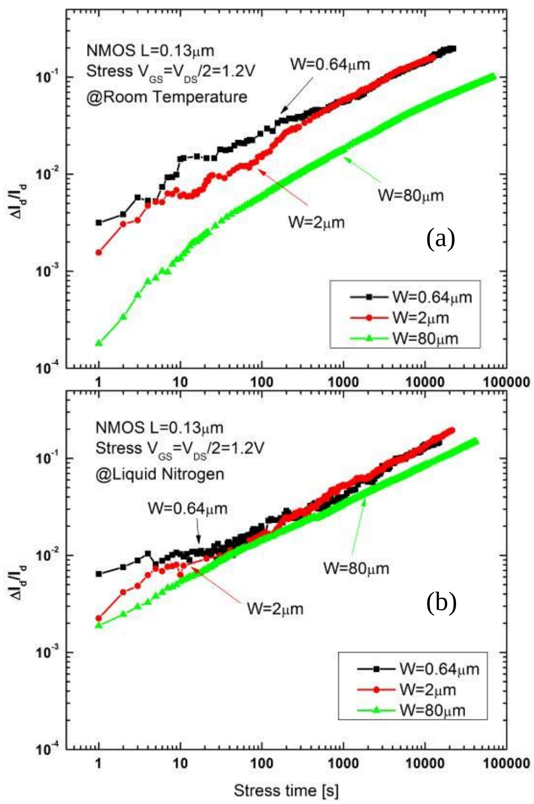

Fig. 5. Normalized change in current with stress time for different width transistors: (a) at room temperature, (b) in liquid nitrogen. In both cases, stress voltages $V_{DS} = 2.4$ V.

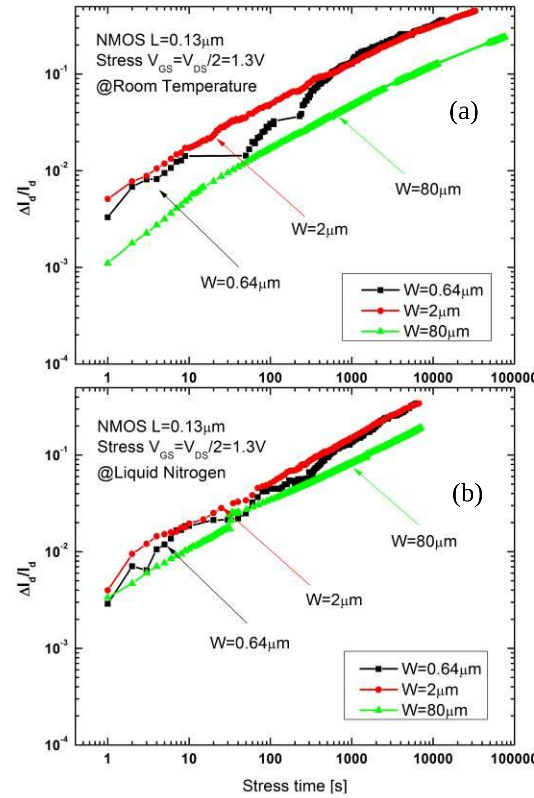

Fig. 6. Normalized change in current with stress time for different width transistors: (a) at room temperature, (b) in liquid nitrogen. In both cases, stress voltages $V_{DS} = 2.6$ V.

VI. Conclusion

This paper introduces a procedure which can isolate both the threshold voltage degradation and the mobility degradation from the drain current degradation in the linear region. Based on this procedure, the saturation tendency of the mobility degradation is found in room temperature tests. It is observed that the temperature effect on the mobility degradation is larger than that on the threshold voltage degradation. Moreover, the drain current degradation for transistors with three different widths (0.64 μm/0.13 μm, 2 μm/0.13 μm and 80 μm/0.13 μm) are compared. The dependence of drain current degradation on the transistor width is observed. First, the width dependence is evident at room temperature but not so evident at liquid nitrogen temperature. Moreover, the temperature plays a more important role on the drain current degradation for larger width transistors (W=80 μm) than on the smaller width transistors (W=0.64 μm and 2 μm).

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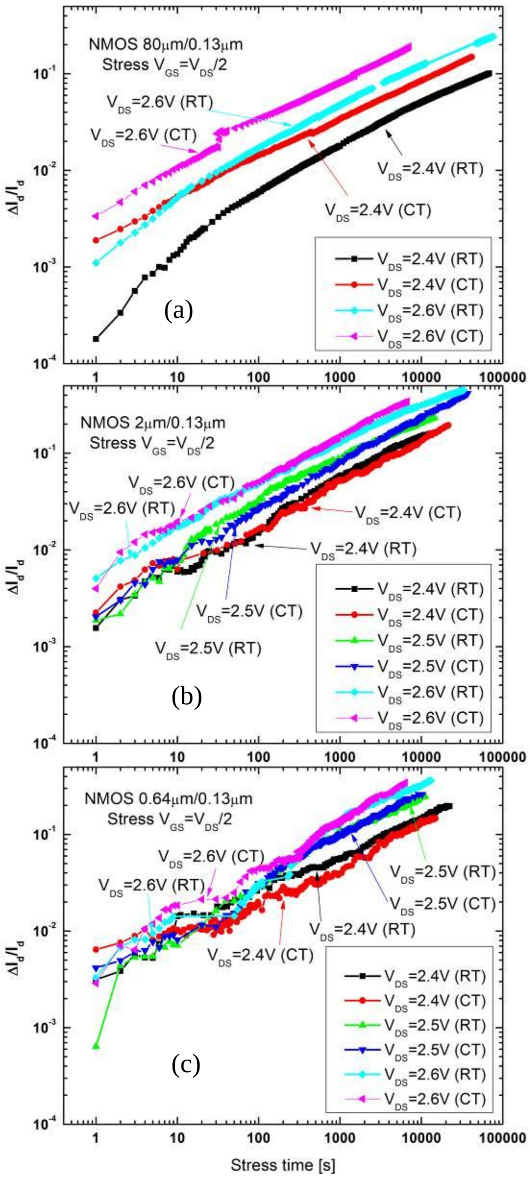

Fig. 7. Normalized change in current with stress time at different stress voltages and different temperatures: (a) 80 µm/0.13 µm transistor, (b) 2 µm/0.13 µm transistor, (c) 0.64 µm/0.13 µm transistor.

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