Design and Tests of the Vertically Integrated Photon Imaging Chip

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***Abstract*– The Vertically Integrated Photon Imaging Chip (VIPIC) project explores opportunities of the three-dimensional integration for imaging of X-rays. The design details of the VIPIC1 chip are presented and are followed by results of testing of the chip. The VIPIC1 chip was designed in a 130 nm process, in which through silicon vias are embedded right after the front-end-of-line processing. The integration of tiers is achieved by the Cu-Cu thermo-compression or Cu-based oxide-oxide bonding. The VIPIC1 readout integrated circuit was designed for high timing resolution, pixel based, X-ray Photon Correlation Spectroscopy experiments typically using 8 keV X-rays at a synchrotron radiation facility.**

I. Introduction

DRAWING on the experience of how major advancements in solid state detectors and readout integrated circuits (ICs) have revolutionized the High-Energy Physics (HEP) experiments, it is thought that the time is approaching for three-dimensional (3D) integration of ICs and building of detector assemblies. The 3D integration technology is one of the avenues pursued by industry for obtaining higher performance from the current generation of ICs. 3D ICs are formed by bonding two or more IC wafers (called 3D *tiers*), and interconnecting them with small (preferably single micron-size) through silicon vias (TSVs). Addition of TSVs to an IC may be achieved in many ways. Embedding of TSVs right after the front-end-of-line (FEOL) part of the manufacturing flow, as it is the case for the process used for the work described in this paper, permits small vias and does not impact the back-end-of-line (BEOL) part of the flow. On the other hand, such TSVs are shallow and remain buried in the substrate until a 3D assembly of wafers is thinned down, which requires additional processing steps.

Fermilab began investing in 3D technologies by prototyping a 3D pixel readout IC for the International Linear Collider (ILC) vertex detector in 2006 [1]. Subsequently, the ASIC Design Group submitted prototypes in the 3D multi-project wafer (MPW) run that was managed by Fermilab [2]. The designs targeted there the Compact Muon Solenoid (CMS) track-trigger concept for the High-Luminosity upgrade of the Large Hadron Collider (LHC), herein mentioned the ILC vertex detector that were the High Energy Physics (HEP) projects, and, as a spinoff of these efforts, X-ray imaging for the Photon Science. In a wider scope of projects, the role of rapid transfer of technological innovations from HEP to related fields, such as photon sciences, material science and nuclear medicine got emphasized once again. The Fermilab work on 3D circuits quickly evolved into a conglomeration of projects conducted by several groups working together under the 3D integration umbrella.

The paper is organized in 6 sections, including introduction. The second section provides an analysis of the benefits of 3D integration. The third section reveals details of a design of the VIPIC1 chip: the general architecture of the chip, the flow of data readout, the analog and digital pixel parts and the features related to the use of the 3D techniques. The fourth section discusses results of the bench tests of the chip. The last section of the paper concludes and summarizes the presented material.

II. Benefits of the Three-Dimensional Integration

The turn towards the 3D technology is due to the inability to overcome serious limitations in fine-grained detectors with large numbers of imaging elements using current detector technologies. This relates in particular to large-area pixel detectors. Technologies od 3D chips offer much more real estate and interconnections, which is invaluable in efforts to implement intelligent readouts that fit into the needs of modern experiments. 3D integration offers a transformational change to address current roadblocks and three breakthroughs deserve specific mention. These are: 1) the isolation of digital blocks from analog, low-noise parts, 2) distribution of power supplies on big chips without IR drops, and 3) integration of readout ICs on sensors that leads to tiling without dead space. Dead-area-less tiling eliminates wire-bonding for module mounting and allows on new types of supports.

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A comparison of isolation of digital blocks from analog parts on a classical 2D IC with a 3D device is shown in Fig. 1. Transistors in 2D chips share the same substrate and currents that are sent to the substrate material in blocks of intense digital activities may cause fluctuations of potentials of bodies of transistors in other parts and may affect their reference levels or cause injections to signal processing circuit networks due to non-zero substrate resistivity.

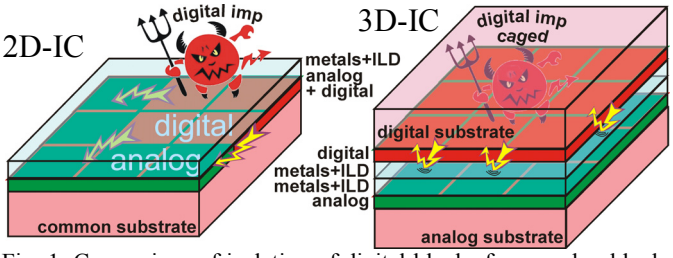

Fig. 1. Comparison of isolation of digital blocks from analog blocks on 2D integrated circuits with 3D integrated circuits.

Isolation in classical 2D processes is accomplished by placing transistors from blocks that may cause interference in triple or quadruple deep wells. Designers also use guard-rings as fire-walls between such blocks and pay careful attention to separation of analog and digital power supplies.

It is worth noting that the use of deep wells consumes a lot of space in project designs, thus increasing the silicon area e.g. a minimum distance of a deep well to other elements cannot be less than 3 μm in a typical 130 nm process. 3D integration allows a complete separation of aggressor and victim circuits by locating them on different tiers. It leads to uncomplicated separation of power supplies. Circuits can have separate substrates and even a shield may be built between tiers by using one or more metal layers at the tiers interface.

An improved power distribution network in a pixel readout IC is illustrated in Fig. 2. An IC can be constituted of just one tier fused to a sensor, and TSVs, distributed on the whole area of a chip, can provide connections to internal traces carrying power supplies, biases and signals. TSVs are exposed after thinning of an IC part of the assembly. Metal pads are deposited next on the exposed TSVs tips. By careful planning of the pads placement, low impedance paths to power all pixels, including those in the middle of a readout IC that usually are the biggest concern can be achieved. Designers have been facing significant challenges in large size 2D chips. TSVs make these challenges manageable.

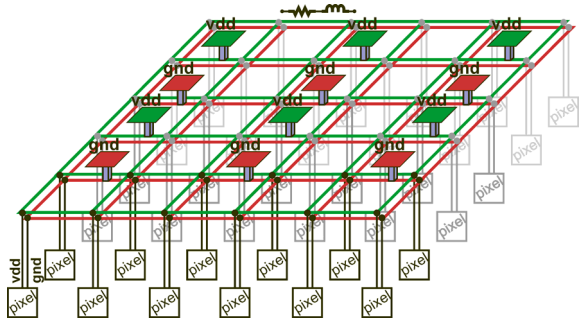

Fig. 2. Improved power distribution network by an array of power pads on the back side.

By using TSVs for threading all electrical connections to the side opposite to that on which the sensor is attached allows achieving new forms of pixel detectors as it is depicted in Fig. 3. Readout ICs are usually smaller than sensor planes due to the concerns of ensuring suitable chip yields that worsen with increasing die size and limitations of reticle sizes that are typically 2×3 cm^2. Thus, multiple readout ICs are attached to a large area pixelated sensor in a tiling pattern to build larger area detector modules.

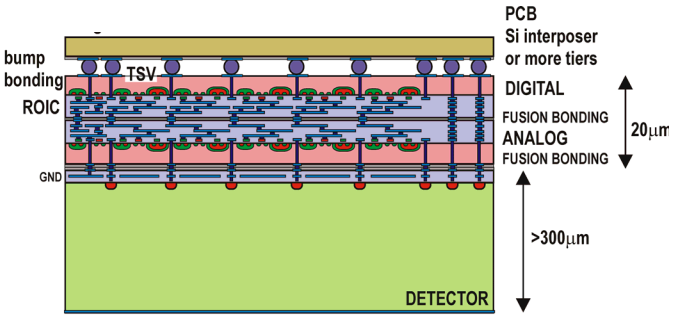

Fig. 3. Illustration of a 4-side buttable, dead-area-free detector structure without wire-bonding.

A readout IC that employs 3D techniques may be built without any peripheral segments dedicated for example to wire-bonding pads or otherwise adding area that cannot be usable for direct processing of signals from a detector. Also all the circuitry required for conditioning of data and signals and physical communication with the chip can be located on the added on tier. Thus, an assembly employing a chip with the 3D features is capable of breaking the convention of hybrid pixels with 2D chips of relatively small detector modules and gaps in active areas. Four-side buttable, dead-area-free detector structures can eventually eliminate modular structures with their associated coverage gaps. Construction of fully active detectors, containing megapixel arrays in seam-less macroscopic planes, limited only by a size of a wafer, may come to light. Interposers will play a key role, as these silicon or glass based passive tiers with TSVs and interconnects are ideal to serve as versatile mounting beds for 3D assemblies, interfacing them to acquisition systems. The structures employing interposers will be rigid and will look and perform as monolithic structures, while possessing all features in which hybrid assemblies show their superiority, e.g. sensor can be optimized to characteristics of the radiation to be used for. 3D integration is the toolbox to achieve these goals.

III. Foundations of the VIPIC Project and Design Details of the Chip

The Vertically Integrated Photon Imaging Chip (VIPIC) project targets development of a camera for X-ray Photon Correlation Spectroscopy (XPCS) [3] experiments using 8 keV X-rays as a part of the detector development program for the National Synchrotron Light Source (NSLS) at the Brookhaven National Laboratory (BNL). The occupancy in the XPCS experiments is low, typically reaching a few photons/mm^2/μs but the timing requirements are stringent. Achieving microsecond precision or even better is the key for advancing this sector of science. The target for the VIPIC project is to operate without any dead-time and register photon

hits providing a two-dimensionally resolved impact position and time of arrival for every photon impact.

The VIPIC1 is the first chip designed in the scope of the VIPIC project. Its construction was possible by successful application of bonding of two wafers together. Two bonding methods were applied. The first method of integration of tiers was Cu-Cu thermo-compression [4] and the second one was Cu-based oxide-oxide bonding [5]. They were a part of the 3D MPW run managed by Fermilab.

The set of requirements of the XPCS experiments is not satisfied by any existing system and led to the architecture of the VIPIC1 device that is significantly different from any currently available readout circuit developed for the Photon Science [6][7]. The VIPIC1 chip is a small prototype, the size of which resulted from the division of the reticle into 5.5×6.3 mm^2 blocks in the first 3D MPW run. The design was accomplished through a collaboration of Fermilab and AGH-UST. It was submitted for fabrication in mid-2009 and the first prototypes, diced out from correctly bonded wafers, became available mid-2012 and they were tested forthwith.

A. Application of the 3D integration for VIPIC1

The VIPIC1 chip was designed for fabrication in a bulk CMOS 130 nm process that had 1 μm diameter TSVs added on as a part of the process after completion of FEOL. The wafers were fabricated by Chartered Semiconductor (Global Foundries) and the subsequent 3D face-to-face stacking of the wafers and the remaining processing was done by Tezzaron [2]. The circuitry of the VIPIC1 chip was allocated between two tiers and the design was carried out as if there were two independent ICs. Connections for inter-tier flow of signals had to be appropriately organized so that the two parts matched when combined. The two tiers were joined together when both parts of the VIPIC1 chip were still on the wafers. A so called bonding interface, which was a special arrangement of the most top metal layer on both wafers to be bonded, was required in order to make fusing two wafers together with electrical connections between tiers possible. The bonding interface was composed of small, 2.7 μm uncovered metal bond-point octagons that were instantiated on a continuous hexagonal grid at a pitch equal to 4 μm. Most of bond points were present only for providing mechanical strength of the connection; some of them were used to carry signals between the tiers. An illustration of a topology, showing the division of circuitry between the tiers in a single pixel, is given in Fig. 4. The analog chain, composed of a charge sensitive amplifier, a shaping filter, a discriminator, trimming DACs for adjusting the filter time constant and for correction of discriminator offsets and a test charge injection circuitry, is located on the first tier that will be called *the upper tier*. The digital blocks, including main components such as *set_pixel* and *reset_pixel* configuration latches, a 12 bit pixel configuration register with shadow latches, two 5-bit long event counters with their control logic, a hit registration logic and a part of the priority encoder logic with a pixel address generator (to the extent which is attributable to a given pixel) are located on the second tier that will be called *the lower tier*. There are 13 connections threading between the tiers. Only one, i.e. the output of the discriminator is single-ended and every connection uses 2 metal dots for better yield, thus there are 50 bonding interface points used for signals in every pixel in total. The pixel size of VIPIC1 is 80×80 μm^2.

Removal of the substrate material that encloses a 3D IC stack after the face-to-face bonding allows accessing the tips of the still buried TSVs. Only about 6 μm of the original thickness of the tier is left. Eventual patterning of Aluminum bonding pads on the exposed TSVs tips provides means of driving the electrical connectivity down to the chip. Thinning of VIPIC1 from the top of the upper tier allows attachment of a pixel sensor and access to all the chip pins that were routed to the periphery [2].

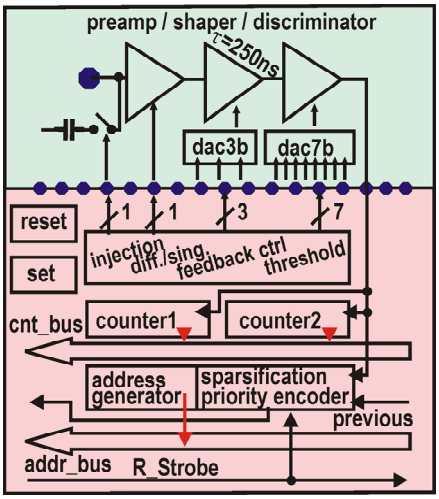

Fig. 4. Block diagram of a pixel depicting split of analog (green) and digital (red) circuitries between tiers and showing signals other than power supplies that traverse through the bonding interface.

A picture of the VIPIC1 die that was prepared in the manner described above was mounted on a PCB for bench tests and is shown in Fig. 5. A square form in the center part of the die is an array of 64×64 pads for connecting to a sensor.

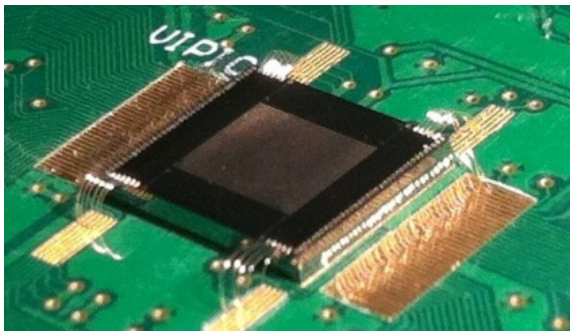

Fig. 5. Picture of a VIPIC1 die that was thinned from a side of the upper tier mounted on a PCB for bench tests.

The design of the VIPIC1 prototype was done in such a way that exposing either the lower tier or the upper tier vias offers access to all the same connections required to run the chip, i.e. to all signals, power supplies, biases, etc. All were one-to-one rerouted from one side to the other, except that on the upper tier, they were distributed over the periphery and, on the lower tier, they were distributed over the entire surface [2]. Both types of chips were delivered by Tezzaron. Simultaneous availability of both types of chips results from fabrication of chip parts, which later become the tiers, on the same wafer in

suitable, axially symmetrical locations on the reticle [2]. Ultimately the plan is to access VIPIC1 from both the top and bottom. This requires thinning of both sides. After thinning of the upper tiers and attachment to a sensor, the opposite side can be thinned. This requires further post-processing of devices after their delivery and is envisaged for later, after proving the functionality of the chips without attached sensors. The test results presented in this paper were obtained with the VIPIC1 dies mounted as shown in Fig. 5.

B. Readout architecture and data flow

The VIPIC1 topology was determined by matching the needs of experiments with a synchrotron radiation beam and assuming an evolutionary path of further developments for the VIPIC project. Equipping every pixel with a measurement unit that would provide accurate timing of an event with respect to the time frame of a much longer duration is foreseen as one of the steps. At the present time, VIPIC1 does not extend beyond registering radiation hits and assigning their occurrence to the coarse time frames that are orchestrated from the outside of the chip.

The VIPIC1 chip is a prototype matrix of 64×64 pixels, which is divided in 16 groups (4 rows of 64 pixels each). Every group has one serializer and an LVDS driver that allows outputting data from a group. All serializers work in parallel timed by the Serial_Clk clock. The structure of the VIPIC1 chip is shown in Fig. 6.

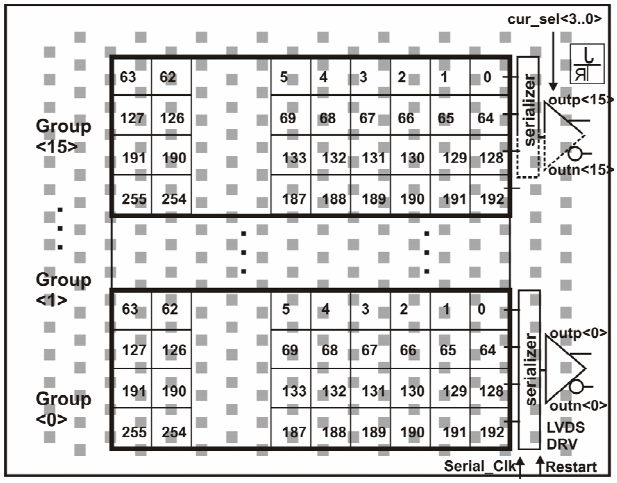

Fig. 6. Structure of the VIPIC1 chip .

Every pixel outputs only digital data that is a binary word combining the contents of a 5 bit in-pixel event counter and an 8 bit address of a hit pixel. This information gets to a serializer, where it is supplemented by the 010 *START* symbol and is sent off the chip in the following order: first a counter content is sent and then a pixel address. Pixels that were hit are identified by sparsification engines that run simultaneously in each group. Sparsifiers allow fishing out pixels with hits in each time frame. The process of acquisition of new events continues during sparsification. A standard period of the time frame was set as Δt=10 μs, which defines the base time resolution of VIPIC1. The sparsification circuitry is inspired by an encoder idea proposed for the MEPHISTO prototype [8] in the past. The VIPIC1 encoder selects pixels for readout and generates addresses of hit pixels in the binary code automatically. Unlike the reference idea, it uses tristateable buffers and interleaved NOR and NAND stages to improve speed and compactness of the design. A binary tree of the sparsifier designed is shown in Fig. 7. The number of pixels is reduced from the actual 256 pixels in VIPIC1 to 32 only in this representation for the sake of clarity. The inputs to the sparsifier are marked from in00 to in1F. States on these inputs indicate whether a given pixel was hit or not. Two pixels are shown active in the system. Their states are snapped in the figure as an example to explain how the system works. Those are in01=1 and in02=1. There are two directions of flow of information in the sparsifier. The first one is towards the HIT signal, which effectively yields a multi-input logic OR gate. Activation of the HIT signal switches off pull-downs built with NMOS transistors and the sparsifier becomes ready to output an address of a hit pixel. Any address is generated automatically using combinations of NAND or NOR gates and buffers, outputs of which can be put in the high impedance state. The actual generation of an address occurs when the HIT signal is looped after inversion as the Back signal. The looping of the HIT signal may be gated for example in a case when some delay is required in sending new data to the data acquisition system. The circuitry for gating is not shown in Fig. 7. Activation of the Back signal causes the information flow in the opposite direction through the cascaded branches that are alternately built of two NAND gates and one NOT gate or two NOR gates and one NOT gate. The system acts as a priority encoder selecting a pixel whose inXX signal has the lowest XX number among all pixels that have signaled being hit. In a given example only one pixel, i.e. this one that raised the in01 line to the logic state '1' has the a01 signal equal to the logic state '0'. Thus, this pixel knows that it address should be generated now. This pixel also knows that when it detects a rising edge on a global strobe signal, meaning *end of readout of a pixel* (RStrobe shown later), its inXX line should be deactivated, because its time for readout is over and the next pixel in the hierarchy should be serviced. Addresses of hit pixels are generated by a combinatorial logic that decodes internal states of the priority encoder. The binary number 000001 is generated that corresponds to the pixel that signaled a hit on the in01 line in the considered example.

The VIPIC1 chip can operate in two modes, i.e. a data readout with sparsification mode and an imaging mode. The data sparsification mode is the primary readout mode for the VIPIC1 chip and it is adapted to low levels of pixel occupancy. In the imaging mode, only contents of counters are read from all pixels and addresses are skipped. Individual radiation events can be counted in each pixel in both modes. The VIPIC1 chip is designed to function dead-timelessly in both modes of operation. Fitting the VIPIC1 pixels with counters that are only 5-bit long does not compromise lossless operation in the imaging mode. This is because the time required to send all data out from all pixels in the group is shorter than the time a working counter can be filled in with new hits. The maximum speed of counting is limited by the time the front-end needs to return to the baseline. At faster speeds, signal pile-up would cause counts to be missed. Sending pixel addresses off is not required in the imaging mode, thus the output word is shorter. Assuming a moderate

frequency of 100 MHz for the serializer clock, it can be calculated that 2000 bits can be sent off the chip every 20 µs. These 2000 bits are more than the total length of a record produced by one group of pixels in the imaging mode. Thus, assuming a maximum counting rate of 1 MHz does not cause pile-up, it can be concluded that a 5-bit counter will not overflow within quoted 20 µs, leading to the achievable rate of 50×10^3 frame/s in the imaging mode for the VIPIC1 device.

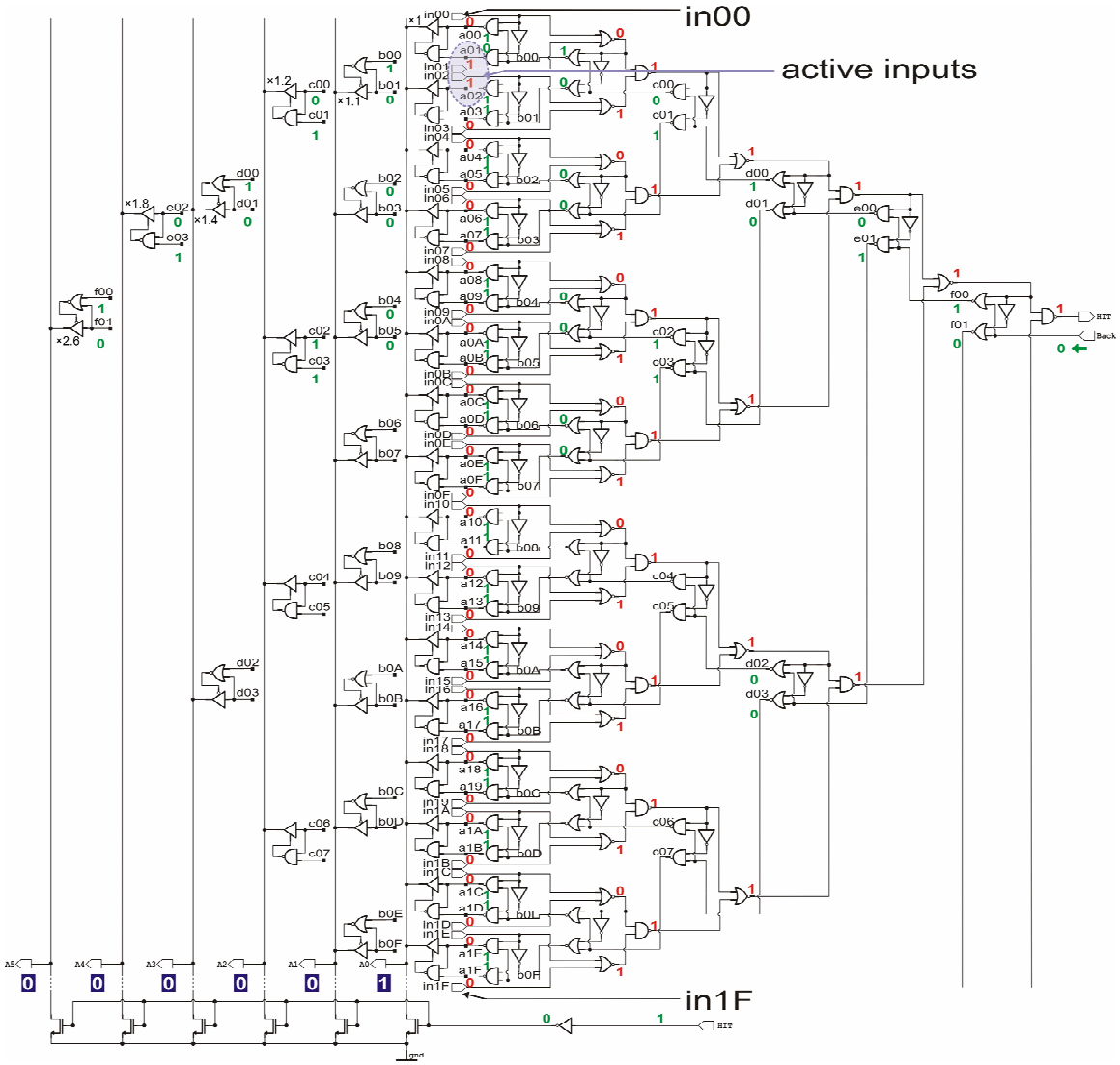

Fig. 7. Binary tree of the priority encoder used as the sparsifcation circuitry with automatic generation of an address of a hit pixel (shown for 32 pixels only).

C.Analog part of the VIPIC1 pixel

The analog part of the VIPIC1 pixel has a classical topology of a cascade composed of a charge integrating amplifier, a shaping filter and a discriminator. A block diagram of the analog part of the VIPIC1 pixel is shown in Fig. 8. The SPICE-type simulations yielded the following parameters of the front-end chain: charge-to-voltage gain equal to 52 µV/e^- in a pulse peak, noise ENC < 150 e^- rms (with capacitance seen at the input equal to 100 fF) and peaking time τ_p < 250 ns. The power consumption is 25 µW/pixel in the analog part [9]. The circuit contains some elements that were added to compare performances of the signal processing chain in configurations that can be later modified. An example of this is the presence of two charge sensitive amplifiers, i.e. CSA and CSA-replica in every pixel. The first of them accepts charge signals from a sensor, and the second amplifier is a replica of the first amplifier, but is not connected to a sensor.

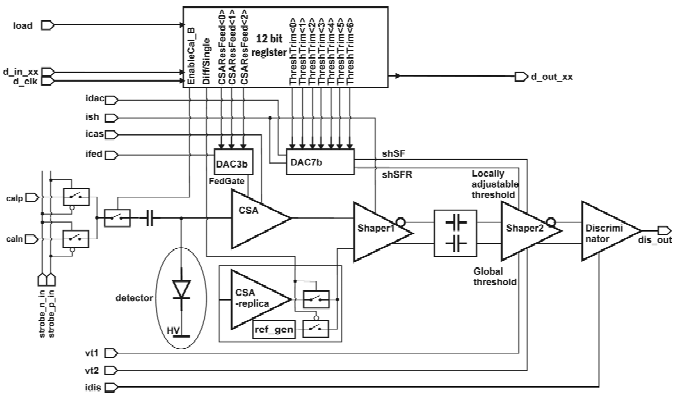

Fig. 8. Block diagram of the analog part of the VIPIC1 pixel.

Its role is to provide a reference signal for the shaping filter that handles differential signals in order to improve immunity of the chain for interferences.

The shaping filter has two stages: Shaper1 and Shaper2. They are AC-coupled to cancel any inter-stage offset propagation and to adjust time properties of the processed signals. Differential or single-ended operation of the front-end is selectable on a per pixel basis. The reference terminal of the shaping filter can be connected to the output of the replica amplifier, or a reference voltage level can be alternatively given to the shaping filter by the reference voltage generator. The time constant of both CSAs is adjusted simultaneously by voltage resulting from summing of an external reference with a value that is put out by a 3-bit DAC. The adjustment takes place individually in each pixel. The core of the CSA is based on a folded cascode configuration. The input transistor is a non-minimum channel length PMOS device that is polarized to work at the nominal drain current of 4.6 μA. The CSA works with an 8 fF capacitor (built as a MET3-MET4-MET5 sandwich structure). There is also a PMOS transistor with a long 5 μm channel operated in the linear region in the feedback path of the amplifier. The CSA uses two power supply voltages 1 V and 1.5 V from which the input transistor and the output part of the CSA are operated, respectively. The two-stage topology of the shaping filter allows voltage gain increase before the AC-coupled discriminator stage with lesser penalty of increased bias current for the desired bandwidth. Both stages use a differential pair loaded with cascaded, diode connected transistors. All transistors are biased in weak inversion thus gains of both stages are independent of the actual bias and of input offsets. The gain of the first stage is about -3 V/V. The DC path of the signal processing chain is cut at the input of the second stage of the shaping filter. Two 625 fF capacitors that are realized with transistors polarized with their channels in inversion provide coupling between the stages. They also introduce differentiation of a processed signal with a time constant defined by active resistors shunting the input of the second stage. The second stage adds a gain of less than -2 V/V and is the place, where the global threshold level for the discriminator is set. The threshold is set differentially by feeding voltage levels vt1 and vt2 to a chip from the outside. The discriminator threshold is additionally trimmable by a 7-bit precision differential current DAC on a per pixel basis. The discriminator threshold is trimmed by adjusting bias currents of two source followers coupling the second stage of the shaping filter to the discriminator. The discriminator consists of an operational transconductance amplifier that is followed by a current discriminator. The discriminator feeds its output to the digital part of the pixel. Other blocks that belong to the analog circuit network and which are located on the upper tier are a charge injection circuit, and an analog reference block.

D. Digital part of the VIPIC1 pixel

The digital part of the VIPIC1 pixel stores hits and feeds the resulting data to the sparsifier. It is composed of two logical entities. The first one is a single stage pipeline that relentlessly receives the hits in consecutive time frames and presents them to the sparifier at times of transition to every new time frame. This part of the digital circuit is shown in Fig. 9. The second unit is a set of two counters that are alternately selected to count events in consecutive time frames. The two counters with the circuitry controlling their operation and a timing diagram, providing explanation of their operation, are shown in Fig. 10. Succession of time frames is determined by the rising edges of the TS_Clk clock. The output of the discriminator is connected to the dis_in terminal of the digital block and the first change of a state from the logical level “low” to the logical level “high” in a current time frame results in setting the first flip-flop of the pipeline high. This flip-flop is called “waiting room” in Fig. 10. When it is set high, it means that at least one hit was registered in a given time frame by the pixel and it needs to be read out. The discriminator signal is gated before it gets to the waiting room flip-flop. The state of this flip-flop can be overwritten, regardless of occurrence of hits, by having it always set high if the *set pixel* bit is programmed high or conversely by having it always set low if the *reset pixel* bit is programmed high and the *set pixel* bit is programmed low at the same time.

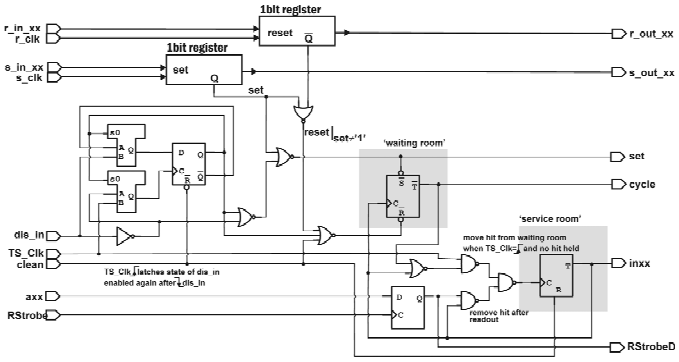

Fig. 9. Block diagram of the digital part of the VIPIC1 pixel.

The discriminator signal is also gated by a circuit, which prevents false registration of hits at the transition between two time frames. The circuit for the implementation of this function uses one d-type flip-flop and two 2-to-1 multiplexors. The rising edge of the TS_Clk (new time frame) latches the state of the discriminator input, present at this moment, in the d-type flip-flop. If the Q output changes to the logic state high, it means that the discriminator provided information beforehand about a hit and this hit should not be counted in a new time frame for the second time. The flip-flop is brought back to its ground level with the falling edge of the discriminator. If the Q output stays at the logic level low, it means that there was no hit occurring at the moment of switching between time frames and gating is not happening.

A rising edge of the TS_Clk clock shifts the content of the waiting room flip-flop to another flip-flop that interfaces to the sparsifier. This second flip-flop is called “service room”. If the waiting room contained a hit, shifting to the service room should result in its removal from the waiting room. This is achieved by looping the output of the service room flip-flop back to the clock input of the waiting room flip-flop. Thus the removal of a hit from the waiting room occurs asynchronously with the lowest achievable delay. The process is also reliable, because it is conditioned by having the hit information shifted to the service room. Removal of an old hit from the waiting room does not conflict with acceptance of a new hit should

such a circumstance occur. Any transient state in the flip-flop caused by feeding the hit removal edge to the clock input is shorter than duration of the discriminator signal in all practical cases, and a new hit can be registered should transferring of the information in the pipeline coincide. Both the waiting room and service room flip-flops are toggle flip-flops.

The service room generates the inXX signal that is fed to the sparsifier and receives the acknowledge aXX signal from the sparsifier. Activation of the aXX signal indicates that this pixel is selected for the readout by the sparsifier and its address and its content of the counter are sent down to the serializer. As it can be seen in the block diagram from Fig. 9, a rising edge on the RStrobe line cleans the service room and moves the readout to the next pixel to be indicated by the sparsifier by activation of another aXX line.

Programming of either the *set pixel* or *reset pixel* bit alters the way a pixel participates in the readout process. The *set pixel* bit in the high state causes a pixel to signal its occupancy to the sparsifier at the start of a new time frame. This setting forces reading out a given pixel irrespectively of its counter, which can be even empty. Counting of pulses coming from a discriminator works normally, unless a pixel has the *reset bit* set high. Setting the *reset pixel* bit to the high state eliminates a given pixel from being a part of the readout queue permanently. The *set pixel* bit has higher priority to the *reset pixel* bit. Setting the *set pixel* bit to the high state in all pixels allows operation of VIPIC1 in an imaging mode, in which the actual role of sparsification is given up. Serializers shift out first the contents of in-pixels counters. Issuing the RStrobe pulse during sending a record (counters and addresses) stops the transmission from a given pixel and moves the readout process to the next pixel. Acting on the RStrobe signal before bits of addresses are sent for all pixels allows the imaging mode. Having all pixels with their *set pixel* bits set leads to unambiguous readout. Use of the *set pixel* and *reset pixel* bits allows also Region-of-Interest (RoI) mode as an extension of the imaging operation mode.

Settings of the feedback resistance, switching on and off differential operation of the input stage and correcting the effective discriminator threshold can be achieved by programming serially the chip configuration register.

A block diagram of the counters section with a simple logic circuit, allowing alternating the counters, is shown in Fig. 10. Alternating of counters takes place at rising edges of TS_Clk.

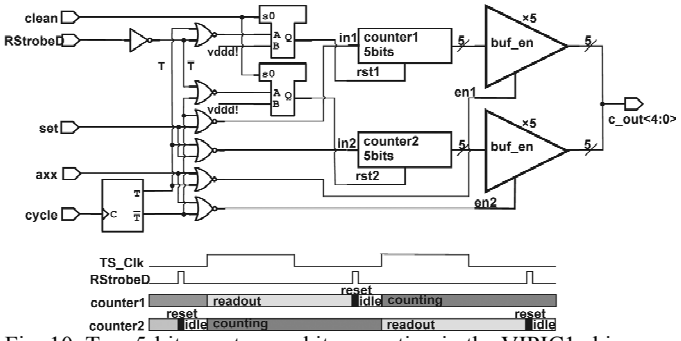

Fig. 10. Two 5-bit counters and its operation in the VIPIC1 chip.

However, in order to limit power consumption due to switching activity, the counters are cycled for a new time frame only when they registered hits in a previous cycle. Issuance of the RStrobe signal results in returning the buffers outputs, shown in Fig. 10, in high impedance. The counters are simple ripple counters without overflow protection.

E. Summary of design features

The analog and digital part of the pixel contains about 280 and 1400 transistors, respectively. The size of the whole chip is 5.6×6.3 mm^2, while its total active area, equal to the matrix of 64×64 pixels with a pitch of 80 μm, is 5120×5120 μm^2.The main design features of VIPIC1 are summarized in Table I.

TABLE I. MAIN FEATURES OF THE VIPIC1 CHIP

X-ray detection (8 keV) with Si pixel detector
64×64 pixels, pixel size: 80×80 μm^2
Separate analog (280 transistors) and digital tiers (1400 transistors)
Active area: 5120×5120 μm^2, chip: 6.3×5.5 mm^2 (6.3×5.6 mm^2)
Power consumption: 25 μW/analog pixel
CSA: noise ENC < 150 e$^-$, τ_p < 250 ns, gain 115 mV / 8 keV, C_{feed}=8fF, single threshold for discriminator
Trim DAC/pixel for offset corrections: 3 bits CSA feedback, 7 bits discriminator threshold
Permanent *pixel set* and permanent *pixel reset* bit per pixel
Test charge injection circuitry: C_{inj}=1.7 fF
Single ended or differential configuration of the front-end
Readout modes: a) sparsified, binary readout (time slicing mode), b) imaging binary readout mode (5 bit signal depth)
Dead-timeless and trigger-less operation in both readout modes
Sparsification: priority encoder based sparsification circuitry
16 parallel serial LVDS output lines (16 groups of 4×64 pixels)
Two 5 bit counters per pixel for recording multiple hits per time frame (useable in the imaging mode)
Frame readout at 100 MHz serial readout clock
- 160 ns / hit pixel in sparsified time slicing mode
- 50×10^3 frame/s in imaging mode (5 bit counting)

IV. TESTS OF VIPIC1

Test results are presented for the chips obtained from dicing of two 3D stacked wafers that were delivered in June 2012. There was one 3D wafer bonded using Cu-Cu thermo-compression and one bonded using Cu-based oxide-oxide bonding. Each 3D wafer yielded five good dies. The tests were carried out for chips before connection to sensors. Bonding to sensors was planned for later.

A. Tests of the sparsification and of the digital readout

The goal for testing of the sparsification engine and of the digital readout was to verify correctness of operation of the whole digital readout chain that begins at registration of hits in pixels and ends at reading out addresses and contents of counters of pixels storing hits.

Programming of *set pixel* and *reset pixel* bits leads to deterministic activation of pixels for readout. Addresses of "hit pixels", as generated by a tested chip, could be compared with addresses expected according to programmed patterns independently of any activity in the analog parts. An example of a reconstructed ring pattern that was programmed in a tested VIPIC1 chip is shown in Fig. 11. The rings were

obtained from pixel addresses reported in the readout process, while the analog front-end was switched off for the data presented in Fig. 11a and the analog front-end was switched on and the discriminator levels were being adjusted for accepting noise hits for the data shown in Fig. 11b. All pixels whose addresses formed a ring were read out because their *set pixel* bits were set as active. But the counters held zero values (white) in the first case. The values were non-zero in the second case. Threshold scans were performed while readouts were repeated multiple times. New contents of the counters were added, after each readout, to the sum that was obtained from the previous steps. Following that, a new threshold level was applied to the discriminators and next readout was executed. As a result, every pixel could be tested on the border of yet to be trimmed discriminator thresholds. Thus, Fig. 11b gives information about a share of pixels correctly registering the pulses originating in the analog chain, which is similar to the registering of photons hits. It is noticeable that all pixels were responding by registering noise hits. The range is from 0 to 777 counts, which is encoded with black and white color in Fig. 11, respectively.

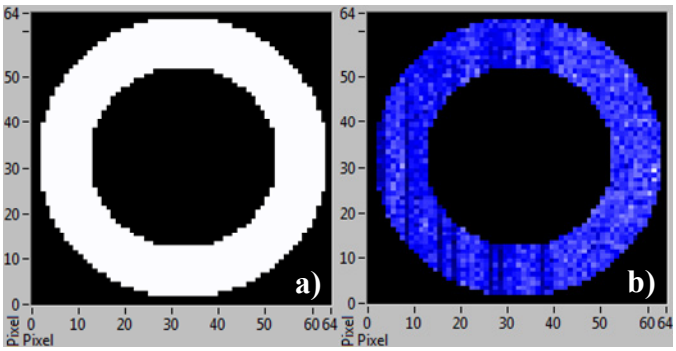

Fig. 11. Reconstructed pattern of a mask that has been programmed by *set pixel* and *reset pixel* bits, obtained from the pixel addresses as reported in the data readout process from the tested VIPIC1 chip, including contents of counters for pixels that were set; a) with analog front-end switched off, b) with analog front-end switched on and with the discriminator level adjusted for accepting noise hits.

Estimation of the fraction of pixels responding by submitting their addresses for readout needed to be done in an unbiased way, i.e. without setting the *set pixel* bit. This experiment was done by moving the discriminator threshold and tracking the results. The outcome is shown in Fig. 12. Should a given address have appeared in the output stream it was marked on the left y-axis of the plot. Contents of counters were marked on the right y-axis. Data used for the graph in Fig. 12 were collected in several stages. Due to not applying threshold trimming in this phase yet, discriminators generated pulses stimulating counters at threshold settings that were dissimilar from pixel to pixel. Thus, a following procedure was applied in order to obtain the graph from Fig. 12: an address of a pixel was marked on the chart if it appeared in the output stream for at least one threshold level applied. Values of counters that were read out were indicated also on the graph. Because only one value could be plotted on the graph, always the highest value that appeared throughout the experiment was chosen. Counters could overflow, so the meaning of the data shown in Fig. 12 does only have qualitative meaning and demonstrates, first, the share of pixels that are active in the chip and, second, ability of registering multiple counts, viz. noise hits. It can be concluded that all the pixels from the tested chip were active.

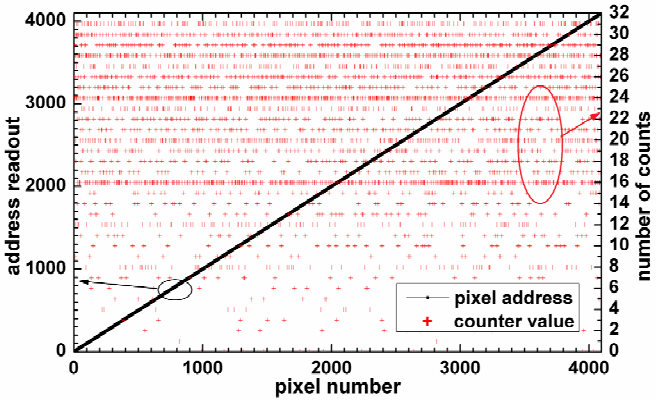

Fig. 12. Addresses of pixels that show up in a scan of addresses and values stored in counters that are read out in scans of discrimination thresholds marked correspondingly to reported addresses.

B. Tests of the range of threshold correction

Spreads of threshold offsets of discriminators can be corrected by the pixel DACs. The static offset levels are equalized by loading code words into the DACs. In order to verify responsiveness of DACs and the corrections range, the code words were loaded serially into a shift register that passes through all pixels. The range of threshold trimming was tested by loading the registers with minimum (1111111) and maximum (0000000) values and measuring the resulting threshold levels individually for every pixel. For both settings of DACs registers, threshold scans were performed by varying global discriminators threshold and registering noise counts. The measurements were performed at the nominal bias current for DACs of 10 µA. An exemplary result of these tests is shown in Fig. 13. Two distinctive histogram groups, containing entries correspondingly for two settings of DACs, can be distinguished. The separation between two peaks corresponds to the range of threshold corrections equal to about 100 mV, while FWHW of the threshold spread of discriminators is about 50 mV in both positions.

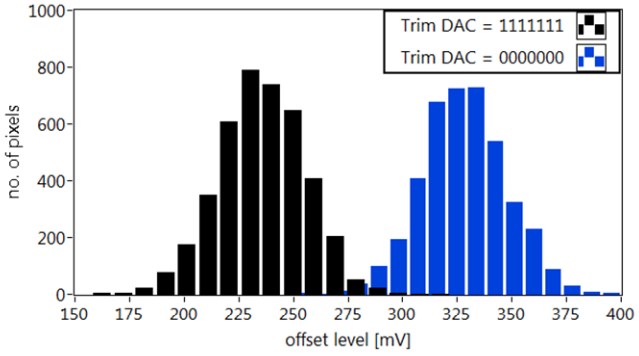

Fig. 13. Distributions of discriminator threshold levels for two extreme settings of the trimming DACs (0 and 127).

All pixels seemed fully responding to loading of the DACs values. This allowed concluding that seven differential connections between the digital and analog tiers, related to

DACs, were functional. Reducing of spreads of discriminator thresholds suffered from a glitch due to lack of complete control over the configuration shift register in the chip and due to the short counters. Nevertheless, about a fivefold reduction of spreads was achieved in a simple way by setting the DACs.

C. Tests of the analog chain: noise and gain

Measurements of output noise could be achieved individually for every pixel by scanning discriminator threshold levels at a high level of granularity and registering rates of noise hits. However, referring the measured levels of noise to the input of the CSA is not straightforward without knowing the genuine gain of the system. An internal calibration pulse with externally controlled amplitude can be used as a source of input pulses for measuring the gain for a VIPIC1 chip. This method, although imprecise, as the designed value of the test charge injection capacitance of 1.7 fF may be significantly different in the fabricated device, is the only method available without a bonded detector on which mono-energetic X-rays could be flashed. Thus, the ENC values were first calculated using theoretical gain values, i.e. as yielded by circuit simulations. Later, the results obtained in such a way were referred to those in which measured gain values were used.

The basic procedure for noise estimation relies on varying the discriminator threshold voltage and reading the number of pulses at the discriminator output occurring in a given time window. The counters are only 5-bit long in a VIPIC1 chip and therefore each step of the threshold scan was repeated 1000 times and the counts were being summed up in software to achieve statistically representative numbers of counts.

The pixel pitch in a VIPIC1 chip is 80 µm in both directions. However, the VIPIC1 chips from the current lot had an array of 32×38 pads laid out with a pitch of 100 µm in both directions and redistributed over the TSV interface in the center part of a device. This 80 µm to 100 µm pitch adaptation required skipping every 5th channel in *x* and *y* directions. The pads were prepared for attaching VIPIC1 to a baby sensor with 100 µm pitch using classical Sn-Pb bump-bonding technology. At a later time bonding to an 80 µm pitch sensor using the DBI® bonding process [2] is planned.

Charts with distributions of pixels with measured output noise are shown in Fig. 14. The measurements were performed at the nominal current of the input transistor I_{nom}=30 µA and for the CSA replica switched off. The pattern of 8×10 groups with typically 16 pixels separated by dark vertical and horizontal lines is visible. Those groups contain channels exhibiting higher noise. They can be identified as pixels with bump bonding pads. The pads represented additional loads and might act as antennas due to their size on channels to which they were added. The scale on Fig. 14a is such that black represents the 0 mV rms level and white level corresponds to 10 mV rms. The mean value of noise is 2.8 and 5.1 mV for pixels without pads and with pads, respectively. The chart, shown in Fig. 14b, has its scale changed in order to expose better pixels for which an atypical behavior in the noise measurements was observed. There are about 40 randomly distributed pixels (~1%) standing out. The origin of behavior of these pixels remains unclear. However, the number of these pixels is small. The distributions of discriminators threshold levels have been found slightly shifting with time. Such fluctuations may signify some problems of reliability of contacts for DACs lines on the bonding interface for this group of pixels.

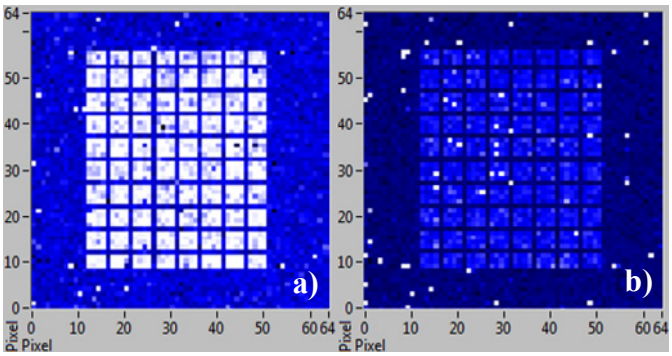

Fig. 14. A) Map of pixels with noise (scale: black – 0 mV rms, white – 10 mV rms), a) map of pixels with noise exposing pixels, marked with white, with atypical behavior in the noise measurement (dark lines are pixels without pads in both charts).

Gain and noise values obtained in circuit simulations are shown in Table II. The values are listed there as a function of the detector capacitance C_{DET}, bias current of the input transistor in the CSA and for both configurations of the CSA, i.e. with the replica switched off and on.

TABLE II. SIMULATED GAIN AND NOISE AS A FUNCTION OF DETECTOR CAPACITANCE AND INPUT TRANSISTOR BIAS CURRENT (CSA REPLICA OFF/ON)

C_{DET}	Gain (µV/e$^-$) Noise (e$^-$) @ I_{nom}/2	Gain (µV/e$^-$) Noise (e$^-$) @ I_{nom}	Gain (µV/e$^-$) Noise (e$^-$) @ I_{nom} ×1.5
0 fF	55.8 / 55.1	62.4 / 61.8	64.5 / 64.1
	80 / 99	63 / 77	55 / 66
100 fF	43.3 / 43.2	52.7 / 52.6	56.6 / 56.5
	116 / 140	90.5 / 104	80 / 89
200 fF	36.3 / 36.3	46.3 / 46.3	50.9 / 50.9
	159 / 186	125 / 138	111 / 118

As expected, noise values in the configuration with the CSA replica on are larger compared to the configuration with this part off. However, the difference is not exceeding 17% because of some noise contribution comes from the stages following the CSA.

Operation of the analog processing chain was tested by injecting varied test charges using the internal calibration system. CSA and other blocks in the chain showed proper responses. Estimated gain values as a function of the input transistor bias current for channels with and without pads are given in Table III.

TABLE III. GAIN AS A FUNCTION OF INPUT TRANSISTOR BIAS CURRENT (CSA REPLICA OFF) FOR CHANNELS WITH AND WITHOUT PADS

PADS	Gain (µV/e$^-$) @ I_{nom}/2	Gain (µV/e$^-$) @ I_{nom}	Gain (µV/e$^-$) @ I_{nom} ×1.5
YES	34.5 ±4.9	40.7±5.5	44.1±5.1
NO	34.7±5.0	40.9±5.5	43.6±4.6

The values were calculated assuming the designed 1.7 fF value of the injection capacitance. The measured gains are up to 30% lower compared to simulations. This measurement however can be explained by not knowing the actual value of the capacitance, through which test charges were injected. The gain and noise were measured following the procedure, in which an externally supplied threshold voltage was stepped with small strides, and multiple charge injections and amplitudes at every threshold level. There were 100 repetitions of readout cycles for every threshold level and 10 charge injections were performed for every repetition. Thus, the summed counts would be equal to 1000 for a threshold level set between the noise floor and maximum signal amplitude. For threshold levels set below the noise floor, the counts from charge injections were supplemented by the noise hits. Longer time frame was used to accommodate 10 injections in each. Thus, overflowing of the counters due to the excess of noise hits was observed, but it was not critical for applying the procedure. An example of the results is shown in Fig. 15. Studies were carried out for three voltage steps, i.e. 100, 200 and 300 mV, resulting in three strengths of charge signals injected. The level of a discriminator threshold, for which a peak of noise counts is achieved, is approximately 130 mV for an analyzed pixel. Actual peak amplitude cannot be read in the chart due to the overflow of a counter. The width of the distribution part with noise entries is larger for larger amplitudes of injected signals. The explanation of this finding may derive the greater the number of counts from cross-talks that are present because of injections occurring to all channels simultaneously.

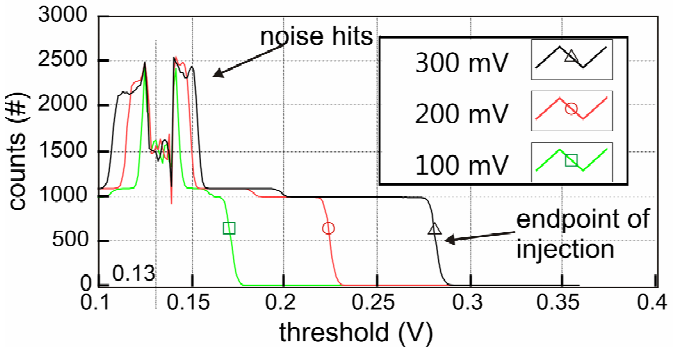

Fig. 15. Calibration pulse responses.

The noise can be estimated in two ways from the chart, shown in Fig. 15. Estimations can be done, first, directly from the width of the part with noise entries at no injection, and second, from the width of differentiated endpoints of injection distributions. The results of noise estimations are given in Table IV for channels with and without pads for varied input transistor bias currents and for the replica in the off state. Noise values reported in Table IV were calculated with gains from Table III. A histogram of noise for the VIPIC1 chip at the nominal bias current in the input transistor and the replica amplifier in the off state is given in Fig. 16. A carried out estimation of noise for the system with the replica amplifier switched on yielded about 12% to 16% larger noise for pixels with pads at the largest and smallest bias current in the input transistor, respectively. Some improvements in noise performance were observed on pixels without pads. However, overall the presence of the replica CSA amplifier has not shown any improvements, but it was increasing power consumption in the pixel. All the tests were performed for chips that were operated in dead-timeless readout.

TABLE IV. NOISE AS A FUNCTION OF INPUT TRANSISTOR BIAS CURRENT (CSA REPLICA OFF) FOR CHANNELS WITH AND WITHOUT PADS

PADS	Noise (e^-) @ $I_{nom}/2$	Noise (e^-) @ I_{nom}	Noise (e^-) @ $I_{nom} \times 1.5$
YES	132±27.3	120±21.4	117±20.7
NO	82±17.6	64±13.4	56±11.2

V. CONCLUSIONS

The earliest results of testing of the first 3D integrated pixelated chip for the photon science are very encouraging. Proper operation of both analog and digital blocks and the communication between them with more than 30 bonding interface terminal per pixel and more than 120k in the whole matrix and TSVs carried signals to the tiers were proven. The tests have showed that performance of the chip corresponds to the design goals. Unbiased measurements of genuine parameters, like: amplification gain and noise are possible only in tests with a sensors attached to the readout chip and using X-rays. These tests are underway due to the overall positive message from the test results presented in this paper.

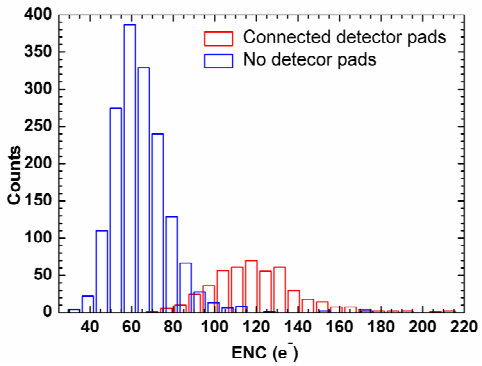

Fig. 16. Distribution of noise for VIPIC1 at nominal bias in the input transistor and with the CSA replica switched off.

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