IOPscience iopscience.iop.org

FERMILAB-CONF-12-814-PPD

Home Search Collections Journals About Contact us My IOPscience

Combining the two 3Ds

This article has been downloaded from IOPscience. Please scroll down to see the full text article.

2012 JINST 7 C12010

(http://iopscience.iop.org/1748-0221/7/12/C12010)

View the table of contents for this issue, or go to the journal homepage for more

Download details:
IP Address: 131.225.23.169
The article was downloaded on 01/08/2013 at 19:58

Please note that terms and conditions apply.

Operated by Fermi Research Alliance, LLC under Contract No. De-AC02-07CH11359 with the United States Department of Energy.

FERMILAB-CONF-12-814-PPD

*J*inst

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *June 25, 2012*
ACCEPTED: *October 15, 2012*
PUBLISHED: *December 10, 2012*

WIT2012 — WORKSHOP ON INTELLIGENT TRACKERS,
3–5 MAY 2012,
INFN PISA, ITALY

Combining the two 3Ds

R. Lipton,[a,1] **G. Deptuch,**[a] **U. Heintz,**[b] **M. Johnson,**[a] **C. Kenney,**[d] **M. Narian,**[b] **S. Parker,**[e] **I. Planell-Mendez,**[c] **E. Sawyer,**[c] **A. Shenai,**[a] **L. Spiegel,**[a] **J. Thom**[c] **and Z. Ye**[a]

[a]*Fermi National Accelerator Laboratory,*
P.O. Box 500, Batavia, IL U.S.A.
[b]*Department of Physics, Brown University,*
Box 1843, Providence, RI U.S.A.
[c]*Department of Physics, Cornell University,*
109 Clark Hall, East Avenue, Ithaca, NY U.S.A.
[d]*SLAC National Accelerator Laboratory,*
2575 Sand Hill Road, Menlo Park, CA U.S.A.
[e]*Department of Physics and Astronomy, University of Hawai'i at Manoa,*
2505 Correa Rd., WAT 232 Honolulu, HI U.S.A.

E-mail: lipton@fnal.gov

ABSTRACT: We describe a project to demonstrate fully active sensor/readout chip tiles which can be assembled into large area arrays with good yield and minimal dead area. Such tiles can be used as building blocks for next generation trackers, such as the tracking trigger system for CMS in LHC, or for precise, low mass pixelated sensors.

KEYWORDS: Electronic detector readout concepts (solid-state); Trigger concepts and systems (hardware and software); Modular electronics

[1]Corresponding author.

© 2012 IOP Publishing Ltd and Sissa Medialab srl

doi:10.1088/1748-0221/7/12/C12010

Operated by Fermi Research Alliance, LLC under Contract No. De-AC02-07CH11359 with the United States Department of Energy.

2012 JINST 7 C12010

Contents

1 Introduction **1**

2 3D circuits **2**
2.1 Active edge sensors 3
2.2 Oxide bonding 3

3 FPIX studies **3**

4 Demonstration project **4**
4.1 Sensor design and simulation 4
4.2 Active edge assembly 5

5 Prospects **5**

2012 JINST 7 C12010

1 Introduction

In the next generation of collider experiments detectors will be challenged by unprecedented luminosity and data volumes. Several talks at this conference have discussed the application of the next generation of LHC trackers to level 1 and 2 triggering [1]. Such a detector needs to have the ability to form clusters, correlate clusters in adjacent layers to filter out hits related to low momentum tracks, and send data out at 40 MHz. Pixelization is crucial to provide the z resolution necessary to isolate the primary vertex of interest from the hundreds of other interactions in the beam crossing.

To achieve this we will need to build large area arrays (100's of meter^2) of highly pixelated detectors with minimal dead area and at reasonable cost. Table 1 summarizes current and projected costs and yields of various technologies. In the past pixel sensor arrays have been limited in the module area by:

1. Space needed at the edges of the detectors to reduce the field near the damaged dicing cut regions. These regions act as charge emitters and can cause unacceptably large currents in the edge strips.

2. Die size of the Readout Integrated Circuit (ROIC), determined by the die yield and reticule area.

3. The need to provide edge locations for wire bonds for connection to the ROIC.

The development of active edge sensors by S. Parker, C. Kenney and collaborators has addressed the first problem [2–4]. Recent work on the large area FEI4 chip [5] has shown that a large pixel chip can be produced with good yield. Processes related to 3D electronics can solve the third problem. Combining all three in a wafer scale process can produce active tiles which can be integrated

Table 1. Current and projected costs and yields for sensor/readout integration technologies.

Component	Current or projected cost	Yield	Comment
Readout IC	$8/cm^2,[1]	65–70% [6]	Current 3D wafer cost and FEI4 prototype yield
Active Edge Sensors	$53/cm^2	≈90%	Current cost for prototype 150 mm wafers
Silicon Strip Sensors	$10/cm^2	≈100%	CMS tracker costs
Bump bonding (2007)	$213/cm^2	98% [7]	CMS forward pixel costs Yield ≡<20 bad bumps/chip
Bump bonding (2012)	$62/cm^2	–	CMS forward pixel upgrade
Wafer scale DBI bonding	$0.04/cm^2	≈90%	Projected by Yole Development [8] for high volume production
Target Costs (2020s)	$10/cm^2	80%	Assuming 200 mm sensor wafers and batch active edge process

into large modules with high yield and relatively low cost. The goal of this work is to combine active edge technology with 3D electronics and oxide bonding to demonstrate the production of fully active tiles. Using such tiles, large area pixelated modules can be assembled with known good integrated sensor/readout die and with large pitch backside bump bond interconnects. All fine pitch bonds to the sensor are made using wafer to wafer oxide bonding.

2 3D circuits

3D circuitry is the generic term for a set of technologies, including wafer bonding, thinning, and interconnect, which allows vertical interconnection of multiple layers of CMOS electronics [9, 10]. 3D interconnects have the advantage of reducing inductance and capacitance while increasing circuit density and allowing the integration of heterogeneous device types. In high energy physics 3D circuitry would allow us to directly integrate sensors and their readout electronics without the use of expensive and cumbersome fine pitch bump bonds.

We have explored three technologies for 3D devices. Our initial studies were with MIT-Lincoln Labs and used their 0.18 micron three-tier process. This process utilizes oxide bonding to join the tiers and vias are etched through the SOI buried oxide after the tiers are bonded. We developed a demonstration 3-tier ILC vertex chip (VIP) in the MIT-LL process [11]. We have also used the Ziptronix oxide bonding process with imbedded metal to mate BTeV FPiX ROIC wafers to sensors fabricated at MIT-Lincoln Labs. We have also sponsored a two-tier 0.13 micron CMOS 3D IC run with Tezzaron/Global Foundries [12]. That run encountered numerous difficulties [13]. A set of chips from the initial run has now been received with good 3D interconnects. Nine of eleven chips CMS trigger prototype (VICTR) chips tested so far function well. In addition 18 reprocessed backup wafers have been fabricated and will be 3D bonded by the end of 2012.

[1]Current cost for 0.18 micron CMOS wafers with through-siicon vias.

2012 JINST 7 C12010

2.1 Active edge sensors

Active edge sensors are an outgrowth of work done to develop 3D sensors, which provide good charge collection combined with radiation hardness. The technique utilizes a deep reactive ion etch of silicon to create a nearly vertical trench with smooth edges. The high quality of the trench wall avoids charge generation normally associated with saw-cut edges. The trenches are filled with doped polycrystalline silicon. The dopant is diffused into the surrounding single crystal silicon and annealed for activation. The dopant density gradient will make an electric field in the collection direction. These steps may be done at the same time for the other like-type electrodes. The depth of the doped silicon must be great enough so it is not depleted by the largest applied bias voltage. Mechanical integrity is maintained by bonding the sensor to a support wafer. The oxide bond also forms an etch stop for the trenching and singulation processes. In the case of an oxide bonded handle, in a silicon-on-insulator structure, the bond also forms an etch stop for subsequent trenching and singulation processes. An alternative active edge technology based on wafer cleaving and atomic layer deposition [14] has the prospect of achieving similar goals without the additional processing needed in the deep trench process. We have included non-trenched structures in our design to allow us to test this process as well.

2.2 Oxide bonding

Bonding of silicon wafers is a key enabling technology for nanotechnology, micromachining and 3D electronics. A variety of techniques have been developed, including adhesive bonding, metal eutectic bonding, and bonding based on the silicon oxide surface either grown or deposited on a wafer [15]. Oxide bonding has the advantages of being mechanically robust, chemically inert, and capable of withstanding the high temperatures typical of silicon processing.

The direct oxide bond [16] is formed by bringing together silicon wafers which have been planarzed and chemically treated to form a hydrophilic surface. When the wafers are brought together at room temperature a Van-Der-Walls bond forms between the hydrogen at the wafer surface. Further annealing above 150°C causes the formation of covalent hydrogen bonds at the surface and provides a substantial increase in bond strength. The Ziptronix DBI process imbeds nickel or copper in the planarized oxide surface. The metal forms an interconnect to a seed metal layer in the resulting oxide bonded wafers which can be used to build 3D interconnect structures [17]. Micron-sized dust particles present during the bonding process can produce millimeter-level bond voids. These unbonded areas limit the large area module yield and are a prime motivation for tile development. The DBI process can be used wafer to wafer or chip-to-wafer and has been demonstrated at pitches as low as 3 microns.

3 FPIX studies

We explored the use of the chip-to-wafer DBI process utilizing existing BTeV FPIX pixel readout wafers mated to sensors fabricated at MIT-Lincoln Labs. The sensors had p-on-n implantation on 50×400 micron pitch with a 50 micron deep active edge trench surrounding the active area. Sensors were DBI bonded to the readout wafer and thinned from 300 to 100 microns. This process did not utilize the active edge feature of the sensors. The resulting wafers were examined with Scanning

2012 JINST 7 C12010

Acoustic Microscopy (SAM) to verify bond integrity. The bonded die yield was 52% on one wafer and 81% on the second. This relatively low yield was attributed to the non-planarity of the sensor wafer. Yields for wafer-wafer bonds of planarized wafers are expected to be significantly higher.

For our tests, contact to the ground surface sensor backside was made by coating it with a indium-gallium eutectic. Noise was measured for both fully and partially bonded devices as measured by SAM. On the fully bonded devices the noise spectrum and laser scans indicated that all pixels were successfully bonded. The noise spectrum also shows minimal capacitance added by the DBI process [18]. Test beam exposure showed the expected resolution and efficiency. We also exposed both bonded and unbonded FPIX chips to 10 Mrad of Co^{60} radiation with similar results, indicating that the DBI process does not affect the radiation resistance of the chip and the DBI itself is not damaged by ionizing radiation. These tests led us to conclude that the DBI process is extremely promising as an advanced fine pitch interconnect between sensors and readout chips.

4 Demonstration project

To demonstrate the combined active edge and 3D electronics technologies we have launched a project to demonstrate reticule-sized active tiles with active edges. An active edge sensor wafer will be wafer bonded to a dummy readout assembly which will route analog signals from the sensor to bump bonds on the body of the chip. A 2×2 array of chips will be bump bonded to a circuit board which will bring the signals to a set of wire bond pads. The signals will then be bonded to an APV readout chip hybrid for beam and source tests.

4.1 Sensor design and simulation

Two sensor types have been included, corresponding to the 1 cm long strip and 1.25 mm short strip sensors envisioned in the CMS upgrade tracker design. Each sensor is 20120×16020 microns with strips on 100 micron pitch. All 320 channels (2×160 1 cm strips) on the long strip sensors are routed to bump bond pads through the dummy readout chip. The short strip sensors have a combination of individual short strips and larger ganged regions routed to the same 320 pads. Contacts are arranged so that the same dummy readout chip connects to the long or short strip sensors. The 20 micron wide n-type charge collection strips are surrounded by 6 micron wide p-stops. All strips are DC coupled. Wafers are fabricated by VTT in an SOI stack with a 380 micron handle and 200 micron thick p-type sensor. Ten micron wide trenches are etched around the sensor and filled with doped polyslicon to provide the edge p-type diffusion. This is unlike the usual VTT angled edge implantation technique in which the trench in unfilled. The polysilicon fill will leave a more planar surface suitable for wafer bonding.

We simulated the fields in the sensor using the Silvaco set of TCAD tools. The region near the sensor edges have the largest local fields and are most subject to breakdown. A typical simulation is shown in figure 1. The p-stops for the long strips have a short edge which, because they terminate near the active edge, are the locations of the highest local fields. Our final design has a minimum gap between the trench and p-stop of 24 microns. There is a test reticule with varying gaps up to 44 microns.

2012 JINST 7 C12010

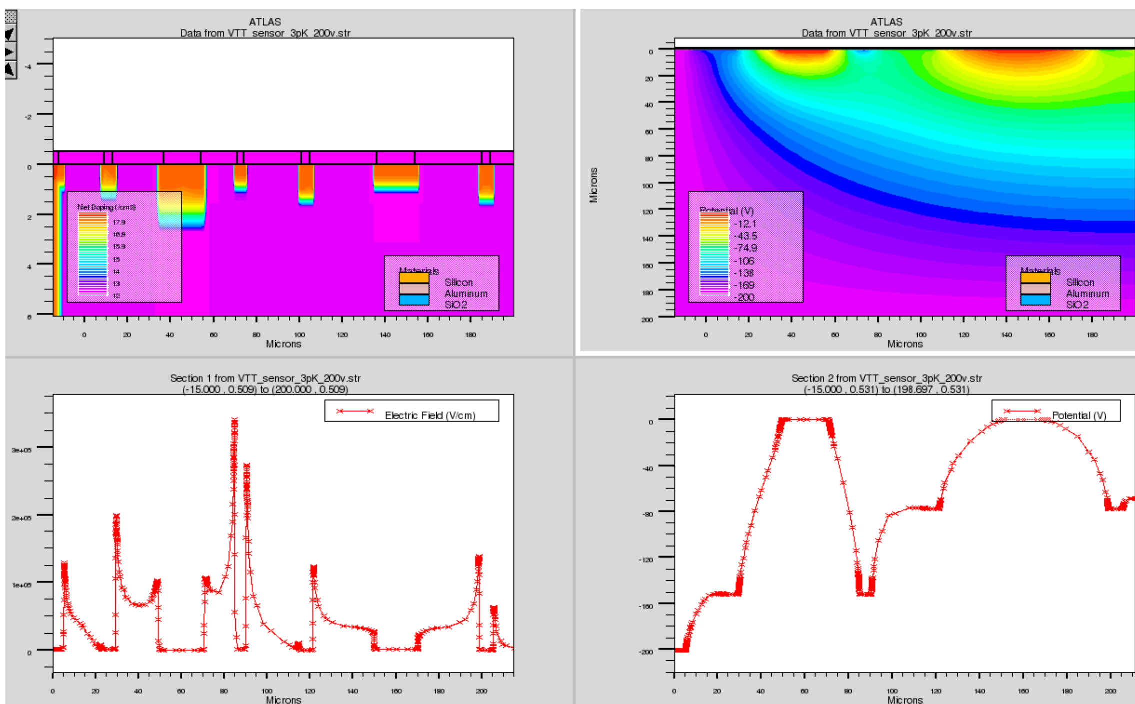

Figure 1. Results of TCAD simulation of the detector edge region at 200 V.

4.2 Active edge assembly

The trenched sensors will be DBI bonded to a dummy readout chip which will route the analog signals from the long and short strips to the top surface of the tile. A single metal layer is needed in addition to the seed metal used in the DBI process. The dummy chip needs to have planarity better than 0.3 microns to insure good wafer bond yields. This is accomplished by fabricating the wafer utilizing a "single damascene" process, where interconnects through the oxide insulating layers are fabricated by etching vertical contact holes, depositing tungsten by Chemical Vapor Deposition (CVD), and using a chemical-mechanical polish to attain a planar surface. The resulting tungsten plugs provide the connection to the bottom metallization.

The sensor wafer and the dummy readout wafer are then DBI bonded to form a 3D two-wafer stack (see figure 2). Contacts on the dummy wafer are exposed by grinding and etching away the dummy wafer silicon substrate and first layer of oxide to expose what would normally be the bottom surface of the readout pads. This surface is then patterned to provide sites for bump bond placement.

Finally the active die must be singulated. This is accomplished by etching the 6 microns of dummy wafer silicon and 3 microns of oxide, followed by an etch of the 200 microns of polysilicon filling the trench. The SOI oxide forms an etch stop in this process. The wafer is then attached to a temporary handle wafer and the original SOI handle is ground away, leaving isolated tiles.

5 Prospects

The ability to build large areas of pixelated arrays is crucial to future detectors such as the CMS central Track Trigger. We have described a plan to demonstrate pixelated tiles which have the

2012 JINST 7 C12010

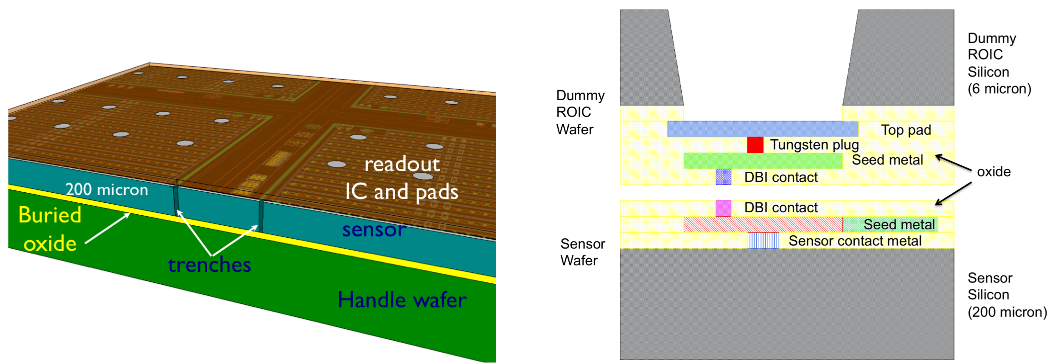

Figure 2. Left – 3D sketch showing a view of the wafer stack, including handle wafer, trenches, and the region between reticules. Right – Schematic view of the final stack with DBI contact layers and sensor and top contacts.

prospect of making such large area devices affordable. To complete this development sensor wafers which match the 8" diameter of the ROIC wafers are needed. Such wafers have been demonstrated in the SOI process by both Lapis/OK [19] and American Semiconductor. Further development will be needed to establish an active edge process in 8" technology.

References

[1] E. Salvati, *A level-1 track trigger for CMS with double stack detectors and long barrel approach*, 2012 *JINST* **7** C08005;
CMS collaboration, J. Hoff et al., *Readout Chip for an L1 Tracking Trigger Using Asynchronous Logic*, 2012 *JINST* **7** C08004.

[2] C.J. Kenney et al., *Active-edge planar radiation sensors*, *Nucl. Instrum. Meth.* **A 565** (2006) 272.

[3] C.J. Kenney, S.I. Parker and E. Walckiers, *Results from 3D sensors with wall electrodes: near-cell-edge sensitivity measurements as a preview of active-edge sensors*, *IEEE Trans. Nucl. Sci.* **48** (2001) 2405.

[4] C. Da Via et al., *3D active edge silicon detector tests with 120-GeV muons*, *IEEE Trans. Nucl. Sci.* **56** (2009) 505.

[5] M. Garcia-Sciveres et al., *TheFE-I4 pixel readout integrated circuit*, *Nucl. Instrum. Meth.* **A 636** (2011) 155.

[6] M. Barbero et al., *The FE-I4 pixel readout chip and the IBL module*, `PoS(Vertex 2011)038`.

[7] P. Merkel, *Experience with mass production bump bonding with outside vendors in the CMS FPIX project*, *Nucl. Instrum. Meth.* **A 582** (2007) 771.

[8] Solid State Technology, `http://www.electroiq.com/articles/sst/2008/10/ziptronix-joins-low-cost-quest-for-true-3d-ic.html`.

[9] IBM Journal of Research and Development, Volume 52 No. 6 (2008), Issue devoted to 3D technology.

[10] P. Garrou, C. Bower and P. Ramm, *Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits*, Wiley-VCH, (2008).

[11] G. Deptuch et al., *Vertically integrated pixel readout chip for high energy physics*, FERMILAB-CONF-11-020-PPD.

2012 JINST 7 C12010

[12] G. Deptuch et al., *Vertically Integrated Circuits at Fermilab*, *IEEE Trans. Nucl. Sci.* **57** (2010) 2178.

[13] R. Yarema, *The First Multiproject Wafer Run With Chartered/Tezzaron*, *Front End Electronics Meeting* Bergamo Italy, 2011 https://indico.cern.ch/getFile.py/access?contribId=34&sessionId=1&resId=1&materialId=slides&confId=122027.

[14] R. Mori et al., *Charge collection measurements on slim-edge microstrip detectors*, 2012 *JINST* **7** P05002.

[15] Q.-Y. Tong and U. Gösele *Semiconductor Wafer Bonding: Science and Technology*, first edition, The Electrochemical Society ed., Wiley-Interscience, (1998), [ISBN 978-0-471-57481-1].

[16] Q.-Y. Tong, E. Schmidt, U. Gösele and M. Reiche, *Hydrophobic silicon wafer bonding*, *App. Phys. Lett.* **64** (1994) 625.

[17] P. Enquist, G. Fountain, C. Petteway, A. Hollingsworth and H. Grady. *Low Cost of Ownership scalable copper Direct Bond Interconnect 3D IC technology for three dimensional integrated circuit applications*, in *IEEE International Conference on 3D System Integration*, San Francisco CA U.S.A., September 28-30 2009, [DOI]

[18] FERMILAB PIXEL R&D GROUP collaboration, Z. Ye, *Sensor/ROIC Integration using Oxide Bonding*, in proceedings of the *International Linear Collider Workshop (LCWS08 And ILC08)*, M. Barone, Y. Torun and N. Varelas eds., (2008), [arXiv:0902.2801].

[19] Y. Onuki et al., *SOI detector developments*, PoS(Vertex 2011)043.

2012 JINST 7 C12010