Vertically Integrated Circuit Development at Fermilab for Detectors

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ABSTRACT: Today vertically integrated circuits, (a. k. a. 3D integrated circuits) is a popular topic in many trade journals. The many advantages of these circuits have been described such as higher speed due to shorter trace lenghts, the ability to reduce cross talk by placing analog and digital circuits on different levels, higher circuit density without the going to smaller feature sizes, lower interconnect capacitance leading to lower power, reduced chip size, and different processing for the various layers to optimize performance. There are some added advantages specifically for MAPS (Monolithic Active Pixel Sensors) in High Energy Physics: four side buttable pixel arrays, 100% diode fill factor, the ability to move PMOS transistors out of the diode sensing layer, and a increase in channel density.

Fermilab began investigating 3D circuits in 2006. Many different bonding processes have been described for fabricating 3D circuits. [1] Fermilab has used three different processes to fabricate several circuits for specific applications in High Energy Physics and X-ray imaging. This paper covers some of the early 3D work at Fermilab and then moves to more recent activities. The major processes we have used are discussed and some of the problems encountered are described. An overview of pertinent 3D circuit designs is presented along with test results thus far.

KEYWORDS: Electronic detector readout concepts (solid state), VLSI circuits, Front-end electronics for detector readout

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1 Introduction

Three-dimensional integrated circuits were still in an early stage of development when we began exploring the possibilities of 3D circuits for HEP (High Energy Physics). Our initial motivation was for a compact pixel detector for the International Linear Collider. In addition we felt that there were many potential benefits in 3D for HEP including: finer pitch pixels, less massive on-detector circuits, higher localized functionality, an alternative to conventional bump bonding techniques, and development of 4 side buttable detector arrays. Also we thought that successful 3D integrated circuit design could lead to altogether new concepts for detector electronics.

Over the years we have found that it was a giant step to move from 2D circuit design to fabricated 3D chips. With every technique we have tried there has been a learning curve punctuated with delays due to design issues, fabrication issues, and assembly issues. Although success often seemed distant we have persevered and recently some positive results have been achieved.

2.0 Early history

Our first 3D design was a 3-tier chip fabricated at MIT Lincoln Labs in a 0.18 um SOI, 4 metal process. [1] The chip, which took only 10 week to design, was submitted in October 2006 but was not received back until February 2008.

Our MIT LL 3D design was based on requirements for the ILC pixel vertex detector. The goal was to have small pixels with a high degree of functionality built within the pixel and to build a low mass detector, which was a major requirement for the vertex detector. The first design was a complete pixel design with a 64 x 64 pixel array, 20 um pixels, a combination of digital and analog time stamping for high precision timing, data sparsification with high speed look ahead for the next hit pixel, and analog readout for each hit pixel. [2]

Due to the SOI process itself, and not the 3D fabrication, yield from the first submission was bad. A decision was made to resubmit in late 2008 with a much more conservative design with larger transistors and trace widths and change to a higher resolution all digital time stamp. Again this chip took well over a year to get back. However, the yield was much better and the concept of a 3D integrated circuit for the ILC was shown to be feasible.

3.0 Recent Activity

Future 3D design work was transferred to a commercial CMOS wafer foundry with the hope that delivery times would be better along with better analog circuit performance and radiation tolerance. The 3D process with small vias that we could access was Chartered Semiconductor (now Global Foundries) with Tezzaron TSV technology. [1] We decided to use the 0.13 um CMOS process and to use Tezzaron Semiconductor as our silicon broker.

Vias are inserted into wafers at Global Foundries in what is termed a via middle process. After transistors are formed, a blind via with passivated walls is inserted. The via is 1 um in diameter and 6 um deep. At the same time that tungsten connections are made to the transistors, the via is filled. The back end of line (BEOL) processing is then completed by adding up to 8 levels of copper. Our designs used only 6 levels of copper. The M6 level contains a very

regular array of octagon shaped pads in a hex pattern with a 4 or 5 um pitch. The octagon pads are used for Cu-Cu thermo compression bonding between wafers. In this assembly process, a 2-tier 3D chip is formed by a face-to-face bond between two wafers, which leaves the vias pointing into the substrate, away form the bond interface.

An international consortium was formed that submitted a 3D multi-project run to Global Foundries, through Tezzaron in May 2008. Several design revisions were necessary before final acceptance for the run. The multi-project run contained over 25 individual designs. One set of masks was used for a 2 tier 3D chip with wafer-to-wafer, face-to-face bonding. The frame was divided into 24 subreticles. The 12 subreticles on the left were for the top tier circuits and the 12 subreticles on the right were for the bottom tiers circuits. The subreticles for the top and bottom tiers are placed symmetrically about the centerline of the frame as shown in figure 1.

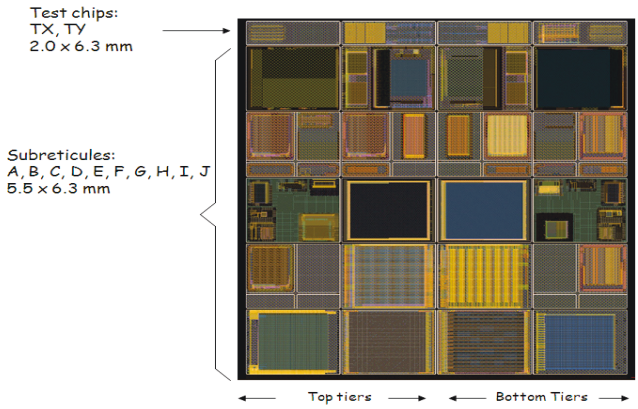

Figure 1- Multi-project run frame layout.

When one wafer is flipped on top of the other, one half of the 2 tier subreticles will have the top tier on top and the other half will have the bottom tier on top. The first case is considered a normal assembly and the latter is called a reversed assembly. Fermilab had 3 full chip designs called VICTR, VIPIC, and VIP2b in the frame. VICTR and VIPIC have been tested. Tests for the VIP2b (for the ILC vertex detector) are about to begin.

This being the first 3D multi-project run handled by Tezzaron from an outside group, numerous design, submission, and fabrication issues arose that caused painfully long delays [3]. One of the most frustrating delays was caused by the foundry not placing the frames on the wafer symmetrically about the centerline of the wafer. This misalignment of 1.2 mm made it impossible for the wafer bonder to properly align the wafers for bonding. Thus after much waiting and anticipation, the foundry had to refabricate all of the wafers.

After the batch of new wafers was received, the 3D bonding process began. The surface oxide on the wafers was recessed by 350 nm to expose the copper bond pads for Cu-Cu thermo compression bonding. Pairs of wafers were aligned face-to-face and bonded. After bonding, one of the pair of bonded wafers was thinned to about 12 um to expose the buried tungsten vias and back metallization was added for metal pads. Unfortunately, this bonding, which was done by a vendor in Arizona, did not go well.

The first 6 wafers that were bonded had very poor thermo compression bonds as found by acoustic imaging of the bonded wafers. After separating a pair of bonded wafers, chemical analysis showed that there was a few nm of carbon left on the wafer surface after cleaning, which inhibited bonding. After re-cleaning the remaining wafers, 6 more wafers were bonded

and one of the wafers was diced. It was then discovered that during the bonding process one the wafers had rotated slightly and shifted by a few microns causing shorts between the Cu-Cu bonding pads. At this point the remaining 16 wafers were sent to a vendor in Austria, which previously had demonstrated better alignment results. In addition, the bonding machine in Austria used a forming gas, which is known to provide better Cu-Cu bonds [4].

Initially 8 of the 16 wafers went through the bonding process in Austria using a forming gas. Various bond pressures were tried with unsatisfactory results. After studying the problem, it was hypothesized that over time the copper grain boundaries on the bonding pads had grown which makes Cu-Cu bonding more difficult. Our wafers had been out of the foundry for over a year. Tezzaron has now found other lots with similar problems. The remaining 8 wafers were returned to the U. S. for bond pad reconditioning and oxide recession, and then returned to Austria for bonding. The bonding of these last 8 wafers had other problems caused by the reconditioning. These last 4 bonded pairs had gas trapped between the wafers (possibly due to planarity issues) limiting the good bond areas. When these wafers were bonded, bonding occurred in the center of the wafer and a narrow band around the perimeter. The acoustic image in figure 2 shows good bonding as dark areas and bad bonding as light gray or white areas. This wafer was diced and parts from the center were used for testing.

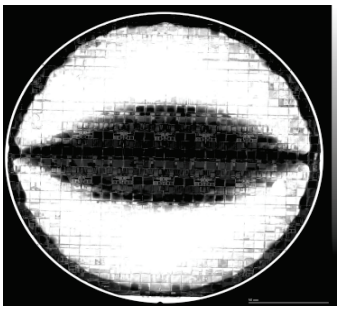

Figure 2 – Acoustic image of Tezzaron bonded wafers

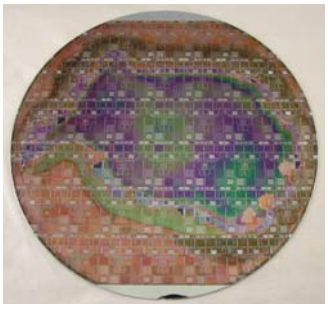

Figure 3 - Ziptronix bonded wafers

As an experiment it was decided to separate two of the poorly bonded wafers from Arizona and attempt DBI (Direct Bond Interconnect) bonding at Ziptronix. The DBI process is an oxide bond process for holding wafers together rather than a Cu-Cu bond process [5]. Once a wafer pair was separated, each wafer had to be processed to reduce/repair the wafer surface damage for the DBI process. A mask was made to add copper onto the existing bond pads Afterwards oxide was deposited and the wafers planarized to expose the new copper pads. The reconditioned wafers were then aligned and bonded. Although the bonding was not perfect, due to the history of the wafers, decent bonding was achieved in the center of the wafer as can be seen in figure 3. This wafer was also diced and parts selected for testing. Thus parts from both a Cu-Cu bonded wafer pair and DBI bonded pair were available in June 2012. These parts were used for testing by Fermilab and the consortium members from the multi-project run.

4.0 Vertically Integrated (3D) Circuits

VICTR (Vertically Integrated CMS Tracker)

The CMS experiment at High Luminosity LHC (HL-LHC) upgrade will require a track-based trigger at Level 1 to retain the ability to select and record rare physics events. A possible

solution to this problem is a hierarchical stub/track segment/track design where all operations are performed locally. This local design is enabled by 3D. The solution being studied here is based on cylindrical assemblies of parallel long and short strip sensors and ASICs that form track stubs. Figure 4 shows a stub cross section which is formed by a long (phi) strip detector, a 1 mm interposer, and a thinned ASIC with connections on top to the long strip detector and on the bottom to the short strip detector. A pair of stubs forms a tracklet which is used to determine track curvature.

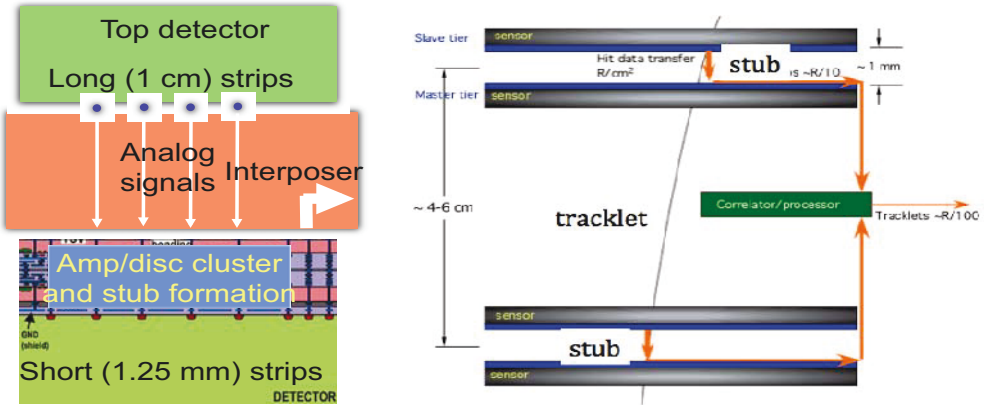

Figure 4–Left: track stub cross section. Right: tracklet formation

The track trigger will look for particles with Pt above 2Gev for data transfer, identify particles with Pt above 15-25 Gev (low curvature tracks), provide z resolution of about 1 mm set by short strips, and provide phi resolution provided by long strips. In this design, the ASIC is a 2 tier 3D chip called VICTR. VICTR is a demonstrator chip that looks for vertical coincidence of hits in a long (phi) strip and 1 of 5 short (z) detector strips, indicating a stiff track. More sophisticated logic will be added to later versions of VICTR. The chip accepts signals from 64 long strips and 5 short strips lying beneath and parallel to each of the 64 long strips. There is a programmable test input for every strip input, a fast OR output for top hits, bottom hits and coincidence hits. The chip was designed with "3D pads" in the top and bottom tiers so the VICTR chip can be tested with the top tier on top (normal) or the bottom tier on top (reversed) as shown in figure 5. Fig. 6 shows the signal processing for top and bottom hits along with coincidence output.

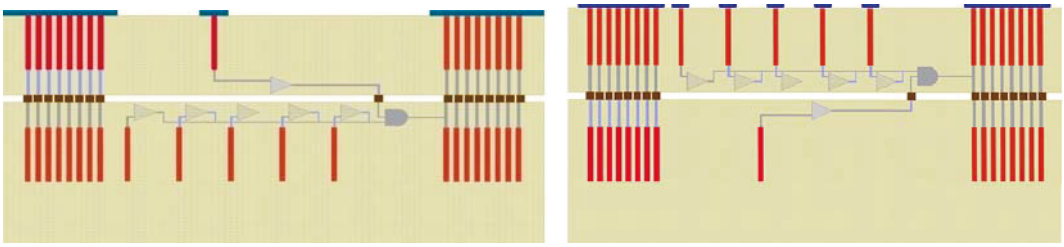

Figure 5–Left: bond pads on long strip side (normal). Right: pads on short strip side (reversed)

From figures 5 and 6 it can be seen that only 1 signal for each of the 64 long strips needs to pass from the top tier to the bottom tier. Each of the 64 connetions uses 4 copper bond pads for redunancy. Thus this chip has a very low interconnect density between tiers.

After visual inspection, several chips from the Tezzaron and Ziptronix wafers were selected for testing. Chips from both the Tezzaron and Ziptronix wafers were found to be fully functional.

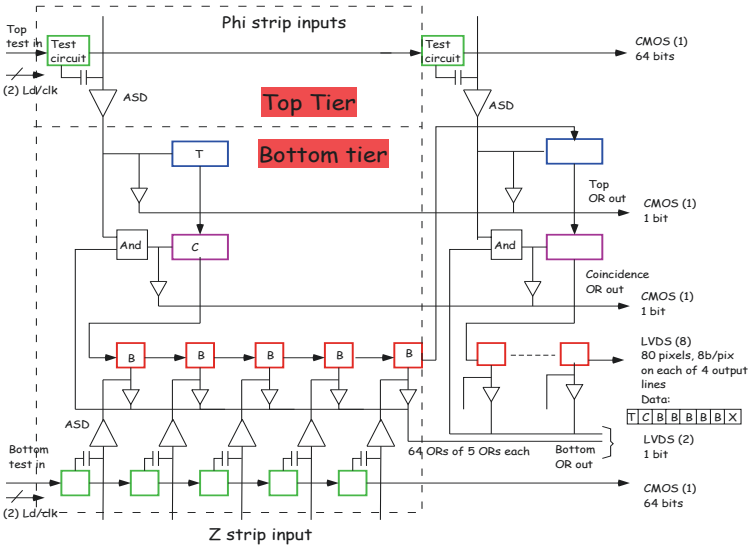

Figure 6 –Block diagram showing signal processing from one long strip on the the top tier and 5 short strips on the bottom tier with coincidence logic.

Numerous tests have been performed on these chips: 1) charge injection to the top and bottom tiers, 2) masking of hit channels, 3) common threshold adjustment for top and bottom ASD circuits, 4) readout of top, bottom, coincidence hits, 5) power dissipation, 6) threshold dispersion, and 7) noise (see figure 7).

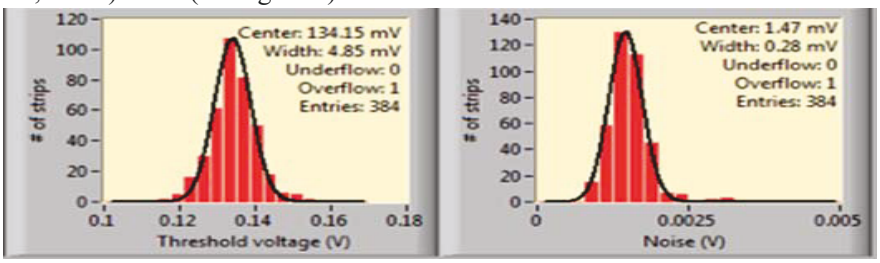

Figure 7 – Threshold and noise distribution for VICTR pixels

One test performed was to reduce the threshold for all the long and short strip detector ASDs until hits appeared, then look for coincidence hits. Results of this test is shown in figure 8 where the top 5 rows show random hits in green on the short bottom strips

Figure 8 – Hit and coincidence map for random hits on bottom and top input channels

The 6th row shows random hits on the long top strips, and the bottom row shows that if there is a a hit on any of the 5 short strips above a long strip **and** a hit on the long strip, a coincidence hit is correctly produced. The tests have been very encouraging thus far and plans are proceeding to bond the VICTR 3D chip to one detector and then to a second detector later. When this is completed the 3D readout chip will have been thinned to about 24um and have connections on both sides.

VIPIC (Vertically Integrated Photon Imaging Chip)

The second 3D chip recently received and tested is VIPIC. The VIPIC is designed for X-ray Photon Correlation Spectroscopy (XPCS), which uses a coherent X-ray source directed at a condensed matter system (gels, liquid crystals, biomaterials, metals, oxides, etc.) to generate a speckle pattern. [6] By recording the speckle pattern as a function of time, one can study the dynamics of the system. XPCS permits observation of very small feature sizes, works with non-transparent materials, and can be used to observe charge, spin, chemical and atomic structure behavior. VIPIC is a chip dedicated to time resolving spectroscopoy with photon counting capabilities. The chip is a 64 x 64 array of 80 um pixels, which is optimized for a photon energy of 8 kev. It has a binary readout, which means no energy information. The chip does not use a trigger and can be operated in 2 modes: 1) timed readout of hits and addresses at low occupancy (10 usec/frame for 100 photons/cm2/usec), 2) imaging mode where alternating 5 bit counters read out hits in each time slot with out addresses but still using sparsification. The chip is 5.5 x 6.3 mm and contains two 5 bit counters/pixel for dead timeless recording of multiple hits per time slice, a sparsified address generator [7], and 16 serial high speed LVDS output lines where each serial line takes care of 256 pixels. Pixel address generation occurs in 5 nsec regardless of hit pixel location. The chip is implemented as a 2 tier 3D ASIC with separate tiers for analog and digital circuitry. Figure 9 shows an overview of the chip organization and how the pixel analog and digital circuitry is split between the two tiers. Programming DACs with differential outputs and control lines are located on the digital tier. Thus 25 lines are passed across the bond interface to the analog tier for every one of the 4096 pixels. Thus this chip has over 100,000 interconnects between tiers.

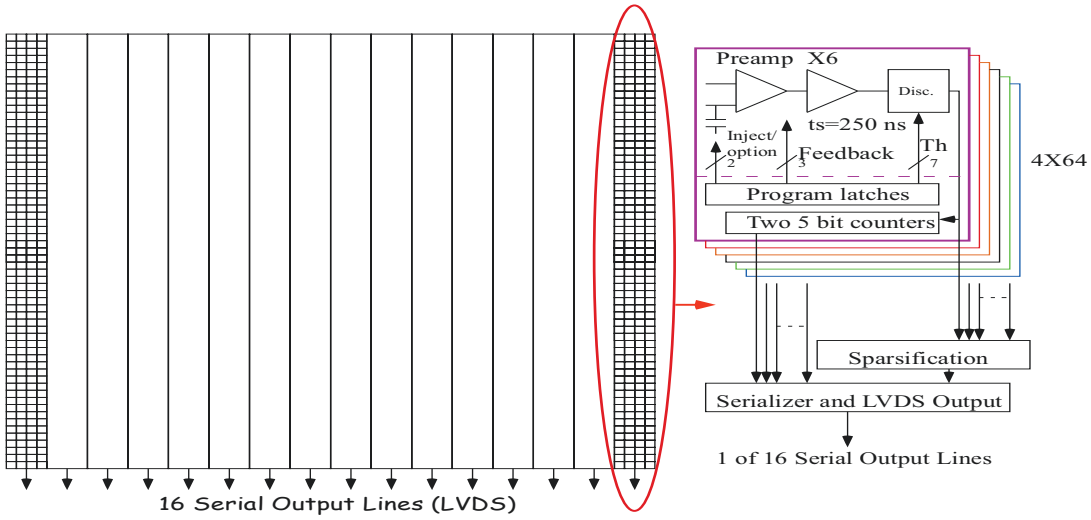

Figure 9 - VIPIC organization. Dashed line on right image indicates circuit split between tiers

After visual inspection, several Tezzaron and Ziptronix chips were wire bonded and tested. Tests confirm that the chips from both wafers work in both operating modes and the configuration registers (up to 49152 bits) work. [8] One important test shows that when 1's are shifted into all cells with the cal strobe, every address is read out in sequential order using the normal readout mode as shown in figure 10. In another important test, all pixels can be killed and when pixels are set in a region of interest, the appropriate sparsified addresses are readout as shown in figure 11.

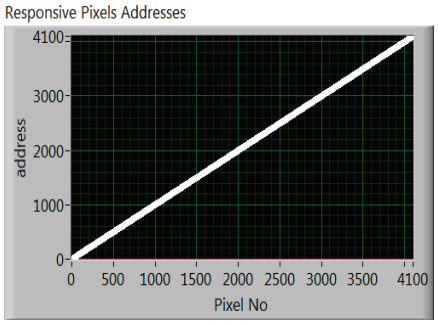

Figure 10 – Sequential address readout.

Figure 11- Proper address readout of region of interest.

In other tests, the discriminator thresholds were reduced to get noise hits and the counters showed non-zero values. As a final test, the 7 bit threshold DACs were set to their end values and the appropriate shift in threshold distribution was observed. Furthermore, the DAC range was found to be wide enough to corrcet for all offsets as seen in figure 12.

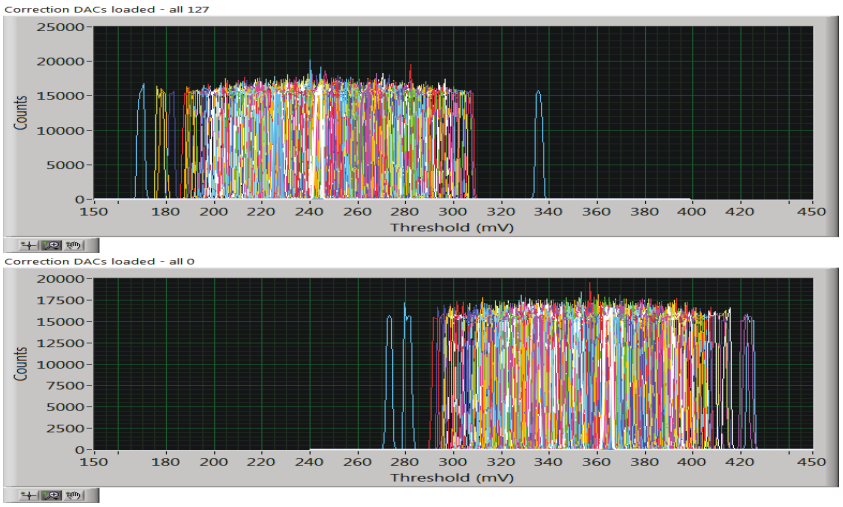

Figure 12- Threshold distirbution of all pixels with threshold DACs set at extreme ends (1111111 in top image and 0000000 in bottom image).

5.0 Future

Positive results on the Tezzaron and Ziptronix bonded chips have also been reported by collaboration members in Italy, France and Germany. Based on these recent results. Efforts are starting toward new 3D submissions for HEP, which will be handled by MOSIS/CMP/CMC.

An entirely new 3D design effort called VIPRAM (Vertically Integrated Pattern Recognition Associative Memory) with unique benefits from 3D circuit concepts, has started at Fermilab. Details of this project were described at this conference [9].

Eighteen new wafers have been fabricated by Global Foundries to replaced our wafers that failed during bonding. Eight of the wafers have been prepared for Cu-Cu bonding in Austria. Another 8 wafers are being prepared for DBI bonding at Ziptronix.

Tezzaron has recently purchased SVTC (formerly Cypress), and is due to receive their own EVG bonder at the end of this year. These additions should allow Tezzaron to assemble 3D chips without dependance on and delays due outside vendors.

6.0 Conclusions

Although there have been a large number of stumbling blocks encoutered with 3D design, fabrication, and assembly, recent positive results on several different designs are encouraging. We have demonstrated 3D chips for HEP using 3 different processes and vendors. This is a big step in showing that 3D chip design for HEP is feasible. It is expected that the path toward 3D designa and fabrication will become easier due to MOSIS, CMP, and CMC providing support and organizing submissions, and the recent acquisitions by Tezzaron.

Acknowlegdements

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