FERMILAB-PUB-11-570-PPD

3D Detector and Electronics Integration Technologies: Applications to ILC, SLHC, and beyond

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Abstract

The application of vertically integrated (3D) electronics to particle physics has been explored by the our group for the past several years. We have successfully designed the first vertically integrated demonstrator chip for ILC vertex detection in the three-tier MIT-Lincoln Labs process. We have also studied sensor integration with electronics through oxide bonding and silicon-on-insulator technology. This paper will discuss the status of these studies and prospects for future work.

Key words: SOI, 3D electronics, vertex detectors, vertical integration

1. Introduction

The next generation of Particle Physics experiments will face unprecedented technical challenges. At the Super LHC detectors will need to cope with luminosities of up to $10^{35}\text{cm}^{-2}\text{sec}^{-1}$ corresponding to ≈ 200 interactions per $25ns$ crossing. At the ILC (or CLIC or muon collider) there will be a premium on precision measurements with good time resolution and low mass. At light sources there is a need for fast, precise x-ray focal plane detectors for a variety of measurements. Building detectors to meet these challenges will require innovative design and optimal use of new technologies.

Promising new technologies are now emerging from the electronics industry, which is faced with its own challenge of continuing Moore's law increases in capability while nearing physical and cost limits of decreasing feature size. Vertically integrated (3D) technology is viewed by many as an answer to this dilemma [1] [2]. Technologies have been developed which allow wafer interconnects at less than 3 micron pitch, thinning to 25 microns and below, and layered connection of bonded wafers. Many of these technologies can be directly applied to particle physics detectors. This paper provides an overview of the work underway at Fermilab to explore some of these applications [3] [4] [5] as well as more detailed descriptions of recent work on laser annealing, oxide bonding, and track trigger applications.

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Preprint submitted to Elsevier *May 6, 2010*

Operated by Fermi Research Alliance, LLC under Contract No. De-AC02-07CH11359 with the United States Department of Energy.

2. The VIP1, a 3D chip for ILC vertex detection

The VIP1 chip was developed to demonstrate the ability of 3D to meet the stringent requirements of low power, low mass, time stamping, and precision required for the ILC. It is a three-tier, vertically interconnected chip fabricated by MIT-Lincoln Labs in their 0.18 micron 3D technology [6]. The tiers consist of 1) amplifier/ discriminator, 2) analog and digital time stamps, and 3) digital control and sparcification.

The basic functionality of the chip was demonstrated including propagation of the readout token, threshold scan, input test charge scan, digital and analog time stamping, and fully sparsified data readout. No problems could be found associated with the 3D vias between tiers. However the chip performance was compromised by a combination of SOI issues and aggressive design. This led to a low yield and small operating voltage margins. In addition there were larger than expected leakage currents in transistors and diodes and poor current mirror matching. An improved version of the VIP1, the VIP2, was submitted to MIT LL last year. The VIP2 design is more conservative, including larger features and less dependence on dynamic logic. The pixel size has increased from 20 to 30 microns. A more complete description of VIP1 test results are available in reference [7].

3. SOI activities

SOI technology provides a route for truly integrated detectors and electronics with the handle wafer forming the detector separated from the transistor layer by a thin buried oxide. We have collaborated with the KEK group on SOI multiproject runs at OKI semiconductor [8]. The Fermilab design is a detector intended for X-ray imaging. The detector and associated testing is described in detail in reference [9]. We are also exploring technologies needed for successful implementation of this technology including wafer thinning, backside contact formation, and techniques to address backgate effects.

3.1. Thinning and backside processing

Standard processing techniques limit the thickness of 6” wafers to about 200 microns, and 8” wafer are typically 700 microns thick. For many applications sensors need only $50 - 200$ microns of thickness to achieve an adequate signal/noise ratio. Therefore thinning of processed sensors is becoming an increasingly important technology. Once thinned, the backside needs to have a good ohmic contact to avoid excessive leakage current after full depletion. These contacts are usually formed by high temperature thermal annealing, which will destroy topside metalization in SOI or hybrid devices. One solution, developed by MPI-Munich [11], is to oxide bond a thinned, backside processed wafer to a handle wafer, which is etched away after full detector processing . We have developed an alternate technique which would be preferred for applications where an initial SOI stack is not practical. This technique uses a pulsed UV laser to locally melt the silicon to re-crystalize and activate ion-implanted dopants. This allows the use of standard thickness single-layer wafers for the initial processing.

3.2. Laser Processing

Wafers were initially bonded to a pyrex handle wafer using a 3M thermal release adhesive. The wafers were then ground to the desired thickness, and chemically-mechanically polished. The backside was implanted with phosphorus at 40 KeV to provide the ohmic contact.

The phosphorus implantation was activated using a 350 nm laser at Cornell University. Four overlapping scans were used, the first was at a lower fluence of 1420 mJ/cm^2 due to the initial amorphous state. The remaining three scans were at 1800 mJ/cm^2. This energy melts the silicon well beyond the 0.1 μm range of the implant to provide a well activated contact region.

3.3. Results

This process was recently completed for a set of SOI-based detector wafers from American Semiconductor produced as part of a US Small Business Innovative Research project. The wafers consist of high resistivity silicon handle wafers separated from the silicon layer used by the electronics by a 200nm thick buried oxide (BOX). Diodes are implanted through the BOX and contacts are formed by etching through the BOX to the diode implant. Each reticule contains a set of 1.5mm test structures with interconnected diode implants as well as strip detector and pixel detector structures. Charge collection was measured directly on the detector by probing the test structure contact with a Picoprobe 12C active probe and illuminating the sensor with a 1060 nm diode [12]. This technique allows direct measurement of charge collection and can also be used to measure the capacitance of test devices by measuring the decay constant utilizing a high impedance oscilloscope probe.

Figure 1 shows IR pulse response as well as IV and CV results for a test structure with 8 micron diodes on 30 micron pitch. The device depletes fully by 6V. Given the 50 micron thickness this corresponds to a substrate resistivity of 1.3 KΩ-cm, about 30% larger than the nominal 1 KΩ-cm quoted by the SOI vendor. The total leakage current at room temperature for the unguarded 1.5×1.5mm test structures at full depletion is about 3 nA.

4. Oxide Bonding

The wafer oxide bonding technologies employed in SOI technology can also be used to bond processed die to sensor wafers. We have studied a technology developed by Ziptronix Inc. which allows either wafer to wafer or die to wafer bonding with interconnect pitch as small as 3 microns. In this process imbedded metal in the die and wafer form an electrical contact when die and wafers with activated oxide surfaces are mated [13] [14].

We used BTeV FPiX 2.1 readout chips (ROIC) which contain a 22×128 array of 50×400 micron pixels fabricated in 0.25 micron TSMC CMOS technology. Sensors were diced from 300 micron thick 6" high resistivity wafers from MIT-Lincoln Labs which included a 50 micron deep trench. Sensor chips were oxide bonded to 8 ROIC wafers then thinned to 100 microns. The backside is left in

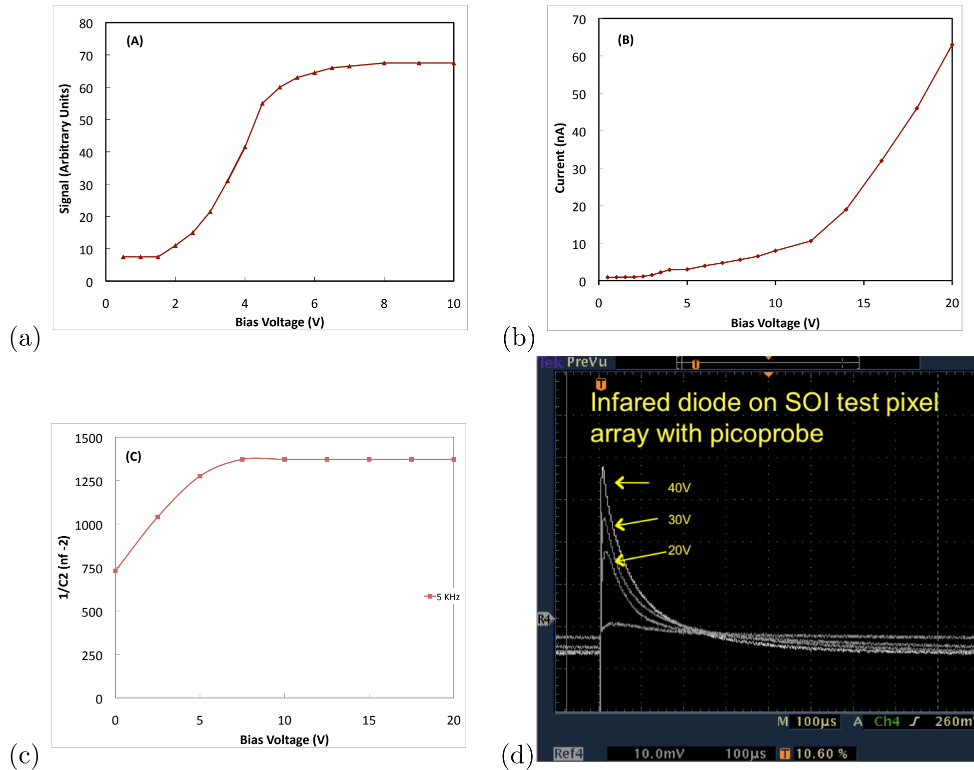

Figure 1: Results of (a) IR diode illumination charge collection and (b) current-voltage and (c) capacitance-voltage scans for 50 micron thick test diode arrays fabricated in the American Semiconductor process. The bottom right plot shows charge collection traces for an unthinned wafer. The fall time decreases as the depletion depth grows. The arrays were illuminated with a 1060 nm infared diode and the resulting charge collection was measured with a Picoprobe 12C.

it's as-ground state. Contact to the backside was made using the conducting trenches on the sides of the die or by coating the backside of the die with an indium-gallium eutectic mixture, which forms an acceptable ohmic-like contact.

Bond voids in the die were detected by scanning-acoustic microscopy. The void rate was 4/21 for wafer 1 and 12/25 for wafer 2. Figure 2 shows results of laser and x-ray bench tests of the bonded devices. All channels appear to be properly connected for die with no voids. Our tests show that the capacitance associated with the interconnect is as least as low as solder bump bonded devices. We saw no evidence of crosstalk from the FPiX chip to the sensor [15].

5. Tezzaron 3D Multiproject Run

Fermilab has sponsored a 3D multiproject run in collaboration with Tezzaron Inc. CMOS wafers with 0.13 micron feature size are fabricated with 6 micron

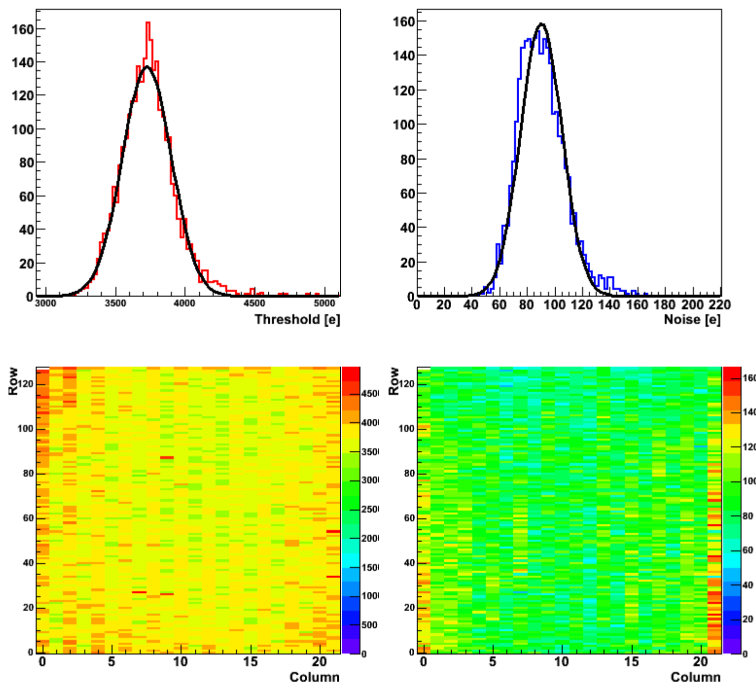

Figure 2: Results of threshold (left) and noise (right) scans for bonded FPiX chips and MIT-LL sensors. Individual results for each pixel in the 22×128 array are shown below the histograms.

deep tungsten through-silicon-vias as a process option at Chartered Semiconductor in Singapore [16]. The top of the wafers contain and array of hexagonal copper pads which form the bond interface. These wafers are copper-copper bonded at 40 PSi and 375 degrees to form a two-wafer stack. One side is then thinned to expose the tungsten vias and metalized to provide external contacts. Processing of the wafers is underway.

6. Application to Super LHC

At super-LHC with a proposed luminosity of 10^{35} cm^{-2} sec^{-1} the standard lepton and jet triggers at CMS will saturate. Acceptable level 1 trigger rates can only be achieved by providing tracker information to the trigger. However the bandwidth needed to collect all of the information generated by a pixelated tracker in a central trigger processor is unacceptable. This makes some sort of local momentum based track filtering crucial. Vertical integration provides a way to locally (=low data transfer power) correlate hit information to limit information transfer to only moderate transverse momentum tracks.

Figure 3a shows a conceptual drawing of a vertically integrated trigger module. Readout chips are oxide bonded to the bottom tier sensor and then thinned to expose the imbedded Through-Sillicon-Vias (TSV). These upper vias are used

to form the contacts to the analog signals from the upper sensor as well as providing an alternate interconnection location for signal and power contacts. Two sensors with $\approx$ 100 micron pitch are separated by a $1-2$ mm thick interposer. Information from the top sensor is transferred vertically down across the interposer to the top surface of the readout chip which combines top and bottom information and generates a signal if the hit pattern is consistent with the momentum cut, reducing the data rate by a factor of 10 or more. A requirement for this design is that the readout chip have direct contact to top and bottom sensors. This can be accomplished either by 3D integration with through-silicon-vias or utilizing SOI or monolithic active pixel sensors.

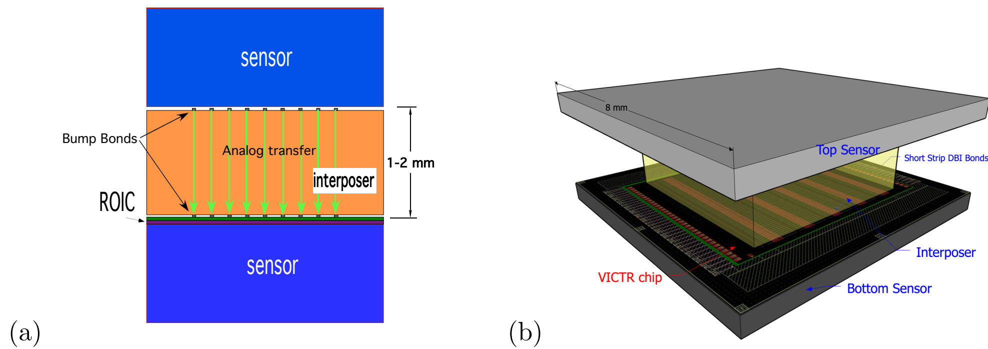

Figure 3: (a) Conceptual drawing of the 3D track trigger stack. Analog sensor signals are transferred through the interposer via bump bonded contacts and processed in the ROIC chip bonded to the bottom sensor. (b) 3D drawing of the track trigger test stack, showing top and bottom sensors, the interposer, and the VICTR chip thinned to 24 microns and DBI bonded to the bottom sensor.

A chip (VICTR) has been included in the Tezzaron 3D run which is intended to demonstrate the vertical interconnection concept. The chip contains 64 amplifier/discriminators on the top tier which is intended to be mated to a sensor with an array of $5mm$ long strips on 80μ pitch. Analog signals from the top sensor are sent across the interposer, which contains an 8×8 interconnect array on 600×640 micron pitch. The bottom tier contains 64×5 amplifier/discriminators which are bonded to $1mm$ strips on the bottom tier sensor. The chip also includes simple logic to form a coincidence between the top and bottom tier discriminators.

The metalized interposer (top) side of the 3D wafer will first be oxide bonded to a handle wafer. The bottom sensor side is then thinned to the TSVs and prepared for oxide bonding. VICTR chips will then be individually oxide bonded to the sensor wafer. Finally the bonded die are thinned to reveal the top metalization for interconnection to the top sensor.

The resulting structure includes the bottom sensor, a chip bonded to the bottom sensor pixels, and topside pads on the chip available for coarse pitch bump bonding. The interposer and sensor are then bumped to ROIC/sensor structure to form the final stacked module. The resulting stack in shown in

figure 3b.

7. Conclusions

The electronics technology associated with 3D circuits potentially offers a rich menu of benefits: low mass, through thinning and bonding; high bandwidth with low impedance connections; radiation hard with thin detectors and deep submicron electronics; low power with low node capacitance, short interconnects; complex functionality with multiple layers each with optimized technology; small pixels with fine interconnect pitch and multiple readout layers; and arrays with no dead regions and 4 side buttable ICs.

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