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Applications of emerging parallel optical link technology to high energy physics experiments

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Abstract

Modern particle detectors depend upon optical fiber links to deliver event data to upstream trigger and data processing systems. Future detector systems can benefit from the development of dense arrangements of high speed optical links emerging from the telecommunications and storage area network market segments. These links support data transfers in each direction at rates up to 120 Gbps in packages that minimize or even eliminate edge connector requirements. Emerging products include a class of devices known as optical engines which permit assembly of the optical transceivers in close proximity to the electrical interfaces of ASICs and FPGAs which handle the data in parallel electrical format. Such assemblies will reduce required printed circuit board area and minimize electromagnetic interference and susceptibility. We will present test results of some of these parallel components and report on the development of pluggable FPGA Mezzanine Cards equipped with optical engines to provide to collaborators on the Versatile Link Common Project for the HI-LHC at CERN.

Keywords: Versatile Link; parallel optics; fibre optic communications

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1. Introduction

The Versatile Link common project is a joint project to specify and develop optical links for use in the HL-LHC upgrades at CERN [1], [2]. This project includes the development of custom radiation hard components for use on the front end of particle detectors. Back end components (off detector) are to be drawn from commercially available components. The Versatile Link standard specifies a point-to-point architecture utilizing components in a standard format operating at a nominal data rate of 4.8 Gbps. Single mode and multimode fibre channels are to be supported with the Versatile Link specification. The single

channel format for the project is the Small Form Factor Pluggable Enhanced (or SFP+) format for back end optical transceivers. Several vendors of this mature technology are also developing parallel optical components (transmitters, receivers, and transceivers) to operate at data rates up to 10 Gbps on each parallel channel.

The use of dense parallel optical modules in detector data readout of high energy physics experiments offers some advantages over single channel formats. By employing parallel channel technology, fibres can be managed more effectively with robust connectors and fibre ribbons. Emerging parallel optical products include a class of devices known as optical engines. These devices allow designers to mount the electro-optical components in locations in the middle of a printed circuit board. This reduces the space needed on the edge of rack-mounted cards and provides the designer with greater flexibility in layout and routing tasks. In addition, by allowing the optical transceivers to be located mid-board, the electromagnetic emissions and susceptibility can be reduced as the length of traces carrying high speed serial data can be minimized.

The Versatile Link project team has begun evaluating the performance of several different devices being developed for parallel optical communications. These devices, driven by the need for high speed data transmission of telecommunications and storage area network markets, are being evaluated using the same measurement techniques as those employed to characterize the SFP+ devices being studied for single channel back end components. Fermilab has partnered with a number of vendors to procure samples of emerging devices. Whenever possible, Fermilab has employed evaluation kits made available by the component vendors to quickly assess the performance of the components. However, in addition to the use of these evaluation kits, Fermilab is also developing custom Field Programmable Gate Array (FPGA) Mezzanine Cards (FMCs) to serve as hosts for several of these optical engines. These FMC platforms can be shared with Versatile Link collaborators to enable them to evaluate the optical engine offerings using FMC-equipped test platforms.

2. Examples of components tested

Figure 1 illustrates the trend in optical transceiver technology as data rates have increased and package sizes have decreased.

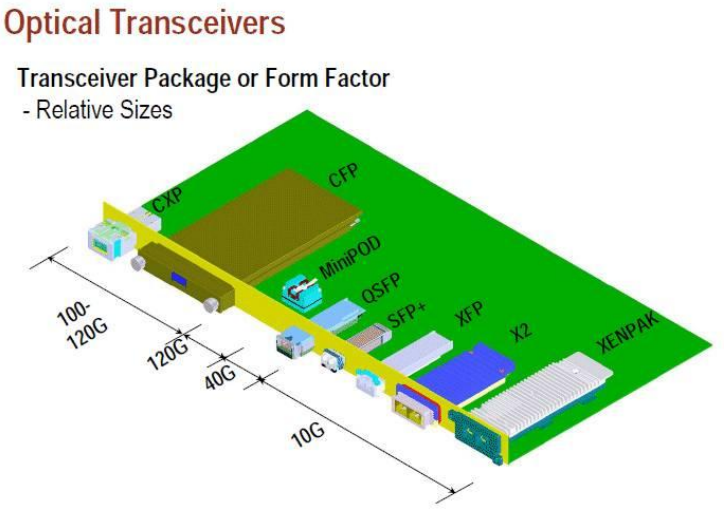
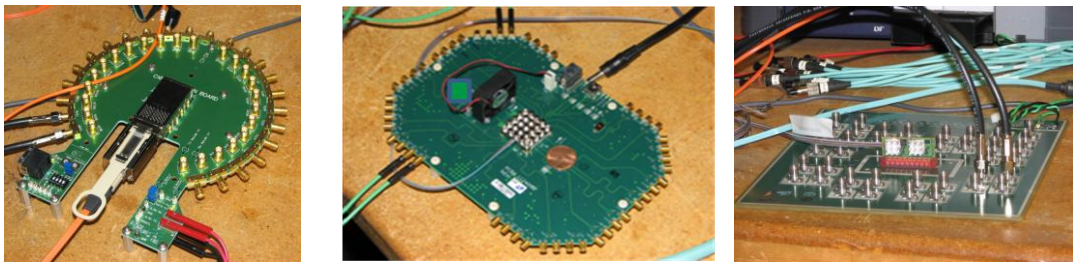


Fig. 1. Evolution of optical transceiver technologies and representative package formats (courtesy of Avago Corporation)

The emergence of standards for single channel and array devices has led to mature products already on the market. In addition to these mature products, new devices in the form of optical engines are being developed. This figure shows a number of devices that are typically mounted on a card edge. In addition, an example of a miniature optical engine is depicted which may be mounted mid-board for improved design flexibility and performance. The improvement in performance may be gained in the integrity of the electrical signals being transmitted and received on the board as metallic trace lengths can be reduced. In addition, the shorter traces needed will reduce the lengths and loop areas of circuits which may emit or receive electromagnetic interference.

At present, many vendors are pursuing different approaches to the design of optical engines. These designs come in variety of packages and channel configurations (transmitters only, receivers only, or a combination of transmitters and receivers as transceivers). Devices are being developed in 12 and 4 channel varieties. Fermilab has obtained samples of some of these devices for testing. Figure 2 illustrates 3 devices tested recently. Each of these devices was provided to Fermilab by vendors along with evaluation platforms for testing the components. These components include 12 channel transceivers and 4 channel transceivers with MTP/MPO connector interfaces to the optical fibres of 12 or 24 fibre ribbons. The device illustrated in Figure 2(a) is an example of a device to be typically mounted on a card edge and installed in an equipment rack. The devices in Figures 2(b) and 2(c) are optical engines which may be mid-board mounted. Note that the evaluation boards all are designed for ease of use with test equipment. In particular, the use of SMA connectors located around the edge of the boards is designed to enable tests to be performed quickly and conveniently using coaxial cables connected to pattern generators and receivers.

Testing of these devices was performed using an FPGA signal integrity kit and standard optical test equipment to measure the performance of electrical and optical signals on the device interfaces. The use of signal integrity kits provides a low cost programmable test pattern generation and error checking capability. With these platforms, bit error rate tests can be performed with a variety of test pattern and encoding options. Optical sampling modules operating at 850 nm are used to deliver the optical test signals to digital sampling oscilloscopes for complete optical eye pattern analysis. Jitter performance is measured with the use of jitter decomposition software and a pattern synchronization module that allows the test equipment to repeat data collection on the individual transitions in the digital test pattern. The transmitter and receiver channels for each of the devices was characterized and compared to per channel specifications being developed for 4.8 Gbps data transmission for Versatile Link compatible systems.



(a) (b) (c)

Fig. 2. Examples of parallel optical devices and evaluation boards: (a,b) 12 channel transceivers, (c) 4 channel transceivers

3. Test results at 5 Gbps

Transmitter tests include the measurement of the following characteristics:

1. Optical Modulation Amplitude
2. Extinction Ratio
3. Eye Opening
4. Rise Time
5. Fall Time
6. Transmitter Deterministic Jitter
7. Transmitter Total Jitter

Receiver tests include the measurement of the following characteristics:

1. Receiver Sensitivity
2. Receiver Deterministic Jitter
3. Receiver Total Jitter

These measurements are standard electrical and optical measurements that are typically made to verify the performance of commercially available devices. The test results presented here are compared with the per channel specifications being developed for array devices for Versatile Link.

3.1 Transmitter Test Results

Figure 3 illustrates results for the measurement of optical modulation amplitude for transmitter channels of the devices. These results are shown against specifications which are designated as “calorimeter grade” and “tracker grade” specifications. The Versatile Link system specifications will include two versions reflecting the specific requirements for inner detector (tracker grade) and outer detector (calorimeter grade) applications. These two grades have different OMA specifications and the data in Figure 3 illustrate the comparison of the channel measurements with each specification. From plots like these, it is possible not only to determine how the measurements compare with the specifications but also the degree to which the devices exhibit uniformity across the channels. This measurement is an important test of the quality of the optical eye pattern under the transmission of pseudo-random bit streams as test data. Such patterns will exercise the system and components under a variety of test conditions and represent a standard way to uncover possible deficiencies in the performance of the components under test.

Figure 4 illustrates a measurement of the data collected for the same set of devices for measurement of the total jitter at the optical output of the transmitter channels on the components. Total jitter is a composite measurement made up of components of both random contributions (which are modeled using normal distributions assumed to be unbounded) and deterministic components (which are themselves composites of several random effects including data dependent jitter, periodic jitter, and duty cycle distortions). Jitter measurements characterize the deviations of timing edges from ideal positions of edges in the data transitions. The effect of timing jitter is one that reduces the temporal width of the eye opening of eye patterns and places more stringent requirements on the sampling position of deserializer circuits typically employed in the receiver channels of FPGAs or ASICs in use in data transmission systems. This optical jitter is seen at the electro-optical circuits at the input to receiver channels of optical communication links.

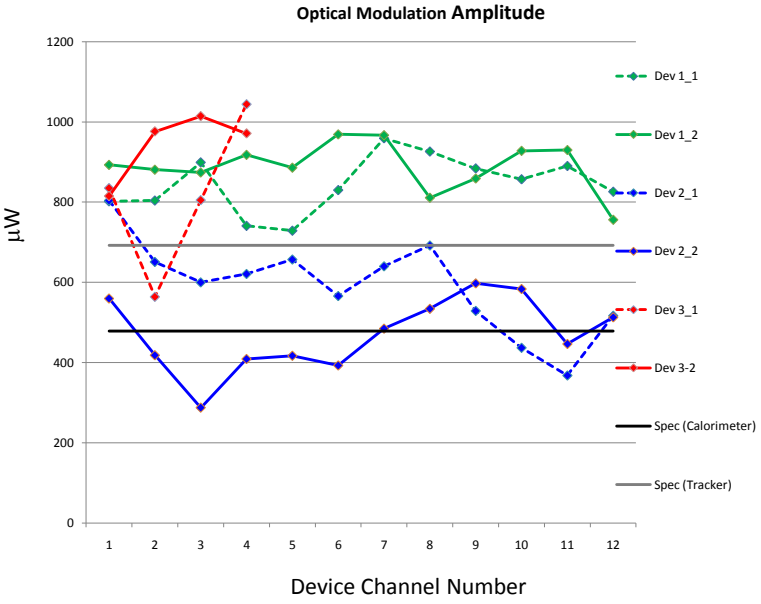


Fig. 3. Optical modulation amplitude measurements for two samples each of three different optical engine families

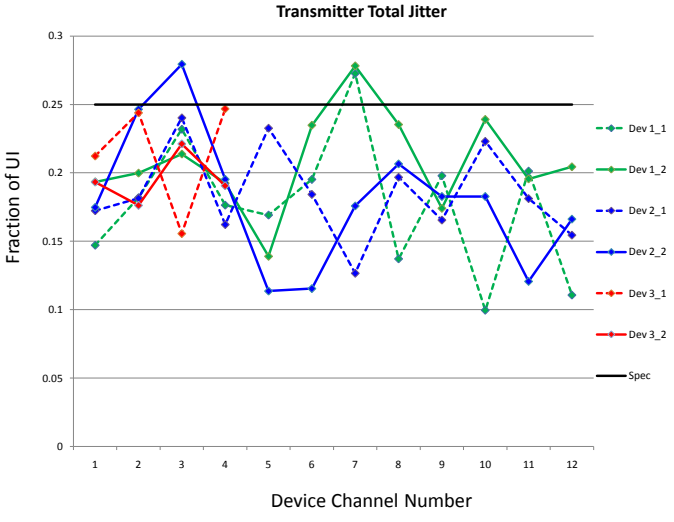


Fig 4. Optical transmitter total jitter measurements for two samples each of three different optical engine families

3.2 Receiver Test Results

Figure 5 illustrates the results of measurements of receiver sensitivity on the receiver channels of the devices. Receiver sensitivity is a measure of the minimum received optical signal amplitude needed to meet a specified level of bit error rate performance.

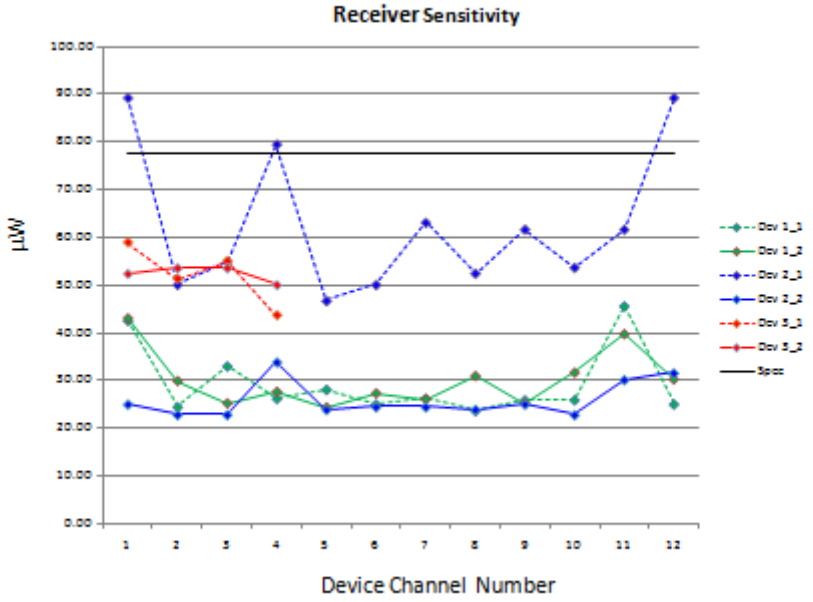


Fig. 5. Receiver sensitivity measurements for two samples each of three different optical engine families

Figure 6 illustrates the results of measurements of the receiver total jitter on each channel of the devices tested. Unlike the jitter measurements shown in Figure 4, these are electrical measurements made at the output of the receiver channels using an electrical sampling module. Jitter measurements made using the digital signal analyzer employed in these tests must be adjusted to remove the effects of other factors to isolate the contribution due to transmitter or receiver components themselves. The adjustment involves isolating the jitter of the stimulus signal from that of the measurements to extract the device jitter. This adjustment uses formulas such as (TJ = total jitter, DJ = deterministic jitter, RJ = random jitter):

$$TJ(device) = DJ(device) + 14*RJ(device)$$

where

$$DJ(device) = | DJ(measured) - DJ(stimulus)|$$

and

$$RJ\ (device)^2 = RJ(measured)^2 - RJ\ (stimulus)^2$$

to make the necessary corrections.

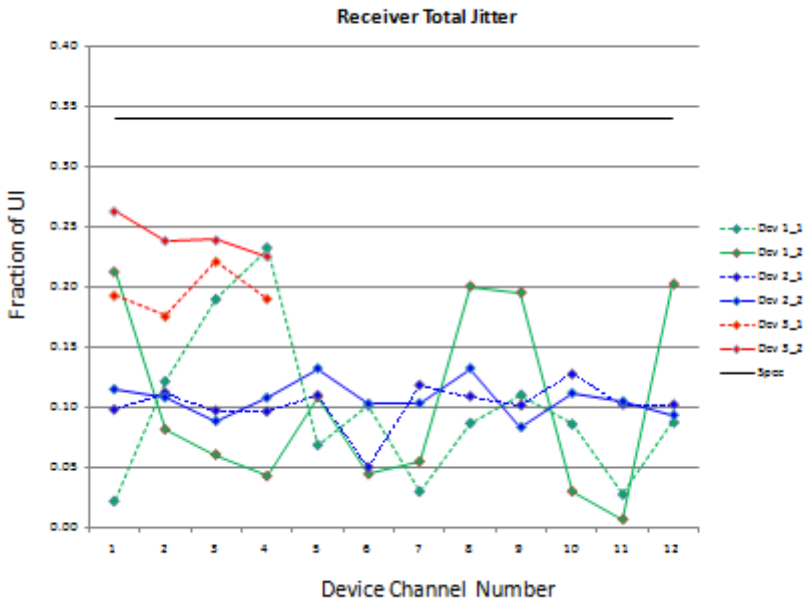
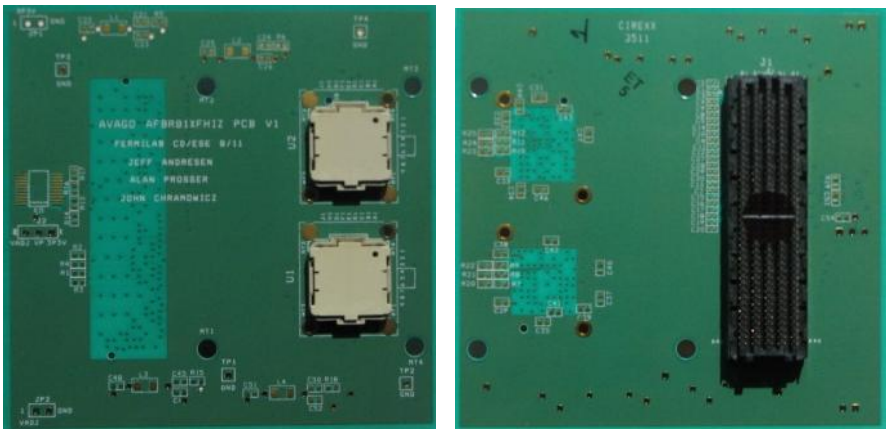


Fig 6. Optical transmitter total jitter measurements for two samples each of three different optical engine families

4. FPGA Mezzanine Card (FMC) Test Platforms

To make the devices tested in this effort available to Versatile Link collaborators, Fermilab has designed custom FMC-based test boards to host various optical engine components. An example of one such design is shown in Figure 7. This figure illustrates the top side (a) and bottom side (b) of the FMC board to be used with 2 optical engines (a 12 channel transmitter and a 12 channel receiver in different packages and to be mounted on the same board). With this hardware, collaborators can access the optical transceivers with high speed electrical data links carried by the FMC connector (not shown on the bottom side of the board) to the Meg Array sockets for hosting the two optical engine devices. These boards represent a more realistic design reflecting a departure from the ideal routing a designer can exploit when



(a) (b)

Fig 7. FMC connector equipped mezzanine card for hosting two optical engines.

designing an evaluation board. For example, the use of the FMC connectors to provide off-board signal access required the board designer to route high speed signal traces on inner layers of the board. This in turn requires vias to be used to complete the routing. Future tests of these boards will illuminate the potential performance impact of such designs on the use of these high-speed devices.

5. Conclusions

The devices that have been tested so far show promise for use as back end components in the Versatile Link project. While some devices show measurements that do not meet the specifications across all channels, further testing is needed to examine a larger number of components. In addition, it should be noted that all of the devices tested here are in the early stages of development and vendors are continuing to work on these designs. Fermilab is partnering with the vendors to provide test results and pursue improvements that will meet the needs of the high energy physics community.

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