

Monolithic Active Pixel Matrix with Binary Counters (MAMBO) ASIC

Farah F. Khalid, *Member, IEEE*, Grzegorz W. Deptuch, *Senior Member, IEEE*, Alpana Shenai and Raymond J. Yarema, *Life Member, IEEE*

Abstract—Monolithic Active Matrix with Binary Counters (MAMBO) is a counting ASIC designed for detecting and measuring low energy X-rays from 6-12keV. Each pixel contains analogue functionality implemented with a charge preamplifier, CR-RC² shaper and a baseline restorer. It also contains a window comparator which can be trimmed by 4 bit DACs to remove systematic offsets. The hits are registered by a 12 bit ripple counter which is reconfigured as a shift register to serially output the data from the entire ASIC. Each pixel can be tested individually. Two diverse approaches have been used to prevent coupling between the detector and electronics in MAMBO III and MAMBO IV. MAMBO III is a 3D ASIC, the bottom ASIC consists of diodes which are connected to the top ASIC using μ -bump bonds. The detector is decoupled from the electronics by physically separating them on two tiers and using several metal layers as a shield. MAMBO IV is a monolithic structure which uses a nested well approach to isolate the detector from the electronics. The ASICs are being fabricated using the SOI 0.2 μ m OKI process, MAMBO III is 3D bonded at T-Micro and MAMBO IV nested well structure was developed in collaboration between OKI and Fermilab.

I. INTRODUCTION

THE combination of detector and signal processing electronics in each pixel is possible by using Silicon-on-Insulator (SOI) Technology. Unlike Monolithic Active Pixel Sensors (MAPS) in CMOS bulk process which offer limited signal processing capabilities and are restricted to the use of NMOS transistors in the active area, the SOI process has the advantage of advanced signal processing capabilities and the use of both NMOS and PMOS transistors. The 0.2 μ m OKI SOI process is available via the SOIPIX collaboration led by KEK. It has a Buried Oxide (BOX) layer of 200nm, in a high resistivity substrate of 1 k Ω cm, n-type handle wafer. Detailed tests from previous designs in this process have led to the conclusion that the process exhibits problems related to capacitive coupling between the detector and electronics. The Monolithic Active Matrix with Binary Counters (MAMBO)

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ASIC has been designed for detecting and measuring low energy X-Rays from 6keV – 12keV for applications such as transmission radiography, autoradiography and fluorescence X-Ray spectroscopy.

II. PIXEL ARCHITECTURE

Each pixel consists of a charge sensitive preamplifier, shaper, baseline restorer, window comparator, 4 bit trimming DACs and a 12 bit ripple counter which can be reconfigured as a shift register.

Each pixel can be configured to several operating modes and can be individually tested. The pixel block diagram is shown in Fig. 1.

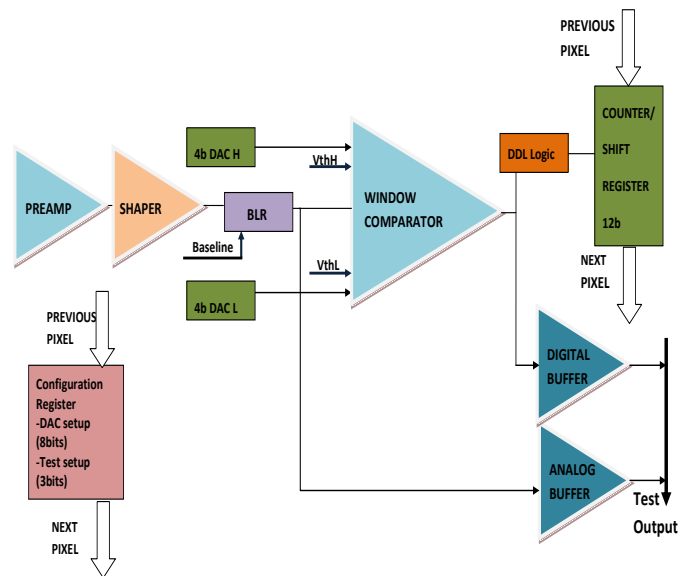


Fig. 1. Pixel Block Diagram

The pixel layout is shown in Fig. 2. Each pixel contains approximately 950 transistors. The primary aim of this design is ease of testability per pixel. The layout has not been optimized for area, in the final version of the ASIC once it is fully tested and characterized a significant part of the test control logic and the configuration register can be eliminated. The analog and digital buffers can also be removed. The area of the counter shift register can be further reduced by using a pseudorandom counter instead of a binary ripple counter. The

above modification would reduce the current pixel size from $100\ \mu\text{m} \times 100\ \mu\text{m}$ to at least $75\ \mu\text{m} \times 75\ \mu\text{m}$.

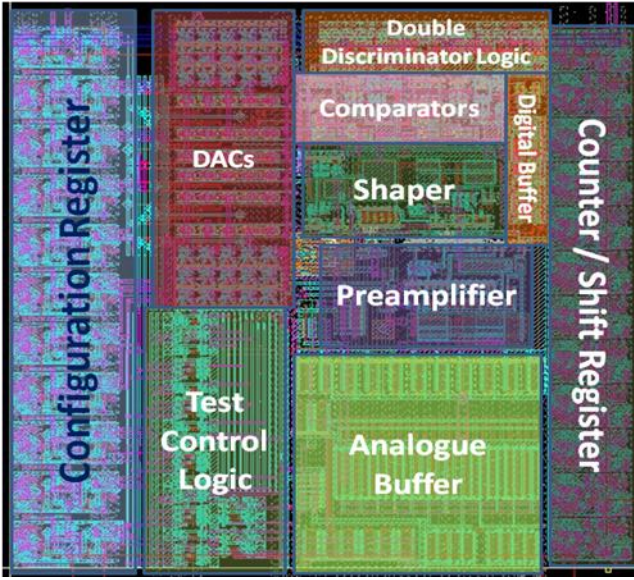


Fig. 2 Pixel Layout

III. IN-PIXEL ELECTRONICS

A. Pre-amplifier, Shaper and Baseline Restorer

A single stage, single ended amplifier in a regulated cascode configuration is used as the charge pre-amplifier as shown in Fig. 3. It has a feedback capacitance of $C_{fp}=5\text{fF}$, an active feedback resistance and a coupling capacitance to the shaper $C_c=35\text{fF}$. The leakage current compensation circuit in the pre-amplifier can tolerate up to 200pA of current, realistic values are not expected to exceed a few pA .

The test setup includes a test capacitance of $C_t = 1.7\text{fF}$ connected on one end to the input through a switch which is ON for calibration and testing phase. Two transmission gates are connected on the other end of the test capacitance. These are connected to in_test_1 and in_test_2 and controlled by strobe1 and strobe2 signals respectively. The calibration circuit produces a pulse of small amplitude V_t , which applied to the test capacitor C_t generates short current pulses of well controlled charge ($Q_{in} = C_t \times V_t$) at the input of the CSA. The amplitude V_t is equal to the difference of voltage on in_test_1 and in_test_2 .

The shaping-filter has two integration stages. The first integration is still in the pre-amplifier, while the second separate stage provides a CR-RC type filtering of the signal and adds voltage gain. The overall degree of the shaping filter is CR-CR². A regulated cascode design in the second stage is designed to provide replica of the DC voltage on the input for proper operation of the nonlinear pole-zero cancelation circuit. A compact design of the second stage was achieved as its transconductance is directly used in the realization of the desired transfer function. The transconductance element $g_m=6.5\ \mu\text{S}$ operates with a feedback capacitance of $C_{fs}=3.5\text{fF}$, an active feedback resistance of $R_{fs}=28\text{M}\Omega$ and the output has a load capacitance of $C_h=25\text{fF}$. Clamping diodes are used in

the feedback to enable a fast overload recovery. Although, a correct shaping of the signal is lost in case of large signals, the recovery to the baseline occurs swiftly. The ratio between the coupling capacitor C_c and the feedback capacitor C_{fs} sets the gain of the shaper equal to 10. The sensitivity of the pre-amplifier, shaper combination is $100\text{mV}/1000+\text{holes}$. The equivalent noise charge is approximately $80e^-$. The input dynamic range is $500h+$ to $4000h+$ for a positive polarity p-on-n type detector.

A simple baseline restorer is used to reduce DC-level variations at the input of the comparators as shown in Fig. 4.

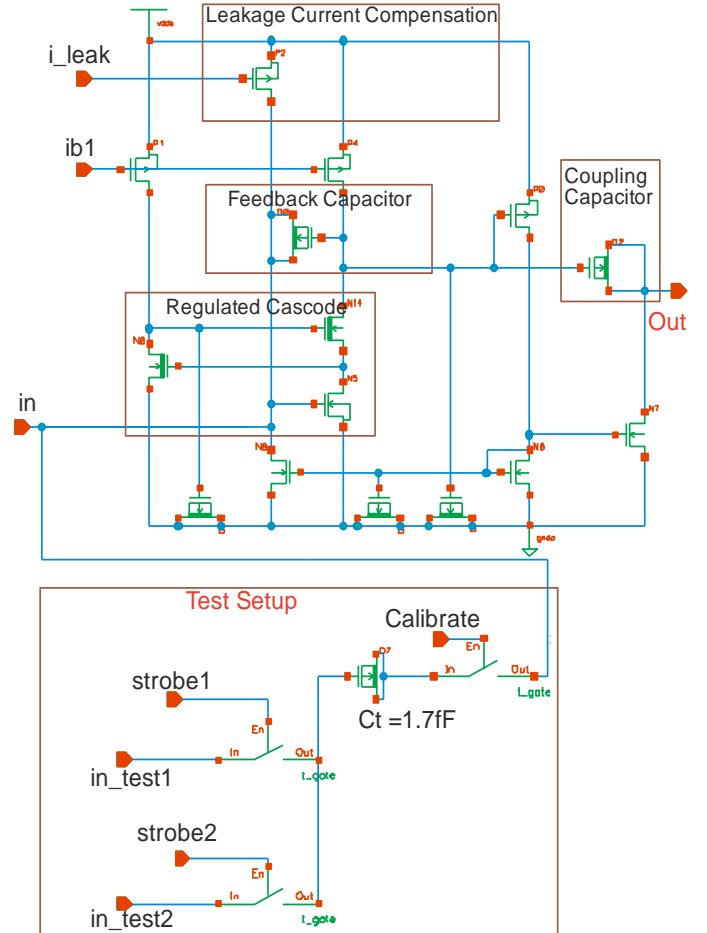


Fig. 3 Charge sensitive Pre-amplifier

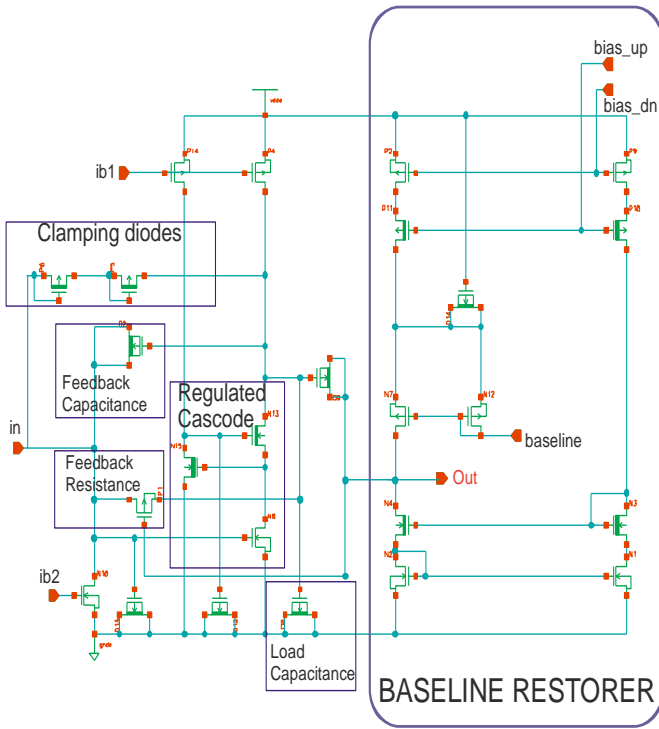


Fig. 4 Shaper and Baseline restorer

B. Window Comparator and trimming DACs

The window comparator consists of two hysteresis comparators in parallel connected to a lower (V_{thL}) and upper (V_{thH}) threshold respectively, the offsets of the comparators can be independently adjusted by the trimming DACs. The double discriminator logic allows the energy windowing function. If $V_{thL} < \text{Signal} < V_{thH}$, then it is recorded as HIT.

Hysteresis Comparator

Source followers isolate the comparator from the shaper as shown in Fig. 5. One input of the discriminator is always connected to the shaper output. During normal operation the other input is connected to the reference voltage (in_vref), when the comparator is being trimmed to cancel offsets, it is connected to the externally generated bias baseline and when the pixel is disabled or during analogue testing it is connected to ground.

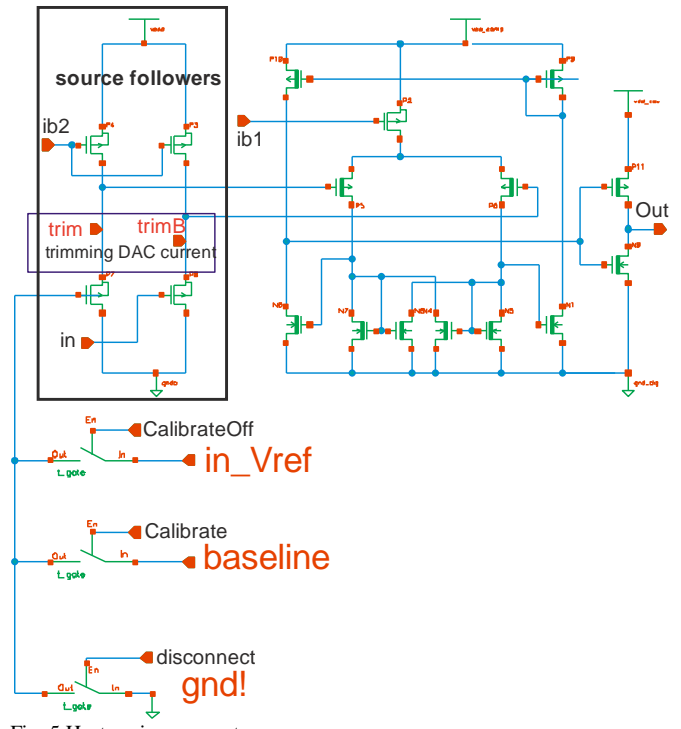


Fig. 5 Hysteresis comparator

Double discriminator logic

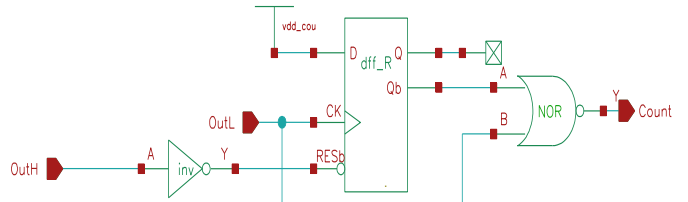


Fig. 6 Double discriminator logic

The double discriminator logic shown in Fig. 6 uses the output of the two comparators for further processing. The output of the lower threshold comparator behaves as a clock. The output of the upper threshold comparator behaves as a reset. If both the comparators fire, the hit is discarded. The Fig. 7 shows the output waveform. Only two hits out of total six are registered as a result of the energy windowing.

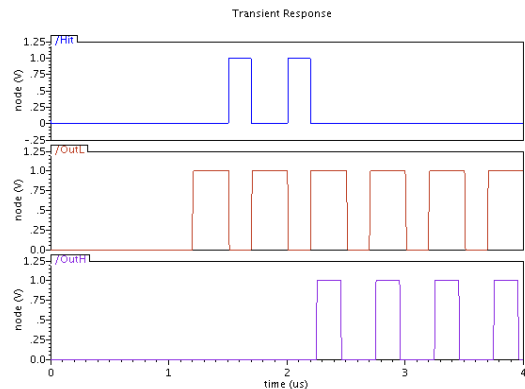


Fig. 7 Window comparator simulation results

Current steering DACs

The current steering DAC consists of cascaded binary weighted current mirrors arranged in conventional symmetrical common centroid geometry. The switches are also binary weighted so that all the current mirrors have equal loads as shown in Fig. 8. Matching is critical for monotonic performance of the DAC. The current can be steered either to the positive or negative terminal. The minimum current of 2nA is used; however this can be increased externally if the offset is more than a few tens of mV.

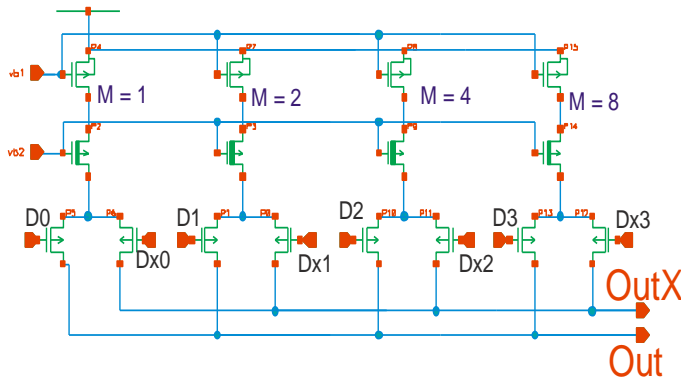


Fig. 8 Current Steering DAC

The output from the trimming DAC cancels the offset at the input of the differential pair of the amplifier.

C. Counter and Shift register

Counter/Shift register consists of a 12 bit ripple counter; the output of the double discriminator logic (DDL) is the clock for the counter. A switch disconnects the counter from the window comparator while shifting connecting the input of the first flip flop to the last flip flop from the previous pixel. An external clock CK_READ is used for shifting data as shown in Fig. 9.

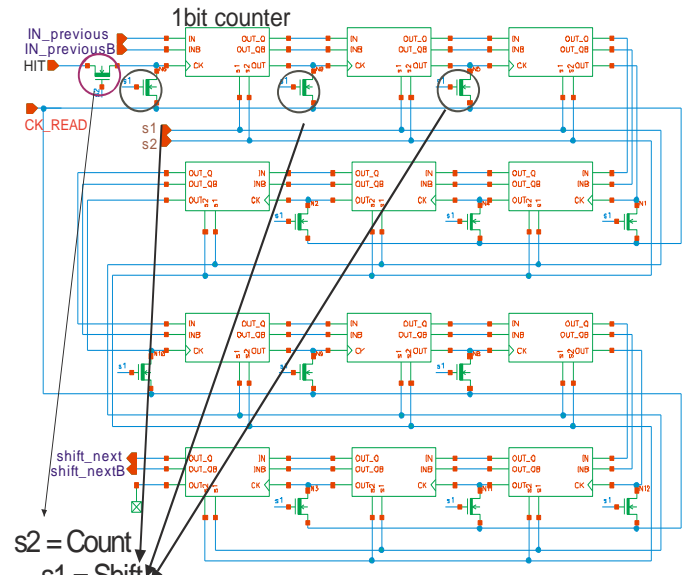


Fig. 9 Counter/ Shift Register

D. Pixel operation modes and test electronics

Each pixel can be individually tested and calibrated with the aid of the pixel configuration register and test logic.

Pixel configuration

An 11 bit configuration register is used to setup the operation of each pixel. The data is input serially using the serial clk. It is then loaded onto a latch using the parallel load signal. 2 x 4bits are used for settings of the two trimming DACs. The rest 3 bits are used by test control logic to setup the pixel for the right mode of operation. 000 is used for normal operation and 111 to disable the pixel. 011 and 100 is used for calibrating the lower and upper DACs respectively. 001 is for analog calibration while 010 is for testing the counter. It also consists of a 3-8 bit decoder and additional combinatorial logic to control switches.

Analog and digital buffer

The analogue buffer is used only for test purposes hence it is disconnected during normal operation. Only one pixel can be tested at a time, hence only one analogue buffer is enabled. The tail current of the buffer is disconnected when it is not in use such that the power consumption of the ASIC is minimized. Source followers are used to shift the voltage level of the signal to the operating range of the buffer amplifier. The buffer is a single stage amplifier with 10 μ A of tail current. It has a gain of about 50dB.

The output of either one of the comparators or the DDL is connected to a digital buffer to enable testing of the digital functionality of the ASIC.

IV. MAMBO III

The T-Micro 3D integration process is used to bond the detector in the lower tier to the electronics in the upper tier. This separates the functions of charge generation and charge processing to two SOI layers, thus, eliminating the direct coupling paths. MAMBO III top and bottom ASIC contains a matrix of 44 x 44 pixels and occupies an area of 5mm x 5mm.

MAMBO III bottom ASIC pixel contains gated diodes; a layout of one element is shown in Fig. 10. The diode is encompassed by a ring of metal. By controlling the voltage of the metal layer any possible short between the adjacent diodes due to surface variation in doping and electrical conditions can be managed. A diode is built with a small p-plus region with a large buried P-well (BPW), almost the same size as the pixel to obtain a parallel electric field in active volume and avoid potential pockets that may alter charge transport.

Each pixel is $100 \times 100 \mu\text{m}^2$ with a $5 \times 5 \mu\text{m}^2$ 3D bump bond pad which has a $2 \times 2 \mu\text{m}^2$ 3D bump bond contact. It is also effectively shielded to electrically isolate the detector from the electronics using metal layers 3 and 4.

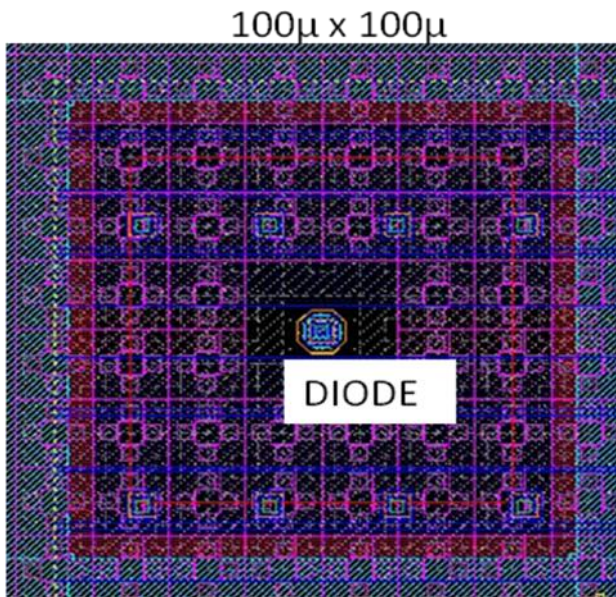


Fig. 10 Diode Pixel

Each pixel has 11 connections, one diode connection from the bottom pixel to the preamplifier in the top pixel. The 10 dummy connections are added to increase the bonding density to satisfy process requirements for better yield. The 3D bonding process requires mechanical rigidity which is enhanced by using more contacts between the two ASICs and eventually epoxy underfill is used. The conceptual diagram of the 3D connection between the two pixels is shown in Fig. 11.

The bottom ASIC does not have any pads for wedge bonding or any other possibility of connecting to the external world. All connections are made using the micro bump bonds to the top ASIC.

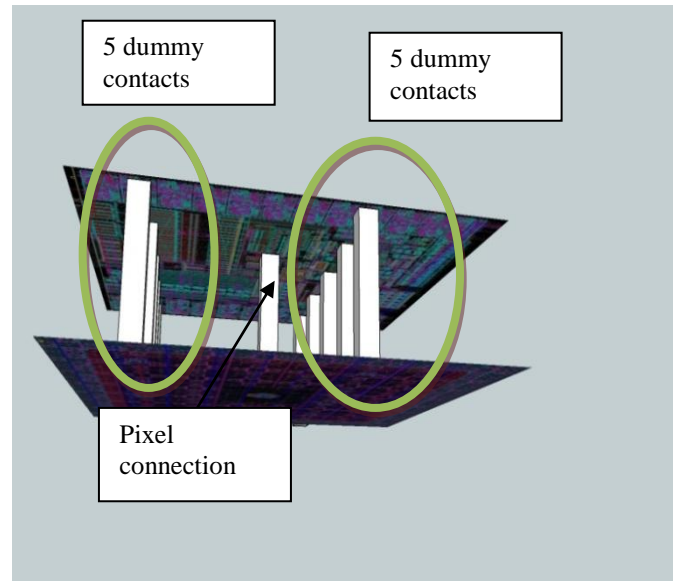


Fig. 11 Conceptual diagram of the 3D bonded pixel

The top ASIC is back thinned. The silicon handle part is removed and through buried oxide (BOX) contacts, inserted at the fabrication of the front-end-of-line part, are exposed. By depositing and patterning metal on the back, all the pads are available on the surface. The through BOX contacts provide electrical connections to the post-processed pads on the surface as shown in Fig. 12.

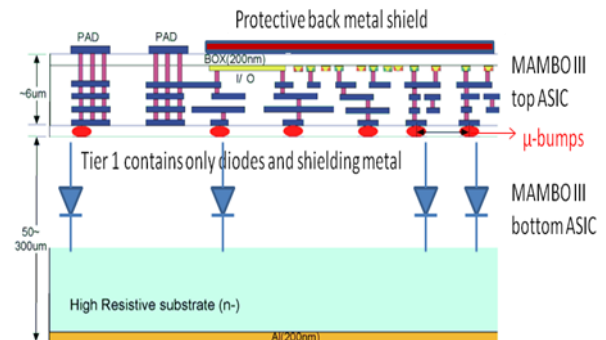


Fig. 12 Cross sectional view of 3D bonded ASICs

After the handle part of the wafer is removed, the transistors and sensitive nodes do not see a reference plane any more. Couplings through the BOX layer of 200nm from external environment and inter-components coupling may be a source of an excess noise in the system, thus the back metal was decided to be used as a shield to protect the transistors, as shown conceptually in Fig. 12 and in the layout in Fig. 13.

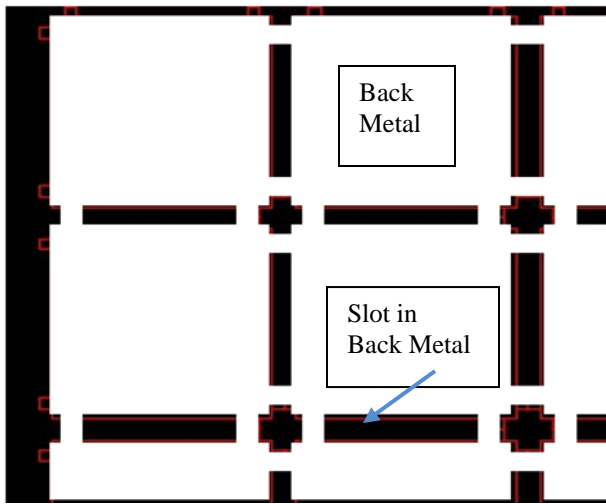


Fig. 13 Shielding per pixel using back metal

T-Micro uses an Au/In + adhesive underfill 3D bonding process. SEM images of the μ bump deposition technique are shown in Fig. 14.

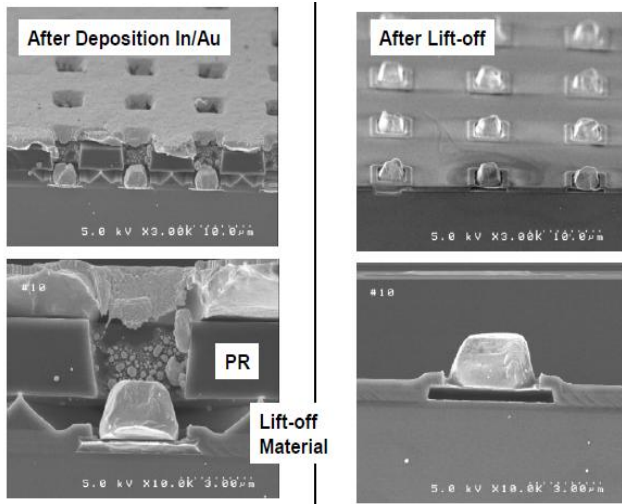


Fig. 14 μ bump deposition

MAMBO III was submitted for fabrication in January 2010; the 2D ASICs were manufactured in May 2010, and due to technological problems with 3D μ -bump bonding process, further process adjustments and repetition of μ -bump deposition is currently being carried out at T-Micro.

V. MAMBO IV

The nested well structure is shown in Fig. 15, it consists of a buried n-well (BNW) underneath all the electronics which acts as an AC ground to all electrical signals capacitively coupling to BNW. A deeper buried p-well (BPW) creates a homogenous electric field through the entire detector volume. This will enable us to once again exploit the advantages of the SOI process with a monolithic combination of the detector and electronics, having eliminated its negative impacts. The main drawback of the nested well structure is the significant increase in diode capacitance as the entire BPW is now the

collecting diode. This capacitance is strongly dependent on the size of the designed pixel, namely on the area of the deep BPW and BNW and the combination of the doping energies and the doses of Boron in the implanting of the deep BPW. In the current layout the diode capacitance is approximately equal to 2pF; in the final design it is estimated that reducing the size of the pixel and further optimizing the conditions of doping of the implant will reduce this capacitance to 1 pF or even less.

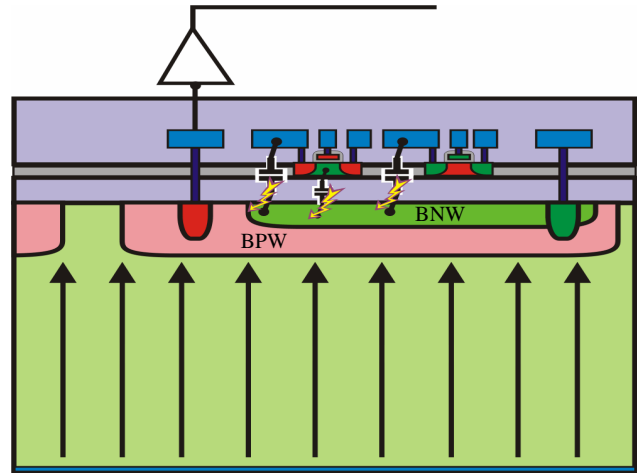


Fig. 15 Nested well conceptual view

The nested well structure was collaboratively developed by Fermilab and OKI Semiconductor Ltd. Fig. 16 shows a Silvaco simulation of the nested well structure using implantation energies for Boron doping of 500keV and Phosphorus doping between 200-300keV.

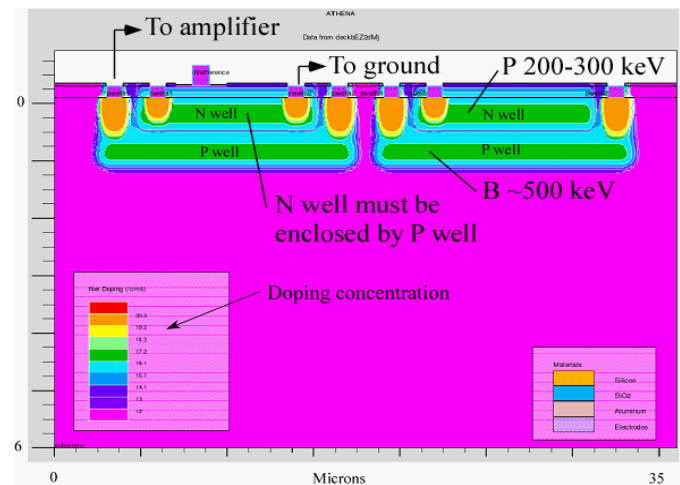


Fig. 16 Silvaco simulation of nested well

Each pixel in MAMBO IV has the same electronics as MAMBO III but the pixel size is increased to $105 \times 105 \mu\text{m}^2$ to meet design rule constraints of minimum separation between adjacent buried p-wells.

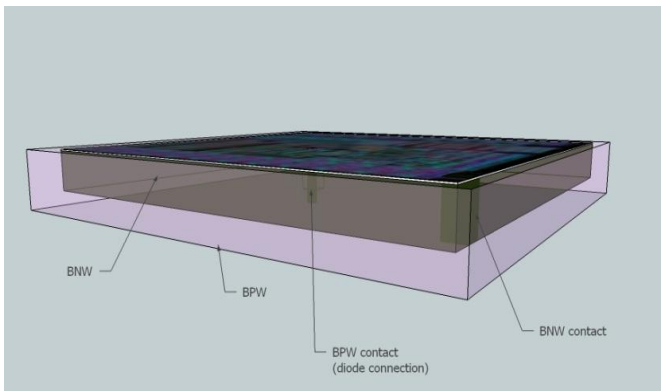


Fig. 17 Model of nested well structure

MAMBO IV ASIC contains a matrix of 41 x 42 pixels and occupies an area of 5mm x 5mm. MAMBO IV was submitted for manufacture in Aug 2010 and is currently being fabricated.

VI. CONCLUSION

MAMBO is a counting ASIC with full testing capability of each pixel. Various methods are explored to avoid coupling between detector and the in-pixel electronics. MAMBO III is a 3D ASIC with the detector and electronics on two separate tiers. The detector is shielded effectively using all available metal layers. MAMBO IV is a fully monolithic ASIC with the high resistivity substrate behaving as the detector. A nested well approach was developed and is used to shield the detector from the electronics thereby eliminating any coupling from the CMOS circuitry into the diodes in the substrate

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